TURUN
YLIOPISTO
UNIVERSITY
OF TURKU

STUDIES OF OXIDE-SEMICONDUCTOR AND METAL-SEMICONDUCTOR INTERFACES FOR REDUCING DEFECT DENSITIES

Masoud Ebrahimzadeh

TURUN YLIOPISTON JULKAISUJA – ANNALES UNIVERSITATIS TURKUENSIS
SARJA – SER. AI OSA – TOM. 705 | ASTRONOMICA – CHEMICA – PHYSICA – MATHEMATICA | TURKU 2023

TURUN
YLIOPISTO
UNIVERSITY
OF TURKU

STUDIES OF OXIDE-SEMICONDUCTOR AND METAL-SEMICONDUCTOR INTERFACES FOR REDUCING DEFECT DENSITIES

Masoud Ebrahimzadeh

TURUN YLIOPISTON JULKAISUJA – ANNALES UNIVERSITATIS TURKUENSIS
SARJA – SER. AI OSA – TOM. 705 | ASTRONOMICA – CHEMICA – PHYSICA – MATHEMATICA | TURKU 2023

University of Turku

Faculty of Science
Department of Physics and Astronomy
Physics
Doctoral programme in Exact Sciences (EXACTUS)

Supervised by

Professor Kalevi Kokko
Department of Physics and Astronomy
University of Turku
Turku, Finland

Docent Pekka Laukkanen
Department of Physics and Astronomy
University of Turku
Turku, Finland

Reviewed by

Professor Filip Tuomisto
University of Helsinki
Helsinki, Finland

Professor Krisztian Kordas
University of Oulu
Oulu, Finland

Opponent

Doctor Rainer Timm
Lund University
Lund, Sweden

ISBN 978-951-29-9578-3 (PRINT)
ISBN 978-951-29-9579-0 (PDF)
ISSN 0082-7002 (Print)
ISSN 2343-3175 (Online)
Painosalama, Turku, Finland 2023

UNIVERSITY OF TURKU
Faculty of Science
Department of Physics and Astronomy
Physics
MASOUD EBRAHIMZADEH: Studies of Oxide-Semiconductor and Metal-Semiconductor Interfaces for Reducing Defect Densities
Doctoral Dissertation, 101 pp.
Doctoral Programme in Exact Sciences (EXACTUS)
December 2023

ABSTRACT

This thesis presents experimental studies of two fundamental components of electronic devices: an oxide- and metal-semiconductor interface. The importance of these interfaces increases continuously when a device size is decreased, and energy-efficiency as well as durability of the devices are increased. It is challenging, however, to characterize the interface properties on atomic level because of their hidden nature beneath the metal or oxide film. Moreover, because the semiconductor surface interacts with oxygen and metal elements during the fabrication of these junctions, electronic defect states form at the interface, lowering device efficiency and durability.

This study focuses on modification and characterization of the following Si(100) and InP(100) semiconductor interfaces: (i) nitridation of HfO_2/Si(100) interfaces, (ii) native oxide modification on n- and p-InP(100), and (iii) Ni/p-InP(100) interface with magnesium surface doping.

The interface properties have been studied by complementary surface-science and electrical methods: scanning tunnelling microscopy/spectroscopy, low energy electron diffraction, X-ray photoelectron spectroscopy, and photoluminescence along with electrical measurements like capacitance-voltage, current-voltage, and contact resistivity. Most interface modifications have been done in ultrahigh-vacuum (UHV) chambers in controlled environments.

The experimental results show that (i) NH_3 nitridation of Si(100) at low temperature reduces the interface defect density at the HfO_2/Si(100) junction, (ii) a proper low temperature gas-based treatment (NH_3 or O_2) improves the quality of the InP native-oxides by reducing the harmful surface defects, and (iii) proper wet chemically treatment combined with UHV-based InP surface modification can reduce the contact resistivity at p-InP contacts.

KEYWORDS: Semiconductor interface, Ultra high vacuum, Wet chemical treatment, Defect state, Contact resistivity

TURUN YLIOPISTO
Matemaattis-luonnontieteellinen tiedekunta
Fysiikan ja tähtitieteen laitos
Fysiikka
MASOUD EBRAHIMZADEH: Oksidi-puolijohde ja metalli-puolijohde rajapintojen tutkimuksia vikatilojen vähentämiseksi
Väitöskirja, 101 s.
Eksaktien tieteiden tohtoriohjelma (EXACTUS)
Joulukuu 2023

TIIVISTELMÄ

Tässä väitöskirjatyössä on tutkittu kahta eri tyyppistä puolijohdekiteen rajapintaa, jotka esiintyvät useimmissa puolijohdelaitteissa. Tutkittavat rajapinnat muodostuvat, kun puolijohdekiteen pintaan liitetään eristävä oksidikalvo tai sähköäjohtava metallikalvo. Näiden laiteosien merkitys kasvaa entisestään, kun puolijohdelaitteiden koko pienenee, ja kun laitteiden energiatehokkuutta sekä kestävyyttä parannetaan. Kyseiset rajapinnat ovat laitteiden heikoimpia osia, koska puolijohdekiteen pinnat reagoivat voimakkaasti eriste- tai metallikalvon valmistusolosuhteiden kanssa aiheuttaen niin sanottuja sähköisiä vikatiloja rajapintoihin. Lisäksi rajapintojen ominaisuuksia on vaikea mitata atomitarkkuudella.

Työssä on valmistettu ja mitattu seuraavia puolijohdeliitoksia: (i) HfO_2/Si(100) jonka Si-pinta käsiteltiin typpikaasulla ennen HfO_2-kalvon kasvatusta, (ii) InP(100)-pinnan oksidien muokkaus typpi- tai happikaasulla ja (iii) InP(100)-pinnan Mg-seostus ennen Ni-metallikalvon kasvatusta.

Rajapintojen ominaisuuksia mitattiin sekä pintatieteen että sähköisten tutkimusmenetelmien avulla käyttäen pyyhkäisytunnelointimikroskopiaa, fotoelektronispektroskopiaa, fotoluminesenssia, kapasitanssi-jännitemittausta ja kontaktiresistanssin määritystä. Rajapintojen ominaisuuksia muokattiin yleensä ultrahyvän tyhjiön kammiossa käsittelemällä puolijohdekiteiden pintoja ennen eriste- tai metallikalvon kasvatusta.

Päätulokset ovat: (i) Si(100)-pinnan käsittely ammoniakki (NH_3) kaasulla tyhjiökammiossa matalassa lämpötilassa pienentää sähköisten vikatilojen tiheyttä ja vuotovirtaa HfO_2/Si(100)-rajapinnassa, (ii) InP-puolijohdekiteen pintaoksidin ominaisuuksien muokkaus NH_3- tai O_2-kaasulla pienentää vikatilojen tiheyttä, (iii) InP-pinnan esikäsittely sopivassa kemiallisessa liuoksessa ja sen jälkeen ultrahyvässä tyhjiössä Mg-atomeilla pienentää Ni-kalvon ja InP kiteen kontaktiresistanssia.

ASIASANAT: Puolijohderajapinta, Ultrahyvä tyhjiö, Kemiallinen esikäsittely, Sähköinen vikatila, Kontaktiresistiivisyys

Table of Contents

Abbreviations

AC	alternating current
ALD	atomic layer deposition
Al_2O_3	aluminum oxide
Al-kα	aluminium kα
C_{ox}	oxide capacitance
c-TLM	circular transfer length method
CV	capacitance-voltage
DC	direct current
ECR	electron counting rule
E_{SS}	energy of surface states
FLP	Fermi level pinning
GRT	generation-recombination time
HCl	hydrochloric
HF	hydrofluoric
hf	high frequency
HfO_2	hafnium oxide
ICT	information and communication technologies
IPA	isopropanol
IV	current-voltage
LDOS	local density of states
LEED	low energy electron diffraction
lf	low frequency
LT	low temperature
Mg-kα	magnesium kα
MIGS	metal-induced gap states
MOSFET	metal-oxide-semiconductor field effect transistor
MOS	metal-oxide-semiconductor
MSI	metal-semiconductor interface
OSI	oxide-semiconductor interface
PES	photoelectron spectroscopy
PL	photoluminescence

Q_{SS}	surface states density
RCA	Radio Corporation of America
RHEED	reflection high-energy electron diffraction
SR-PES	synchrotron radiation photoelectron spectroscopy
STM	scanning tunelling microcopy
STS	scanning tunelling spectroscopy
TLM	transfer length method
UHV	ultra-high vacuum
UPS	ultraviolet photoelectron spectroscopy
VBM	valence band maximum
XPS	X-ray photoelectron spectroscopy
ρ_C	specific contact resistivity

List of Original Publications

This dissertation is based on the following original publications, which are referred to in the text by their Roman numerals:

I **Ebrahimzadeh, M.**, Lehtiö, J. P., Punkkinen, M., Punkkinen, R., Miettinen, M., Rad, Z. S. J., Kuzmin, M., Laukkanen, P., Kokko, K. Effects of thermal vacuum nitridation of Si(100) surface via NH_3 exposure. *Thin Solid Films*, 2022; 757: 139392.

II **Ebrahimzadeh, M.**, Vuori, S., Miettinen, M., Lehtiö, J.P., Granroth, S., Punkkinen, M. P., Rad, Z. S. J., Punkkinen, R., Kuzmin, M., Laukkanen, P. and Lastusaari, M., Properties and modification of native oxides of InP(100). *Journal of Physics D: Applied Physics*, 2023; 56(4): 044001.

III **Ebrahimzadeh, M.**, Granroth, S., Vuori, S., Punkkinen, M., Miettinen, M., Punkkinen, R., Kuzmin, M., Laukkanen, P., Lastusaari, M., Kokko, K. Wet Chemical Treatment and Mg doping of p-InP Surfaces for Ohmic Low-Resistive Metal Contacts. *Advanced Engineering Materials*, 2023; 25: 2300762.

Articles related to this study that were not incorporated into this thesis:

Lahti, A., Santonen, M., Rad, Z., Miettinen, M., **Ebrahimzadeh, M.**, Lehtiö, J. P., Laukkanen, P., Kokko, K., Punkkinen, M., Kuronen, A., Li, W., Vitos, L., Parkkinen, K., Markus, E. Polycrystalline silicon, a molecular dynamics study: Part I - Deposition and growth modes, *Physical Review Materials*, 2023, under review.

Lahti, A., Santonen, M., Rad, Z., Miettinen, M., **Ebrahimzadeh, M.**, Lehtiö, J. P., Laukkanen, P., Kokko, K., Punkkinen, M., Kuronen, A., Li, W., Vitos, L., Parkkinen, K., Markus, E. Polycrystalline silicon, a molecular dynamics study: Part II - Grains, grain boundaries and their structure, *Physical Review Materials*, 2023, under review.

1 Introduction

The modern world is heavily reliant on information and communication technology (ICT). Semiconductor crystals have formed the backbone for advancements in ICT. The demand of modern electronics and photonics is continuously increasing due to the exponential growth of global connectivity. Therefore, engineers and scientists are constantly striving to boost the performance of devices in terms of energy efficiency and durability of devices, data transport speed, and storage capabilities as well as sustainable device manufacturing methods.

Understanding the surfaces and interfaces of semiconductor crystals is becoming critical because surface areas of semiconductor crystals are a limiting factor in many current devices. [1, 2] It has become relevant to modify semiconductor interface properties in such a way that defect densities can be decreased in device materials. [3, 4, 5] Research on semiconductor surfaces and interfaces has made significant improvements during the last 60 years to establish manufacturing parameters and physicochemical properties for state-of-the-art devices. Nevertheless, precise atomic-level understanding of many interface properties remains a long-standing challenge.

This thesis focuses on the characteristics of semiconductor surfaces that form an interface with a metal (MSI) or oxide film (OSI). Both interfaces contribute to guiding the electric current transport in the devices. MSI and OSI are simply made by depositing a metal or oxide film(s) on the top of a semiconductor crystal. The challenge is, however, to produce high-quality interfaces that have a low resistance, low carrier recombination, or/and low leakage current. [6, 7, 8, 9, 10] The semiconductor surface is highly reactive with the surrounding environment, e.g., air, which causes an amorphous layer to form. Furthermore, in the case of the MSI, the metal atoms during the film growth can diffuse into the semiconductor part, which causes point defects. In the case of OSI, most of semiconductors are single crystalline while oxide layers are amorphous or polycrystalline. The amorphous/crystalline interfaces contain many point defects and electrical defect levels, which considerably decrease lifetime and efficiency of devices. Therefore, semiconductor interfaces in more general are a weak part of many practical devices, causing electrical and optical losses.

1.1 Scope of the thesis

This work contributes to the research and development of silicon (Si) and indium phosphide (InP) semiconductor interfaces.

Surface properties were investigated *in-situ* and *ex-situ* manner by surface science methods: low energy electron diffraction (LEED), scanning tunelling microscopy/spectroscopy (STM/STS), X-ray photoelectron spectroscopy (XPS) as well as by electrical measurements: capacitance-voltage (CV) and current-voltage (IV), contact resistivity, and photoluminescence (PL). Both wet chemical pre-treatment and ultrahigh-vacuum based treatment were used to modify the semiconductor surfaces before a thin film deposition. An iterative approach based on complementary electrical measurements and surface modifications was employed to find proper parameters for the interfaces.

1.2 Outline

A background for the publications of this thesis is presented in five chapters.

Chapter 2: Basic properties of semiconductors surfaces: reconstruction, surface band gap, reactivity with many elements.

Chapter 3: Basic properties of OSI and MSI and their role in devices; short description of a transistor.

Chapter 4: Experimental methods, basic working principles, benefits of each method.

Chapter 5: Summary of the main results published.

Chapter 6: Provides the key conclusions derived from the research and offers insights into future work.

2 Semiconductor Properties

Modern semiconductor technology and device physics have motivated also the research of surface and interfaces. Semiconductor interfaces are an active component in many hetero-structure devices. In this chapter, semiconductor surface formation is briefly introduced, and the surface/interface properties are explored in more detail.

2.1 Surface and interface concept

The surface is the area where the bulk lattice structure's regular arrangement is interrupted. A semiconductor interface, as seen in Figure 1, is formed by a finite number of atomic layers that separates a semiconductor bulk from another material (e.g., metal or oxide) when they come into contact. [11] The surface is a simple type of interface when it is in contact with vacuum. It is worth noting that in the athmospheric pressure, an adsorbate layer, typically a contamination-containing layer starts to form immediately. As described further below, the characteristics of the interface (e.g., electrical and chemical) differ dramatically from those of the bulk material.

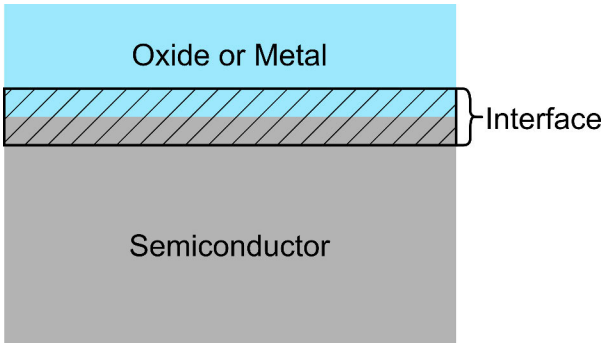

Figure 1. Schematic representaion of semiconductor/metal or oxide interface.

2.2 Geometry of a clean semiconductor surface

Surface atoms lack sufficient neighboring atoms to form a complete bonding configuration (typically four bonds in semiconductors), creating a large concentration of incomplete (dangling, unpaired, or unsatisfied) bonds. The dangling bonds increase the surface energy and reactivity. [12] This causes the surface atoms to be rearranged, resulting in new saturated bonds, which decreases the total energy of the crystal. The atomic rearrangement is classified as (i) relaxation and (ii) reconstruction, as schematized in Figure 2. [13, 14, 15] Relaxation occurs when the spacing between layers changes along the surface normal ($d_S \neq d_B$), but the surface lattice remains constant ($a_S = a_B$). Unlike relaxation, the surface lattice structure alters in reconstruction ($a_S \neq a_B$), but the spacing of the layers remains the same ($d_S = d_B$). Primitive unit vectors of the bulk plane lattice and the surface lattice are a and a_S, respectively. Diffraction techniques, such as LEED and RHEED are useful for observing the reconstruction formation.

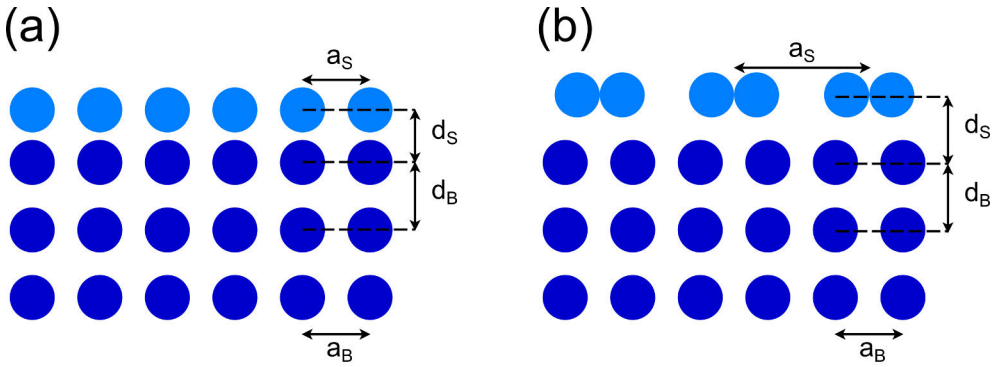

Figure 2. Examples of **(a)** relaxed and **(b)** reconstructed surface.

The surface lattice structure is denoted using the Wood notation as follows [13]:

$$\mathrm{S(hkl)}\left(\frac{a_{S1}}{a_1} \times \frac{a_{S2}}{a_2}\right)\mathrm{R-A} \quad (1)$$

where S(hkl) represents semiconductor material with its face denoted through Miller indexes. R and A are rotation angles between the vectors (i.e., a_S and a) and the element of a possible adsorbate that differs from S. Moreover, the relative vector length is a_S/a. A good example is the dimerization of cleaned Si(100)(2×1), which is a solid of the covalent type. A bulk atom has four bonds, but a surface atom has two bonds to the lower atomic layer, leaving two unpaired chemical bonds on the non-reconstructed Si(100)(1×1). The nearest neighboring atoms are paired together to form dimers at the surface. It reduces the number of dangling bonds in half, lowering the surface energy. On the other hand, a surface stress is likely to compete

with the reconstruction (elimination of the dangling bonds). Therefore, the final structure is a compromise between strain relief and decreasing dangling bonds.

Surface reconstructions are governed by several principles, which give a useful conceptual model for predicting surface structure. Duke summarized these principles, which are as follows [14]:

1. Reconstruction occurs to decrease the density of dangling bonds by forming new bonds between surface atoms. Dimerization of the Si(100)(2×1) surface atoms is an example, on which a regular array of dimers are closely spaced (Figure 3a).
2. Relaxation of surface atoms happens to lower the unfavourable surface energy, which instead of metallic states, produces insulating or semiconducting surface energy bands (i.e., an energy gap). Tilting of Si(100)(2×1) dimers is known as a result of relaxation, which leads to band gap opening (Figure 3b).
3. The preparation conditions determine the lowest energy structure that is kinetically accessible. Si(111) experiences (2×1) reconstruction on a cleaved surface, while it changes to a lower energy (7×7) structure as a result of annealing above 400 °C.

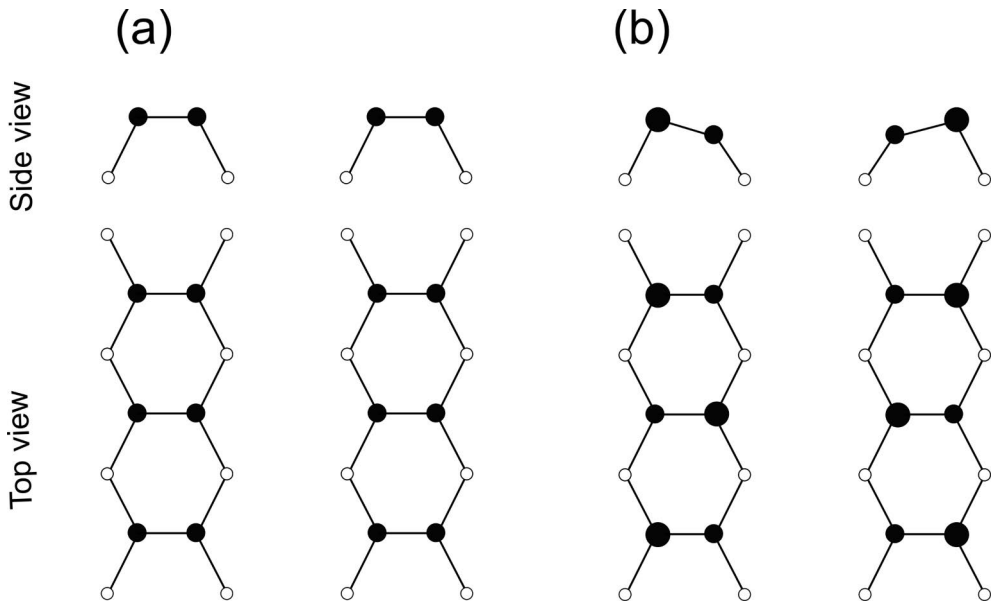

Figure 3. Model of the Si(100)(2×1): **(a)** symmetric dimerization of surface atoms and **(b)** buckling of dimers in up and down. [16]

These principles apply to different semiconductors such as silicon, germanium and III-V compound semiconductors. In addition, so-called electron counting rule (ECR) is often described to predict the formation of reconstructions on III-V surfaces, for example on GaAs and InP. [17] The ECR is based on the knowledge about the dangling-bond induced electron levels around the band gap: group-V dangling bond levels lie below the Fermi level near the valence band maximum (VBM), while group-III dangling bond levels lie above the Fermi level near the conduction band minimum. Therefore, the group-V dangling bond levels should be fully filled by valence electrons, while group-III dangling bonds should be completely empty, to have an insulating band structure. If there are partially filled bands, the surface structure is metallic. The band gap opening decreases the total energy. In the ERC, number of the valence electrons are calculated and compared to the amount of the dangling-bonds, taking into account that each group-III atom donates 3 valence electrons and each group-V atom donates 5 electrons to a joint or shared valence electron pool. The adsorbate-induced surface structures are substantially governed by the same concepts stated above.

The ECR predicts that a (2×4) or (4×2) reconstruction is the smallest unit cell for III-V(100) surfaces. Indeed, the (2×4) or (4×2) reconstruction has been found for many III-V(100) such as GaAs(100), InP(100), InAs(100), InSb(100). The GaAs(100)(2×4) reconstruction includes dimer rows and missing dimer trenches. The atomic structure of the InP(100)(2×4) is different from the GaAs one because InP(100) can have a cation-rich terminated surface, a trimer-like structure was suggested, as seen in Figure 4. [18] The dimerization of In-P atoms explained this trimer, which has not been reported for GaAs(100)(2×4).

Furthermore, a (2×1)/(2×2) surface reconstructions were observed on InP(100), which was considered to violate the ECR in the beginning. However, later it was realized that this P-rich InP(100)(2×1) included also hydrogen (i.e., H-termination or passivation). [19] The presence of an H-adsorbate atom in the uppermost atomic layer resulted in long-range ordering and was most likely connected to P atoms. The STS measurement confirmed that this surface was semiconducting (i.e., bandgap greater than 1 eV), indicating that ECR was obeyed.

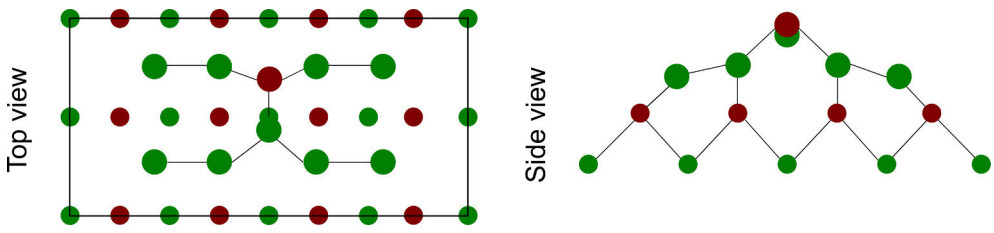

Figure 4. The InP(100)(2×4) surface is represented by a mixed In-P dimer model; top view and side view. P and In atoms are represented as red and blue circles, respectively. [18]

2.3 Semiconductor surface reaction

Surface reactivity refers to the ability of a semiconductor surface to undergo chemical reactions. Generally, semiconductor surfaces are highly reactive with the surrounding environment (Figure 5), which causes the formation of new interface layers (1-10 nm thick) with different chemical and physical properties. Semiconductor crystals typically contain an oxidized surface because semiconductor oxidation is an energetically favoured process, and it is extremely difficult to avoid air contact. Take Si for example, the bond energies between Si-O, Si-C, Si-H, and Si-Si are 798, 435, 334, and 327 kJ/mol, respectively. [20] This means that the total energy of the material system, including a semiconductor crystal and oxygen gas, decreases via forming Si-O bonds and a surface oxide.

The common feature of such reacted semiconductor surfaces is that they have more or less an amorphous atomic structure, in contrast to the well-crystalline bulk semiconductor. Furthermore, an amorphous solid naturally includes higher density of point defects (e.g., interstitials, vacancies, and substitution impurities) than the corresponding monocrystalline material. The difference in geometry and occupation of bonds at the surface alters the electronic properties of semiconductors.

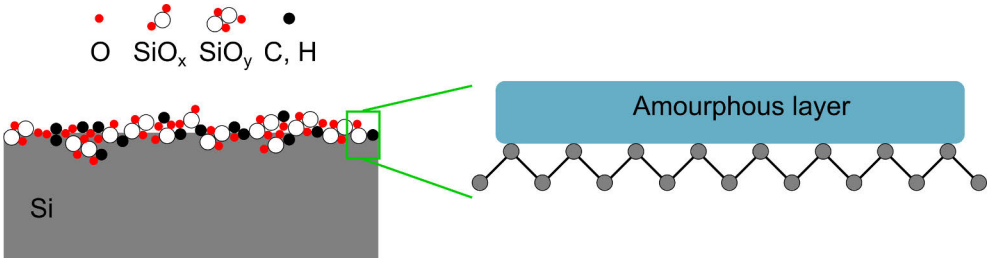

Figure 5. An illustration of the problem with semiconductor surfaces and their reactivity with the environment, which forms an amorphous layer on semiconductor. [13] For instance, an air-exposed Si crystal has a defect-rich oxidized surface portion.

Furthermore, semiconductor interfaces suffer from uncontrolled diffusion of the metal elements or/and oxygen during film growth. Atomic structures formed as a result of such interactions are often poorly defined, amorphous, or disordered. The chemical composition of the reacted semiconductor layer is often different from that of the pure semiconductor. For example, during the formation of MSI, metal elements diffusion, partial oxidation, and contamination with C or H lead to high electronic defect density levels around the crucial band gap of semiconductors. Semiconductor interface states can be explained by a variety of models, including metal-induced gap states (MIGS) [21], unified defect model [22], and unified disorder-induced gap states. [23]

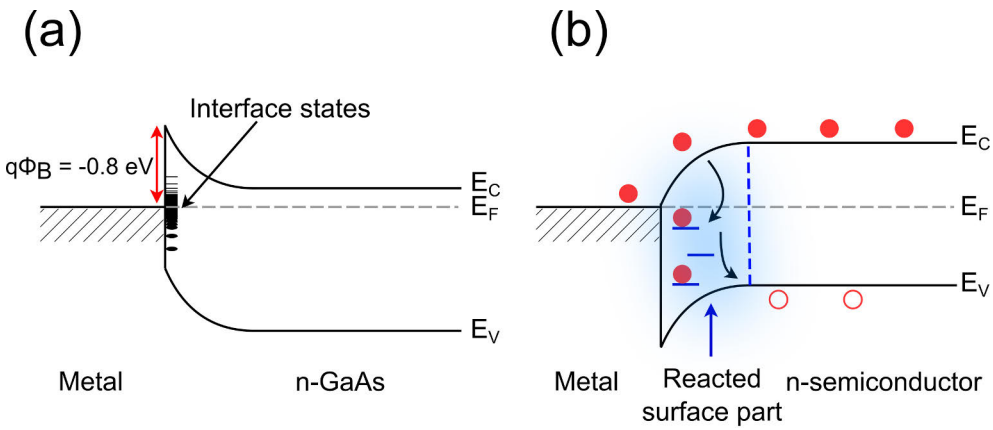

Figure 6. **(a)** FLP in n-GaAs by interface states regardless of metal choice: E_F is pinned around E_C-0.8 eV. [24] **(b)** A diagram illustrating how interface states (blue short lines) at MSI create losses. The full red circles represent electrons, whereas the empty red circles represent holes. E_C, E_F, and E_V reflect the energy of the conduction band, Fermi level, and valece band, respectively.

They also cause the Fermi level pinning (FLP) at specific energies in the band gap, for example in n-GaAs (Figure 6a). The density of these states is often higher than 1×10^{13} $eV^{-1}cm^{-2}$ for interface layers. [24] Low-quality interfaces cause various loss processes. The states operate as charge carrier traps near the surfaces or generate non-radiative recombination centers (Figure 6b). These states degrade the electrical performance of devices by decreasing the efficiency of the electronic devices with increasing energy dissipation and decreasing durability.

2.4 Semiconductor surface bandgap

The surface bandgap of a semiconductor is an important characteristic. Usually, even a clean and well-crystalline surface of a semiconductor does not have the same energy gap as the bulk. For example, the surface band gap on a cleaned Si(100) surface is smaller than the bulk band gap (~ 0.6 eV *vs.* ~ 1.1 eV). The buckling of dimers (Figure 3b) on the Si(100)(2×1) surface leads to the formation of full and empty dangling bonds, pushing the states away from the Fermi level and therefore opening the surface bandgap. In other words, Si(100) with the symmetric dimers would be a metallic. An oxidized surface, on the other hand, has a higher bandgap than the bulk because it contains a partly ionic Si-O bond, which raises the energy required to extract electrons from Si-O bonds, thereby increasing the band gap. On oxidized surfaces, however, Si dangling bonds are often present, resulting in gap levels.

2.5 Semiconductor surface cleaning

As previously described, the reactivity of semiconductor surfaces with the environment makes it difficult to sustain a clean, crystalline semiconductor surface and preserve its crystallinity. Thus, to remove most surface oxides, semiconductor crystals are commonly pre-treated using chemical etching: e.g., dipping in hydrochloric (HCl)- and/or hydrofluoric (HF)-based solutions. The use of hydrogen to passivate the Si surface has been the subject of extensive research. [25, 26, 27] Besides providing a passive layer for Si, the hydride groups provide a flexible foundation for subsequent attachment chemistry. [28] Different recipes have been used to terminate the surface with Si-H bonds. The well-known method was suggested by Weldon *et al.* in which the Si is soaked in aqueous HF acid solutions. [29] Silicon dioxide (SiO_2) is etched by HF, the Si surface is terminated with H as a result of the etching. Since the Si-F bond is substantially stronger than the Si-H bond (585 vs. 334 kJ/mol), the surface was initially considered to be F-terminated, but studies eventually revealed that the surface is H-terminated.

It may be difficult, however, to achieve a well-crystalline surface with only chemical treatment. This means that a chemically etched semiconductor surface often includes a thin amorphous layer (0.5 nm or more in thickness), as shown in Figure 7a,b. Moreover, to effectively reduce the reaction rate of disruptive species, a possible strategy is to introduce the chemically treated sample into ultra-high vacuum (UHV) system. Thermal heating of the sample is one way to remove contaminants from its surface. To remove C and O atoms from semiconductors, high temperatures are generally required; however, semiconductors may melt at this temperature. For Si crystal, flash heating is an option in which the Si is heated to nearly 1300 °C for a few seconds. [13, 30]

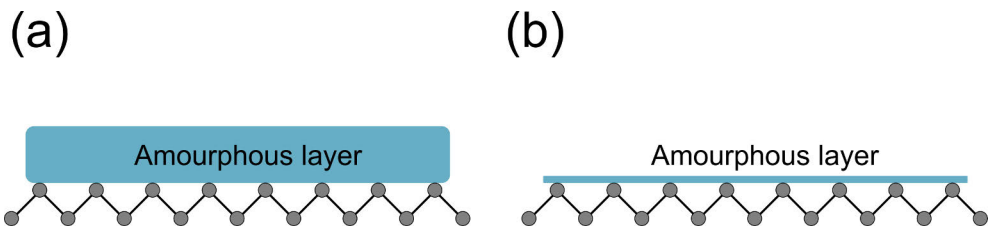

Figure 7. Surface structures of common semiconductors **(a)** before and **(b)** after chemical cleaning. [13]

In the context of III-V materials, a common cleaning procedure involves applying a protective layer of amorphous As or Sb onto the surface. [13] Furthermore, proper sample preparation (i.e., chemical cleanings and thermal annealing) is of great importance to provide an oxide-free surface. In case of InP,

HCl- and HF-based chemical pre-treatment have been investigated. [31, 32] The most proper strategy is combination of the HCl-based cleaning followed by thermal heating at 300 °C. It produces a high-quality surface with less surface roughness than the HF-based approach, preventing surface deterioration. Also, wet chemical etching produces often a group-V rich surface, and post-heating is needed to remove the extra layer. It is useful to verify the atomic structure and the removal of contaminants on the surface regardless of the cleaning method used to grow MSIs and OSIs.

2.6 Chemical passivation

To enhance the interfacial quality prior to oxide and metal deposition, despite *ex-situ* chemical pre-treatments, different chemical surface passivation techniques have been explored to suppress undesired effects caused by pre-existing defects as well as the rapid re-oxidation of the surface after wet chemical cleaning. [33, 34]

For instance, sulphur passivation has been reported to diminish the density of states at the InP(100)/Al_2O_3 interface. One of the most appealing chemical treatment methods is exposing the surface to an N-rich environment to nitridate the surface. Nitridation has been shown to reduce undesired charge carrier recombination, improving device performance and lowering the density of electronic defects and traps on the surface. [35, 36, 37, 38] The nitridation has been studied on a wide range of semiconductors, including elemental and compound semiconductors such as Si, GaAs, InP, and others. The mainly methods for introducing nitrogen atoms onto the surface are plasma-enhanced chemical vapor deposition (PECVD) and thermal nitridation. The incorporation of N into interfaces is indeed an important phenomenon with implications for various technological applications such as transistors, photovoltaic, and photonic.

Silicon nitride (Si_3N_4) and silicon oxynitride (SiO_xN_y), as surface nitridation derivatives, are both very attractive to be integrated in the device structure. For example, Akkaya *et al.* [39] investigated the electrical properties of the Sn/SiO_xN_y/p-Si stack, where oxynitride layer has been deposited using plasma process, and found a reduction in the interface state density. Also, III-V surfaces suffer from the poor quality of the surface, due to high defect density (> 10^{13} $eV^{-1}cm^{-2}$) (see sec. 2.3). The nitridation of the GaAs nanowire surfaces, investigated by Alekseev *et al.* [40], led to a higher conductivity and lower surface defect (by a factor of 6).

In our studies, we used thermal vacuum nitridation with NH_3 to enhance the surface and interface properties of both Si and InP at low temperatures (Publications **I** and **II**). The fact that plasma sources have been shown to reduce surface crystallinity encouraged us to use the concept of thermal nitridation without plasma.

3 Metal-Semiconductor and Oxide-Semiconductor Interfaces

The importance of the semiconductor surface properties has been clarified in the previous chapter, where the properties of the bulk semiconductor are altered due to the unsaturated chemical bonds and reactivity of the surface. This chapter provides a survey of the basic physics of the MSI and OSI, which are two significant parts of electronic devices responsible for electric current transport.

3.1 Metal-Semiconductor interface (MSI)

In applications, the semiconductor components are connected to each other in a circuit through metal contacts. Therefore, it is relevant to minimize the contact resistance to reduce the resistive heating losses. Theoretically, when a metal and semiconductor are brought into contact, there are basically two types of junctions formed depending on the work function difference between a semiconductor (Φ_S) and metal (Φ_m) [41]:

- Ohmic contact refers to a low resistance and non-rectifying (non-directional) metal to semiconductor contact.
- Schottky contact refers to a high resistance and rectifying (non-Ohmic) metal to semiconductor contact.

In an ideal contact, the Schottky barrier height ($\emptyset_B$) is given [42]:

$$\Phi_B = \Phi_m - \Phi_S. \tag{2}$$

A Schottky contact or an Ohmic contact can be formed by both n-type and p-type semiconductors. In n-type semiconductors, an Ohmic contact is formed when $\Phi_m < \Phi_S$ and a Schottky contact is established when $\Phi_m > \Phi_S$, as shown in Figure 8. Conversely, for p-type semiconductors (not shown), an Ohmic contact is established when $\Phi_m > \Phi_S$, whereas a Schottky contact is formed when $\Phi_m < \Phi_S$.

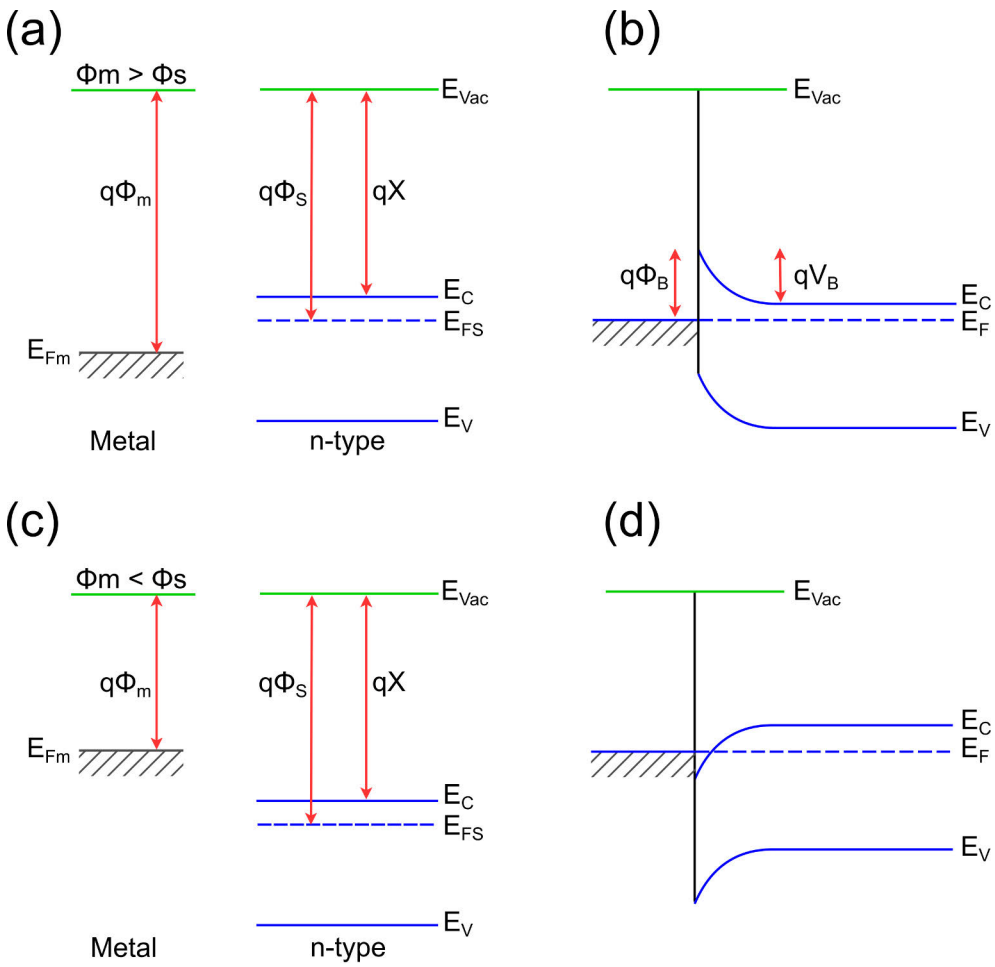

Figure 8. Formation of Scohttky contact for n-type semiconductors **(a)** before contact and **(b)** after contact. Formation of Ohmic contact for n-type semiconductors **(c)** before contact and **(d)** after contact. (X represents the semiconductor electron affinity. E_{Vac}, E_{Fm}, E_{FS}, E_C, E_F, and E_V are the energies of the vacum level, metal Fermi level, semiconductor Fermi level, conduction band, Fermi level, and valece band, respectively.) [42]

In real-world situations, the above-mentioned relation does not explain MSI behavior well because a semiconductor surface affects the energy to remove electron from a crystal. A low-resistance Ohmic-type contact to feed electrical current toward a semiconductor component is frequently required. In many semiconductor applications, however, the MSI often follows the Schottky model, resulting in a potential barrier between the metal and semiconductor regardless of the metal used (Figure 6a, chap. 2). Myerhof, for example, observed no relationship between the barriers and variations in the work functions for different metals on Si and Ge. [43] Bardeen explained the failure of Eq. (2) and proposed that the contact potential

difference between metal and semiconductor is caused by localized surface states. [44] Semiconductor surfaces can contain inherent states (i.e., dangling bonds), or external agents (e.g., oxidized surface and/or MIGS) that may influence the potential at the contact. [45] Figure 9a illustrates how surface states at the semiconductor-vacuum interface bend the semiconductor's electronic bands and create this barrier. [42] The acceptor-like states of an n-type semiconductor (i.e., electron trapping) cause an upward band bending and a shift in the surface Fermi level toward the energy of surface states (E_{SS}). As seen in Figure 9b, if the surface states density (Q_{SS}) is high enough, the contact with metal will not affect the surface Fermi level position (and $q\Phi_B$). The charges from these states are transferred to the metal side, resulting in a capacitive layer with a positive charge on the semiconductor side and a negative charge on the metal side. Therefore, the barrier is determined by the position of the E_{SS}, not the metal type. Thus, in practice, it is not easy to make Ohmic contacts. Hence, semiconductor surfaces need to be modified to enable the movement of electrons without losses by overcoming potential barriers and thereby lowering the contact resistance.

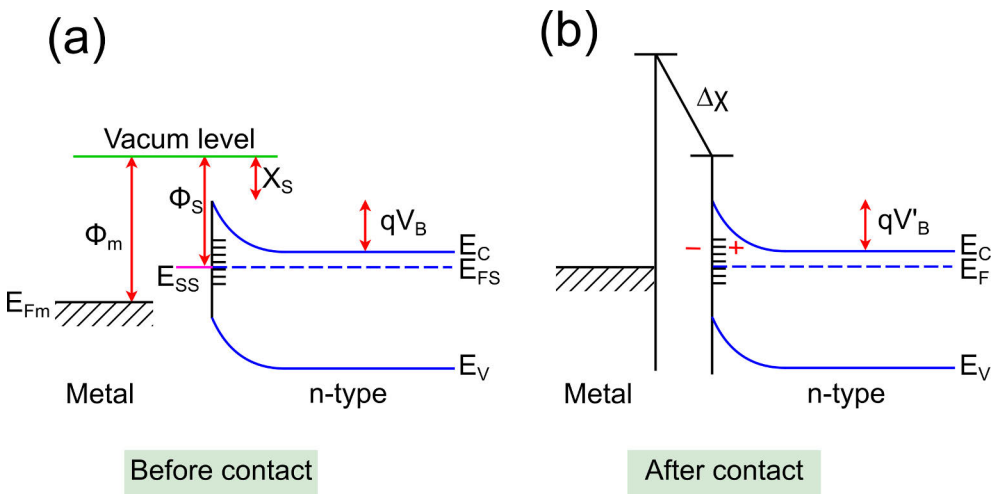

Figure 9. Schematic representation of band diagram of MSI with a high density of surface states: **(a)** prior to contact and **(b)** after contact. (ΔX is dipole potential and is E_{SS} position dependent. The dipole region is thin enough so that electrons can tunnel through it. since the contact is shown as atomically abrupt. Since the contact is shown as being atomically abrupt, the ΔX is suggested rather than plainly seen in the space between the metal and semiconductor). [42]

To this end, in the state-of-the-art research, the following solutions were investigated to increase the carrier movement and decrease the Schottky contact effect; (i) inserting of a thin insulating layer between metal and semiconductor (Figure 10a), for example, incorporation of the ultrathin TiO_2 (10 Å) in between Ti/n-

Si led to Fermi level depinning and also contact resistivity reduction at the interface. [46] Lu *et al.* found that the states induced by the dangling bonds can be shifted out of the band gap by passivation, while the passivation of the MIGS from the gap is done by incorporation of an insulating layer [47]. They demonstrated that TiO_x layer in between Ca/n-crystaline-Si decreases the recombination and resistive losses [48], and (ii) increasing the doping concentration (n- and p-type) at the semiconductor surface (Figure 10b). The contact performance of the device is determined by the density of free charge carriers, which can be controlled by doping concentration. Therefore, the increase of the surface profile doping causes the narrowing of the band bending and allows carriers to tunnel through the contact and hence decrease the contact resistivity. [49, 50, 51]

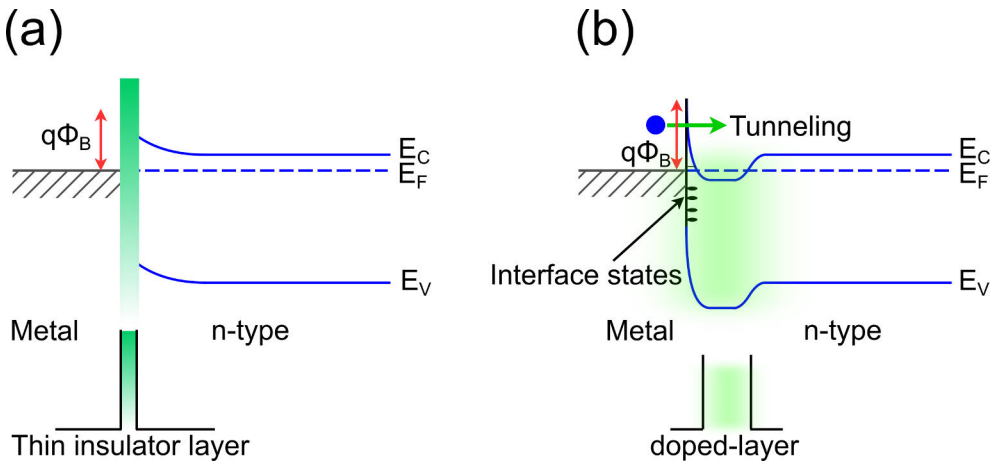

Figure 10. (a) Incorporation a thin insulator, and **(b)** Increasing doping at the semiconductor surface. The full blue circle in (b) represents electron. [52]

3.2 Oxide-Semiconductor interface (OSI)

The significance of OSI has been extensively investigated in a variety of applications, including solar cells and field effect transistors. [53, 54, 55] Because device performance is governed not only by the bulk semiconductor and oxide layer properties but also by the nature of their interface. For example, in the traditional Si-based metal-oxide-semiconductor field effect transistors (MOSFETs), SiO_2 was known as the most renowned oxide layer, which contains the lowest reported interface states (almost 1×10^9 states/eVcm^2) at SiO_2/Si interface after the optimized passivation. [56] Although SiO_2 is a naturally stable oxide for Si, it could not meet the system requirements during size scaling. Therefore, it has been replaced with high-k material such as hafnium oxide (HfO_2). [57] The change allows to use the thicker oxide layer to minimize the harmful leakage current through the oxide film,

as compared to the SiO_2 junctions, keeping the oxide capacitance high enough. Because of the structural and electronic differences between HfO_2 and Si crystal, the interfaces often include high defect densities such as vacancies and impurities, which further cause defect energy levels in the band gap, and consequently FLP. [58, 59] It is important to note that the HfO_2/Si interface still includes a thin SiO_2 layer because it is not possible to avoid Si oxidation, and also because the Si oxidation is an energetically favoured process. The target is often the intentional growth of the SiO_2 interface layer below HfO_2 to decrease the leakage current and carrier recombination.

Integrating oxide/III-V interfaces is also a challenge in achieving a high-quality oxide layer due to the exothermic nature of compound semiconductor surface oxidation. Thus, the oxygen incorporation is an energetically driven process, which occurs anyway at some stage(s) of device processing. The oxidized surfaces have often a disordered or amorphous structure because the oxides have different crystal lattices and the oxidation occurs at low temperatures, generating extra electronic states at the oxide/III-V interface, which adversely affect the interface integrity and the electrical properties of devices. [56]

Crystal orientation and surface termination affect on a high-k/III-V system. InP(111)A and InP(100), for example, are surfaces terminated with In atoms and mixed In-P atoms, respectively. This difference causes the FLP to be closer to the CBM at InP(111)A than at InP(100). The pinning difference is explained with the surface reconstruction. [60] Hence, the distribution of donor and acceptor traps below and above the pinning level inside the band gap of InP(111)A and InP(100) can predict their behavior in the n-MOSFET.

Furthermore, the chemistry of interfaces is relevant to the formation of defect states in the band gap. The nature of the defect states in the InP bandgap is being debated. Midgap states were associated with In-In dimers and P dangling bonds, whereas conduction band states were connected to P-P dimers and In dangling bonds. [61, 62, 63] In reality, an oxygen-free surface and interface are impossible to achieve. Santosh *et al.* [64] investigated the HfO_2/InP(100) interface defective states in terms of oxygen amount, and found that lower oxygen amount causes in fact higher defect density. This is consistent with our finding in publication II, in which the chemically treated InP surface has lower PL intensity, but after prolonged air exposure, PL intensity of InP increases. At high oxygen concentrations, the gap states are suggested to form by InO_x and PO_x bonding. The PO_x has been suggested to increase the interface trap density, when the In atoms are out-diffused into the oxide layer, leaving the unsaturated PO_x behind. [65, 66]

Thus, to address these challenges, one has to carefully control the oxidation process and interface engineering. To achieve this, passivation of the semiconductor prior to oxide layer growth is of great importance to reduce the number of defect states. [56] The interface defects passivation is performed by different methods (i)

incorporation of ionized doping atoms into the oxide layer (field-effect passivation). The ionized doping atoms provide static (fixed) charges to repel the carriers from those interface defects, which is advantageously observed in, for instance, Si solar cells with aluminum oxide (Al_2O_3) film, [67] (ii) applying epitaxial intermediate layer, so-called window layer (e.g., lattice-matched GaInP/GaAs) of which larger band gap causes a barrier for carriers and thus decreases the surface recombination of carriers, [68] (iii) growth of crystalline oxide layer (chemical passivation) by optimizing the bonding and chemistry at the interface, which decreases the density of interface states. For example, In_2O_3/InP crystalline interface provides a well-defined platform for the characterization of OSI properties on n-type InP. [69] (iv) H-incorporation into the dangling bonds at the interfaces is the other chemical passivation method.

3.3 Semiconductor based devices: MOSFET

We next briefly discuss the renowned electronic device, which includes both MSI and OSI, named MOSFET. [52] This device is made of three electrodes (terminals): gate, source, and drain. A thin insulating layer (oxide layer) separates the metal gate electrode from the semiconductor channel. The metal-oxide-semiconductor layer stack acts as a capacitor. The MOSFET operation is based on the principle that the electric field created by a voltage applied to the gate can modulate the presence of carriers, electrons or holes, in channel (i.e. channel resistance) between the source and drain regions. The two MOSFET types that are the foundation of contemporary digital integrated circuits are n- and p-MOSFET, depending on whether the channel is formed by electrons or holes.

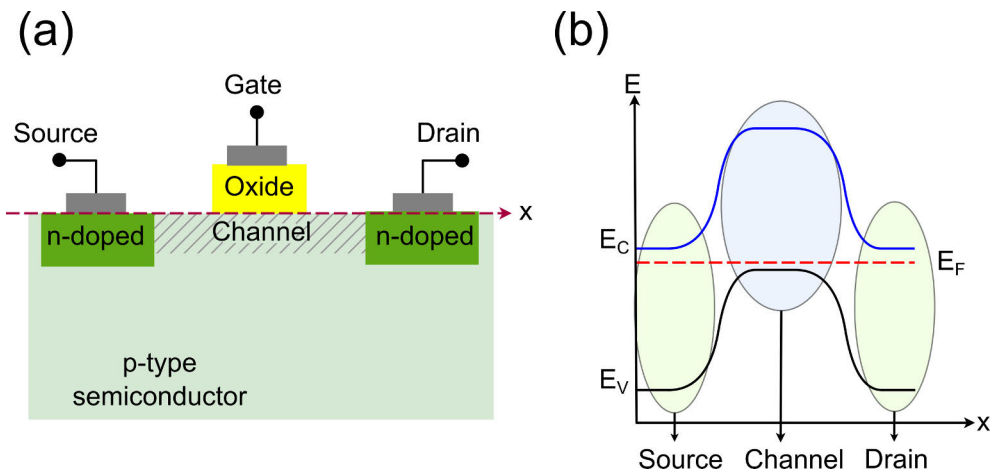

Figure 11. (a) schematic of n-MOSFET and **(b)** energy band diagram along the source to drain. [70]

To demonstrate how a MOSFET works, we will look at an n-MOSFET and its energy band diagram, which is illustrated in Figure 11a,b. The substrate is p-type and the channel is composed of electrons as current carriers. We consider an energy band diagram in the horizon direction (from the source across the channel and out the drain) in equilibrium (Figure 11b). It helps understand how current flows from the source across the channel and out the drain. Before applying a voltage to the gate, no current will flow (blue line in Figure 12). The conduction band is only considered for convenience because of the n-channel.

3.3.1 MOSFET operation

How does a gate voltage affect this energy band diagram?
As schematized in Figure 12, if a low gate voltage (positive) is applied, it increases the electrostatic potential in the channel or lowers the energy in the channel. However, there is still a large energy barrier that holds the electrons in the source and drain (magenta line). They can not flow across the device and out the terminals, and the transistor is off. When a high gate voltage is applied, the gate voltage pulls the energy bands downward in the gate area (black line), which provides the electron channel. Doing so, electrons from the source and drain can easily hop over this small energy barrier and flow into the channel.

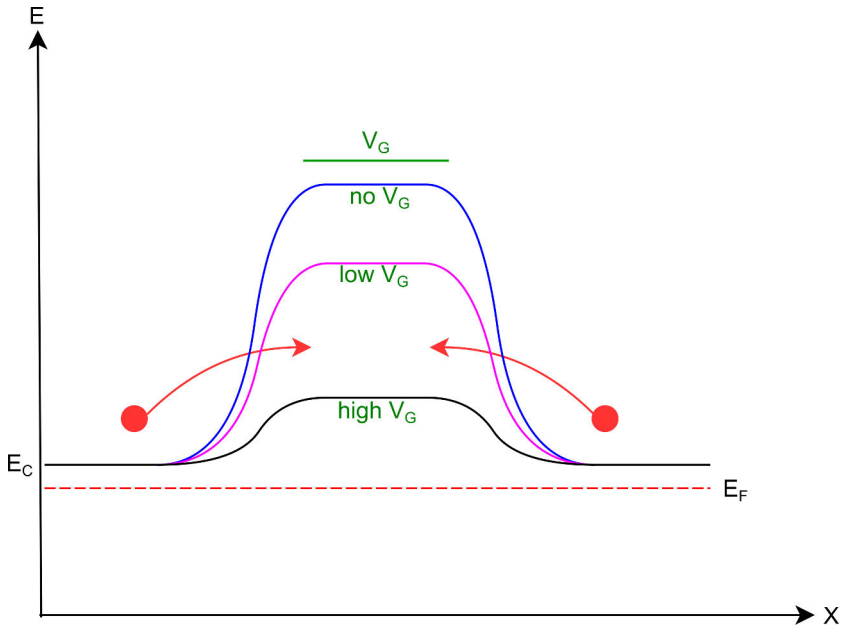

Figure 12. Effect of gate voltage (V_G) on the transistor operation. [70]

If the voltage is provided between the drain and source, but V_G is zero, there is a large energy barrier, which holds most electrons in the source and they are unable to flow out the drain. This situation is called off-state (black line, Figure 13) and one can measure the off-current. Because there is a very low probability that a few of charge carriers can hop over this very large barrier and carry current out to the drain. If a high V_G and V_D are simultaneously applied, electrons can easily hop over that barrier and just flow across the channel and out the drain causing current to flow in the inversion channel (i.e., high positive gate voltage bends the bands downward). This situation is called on-state (blue line, Figure 13). It means that it is easy for many electrons to flow from the source to the drain.

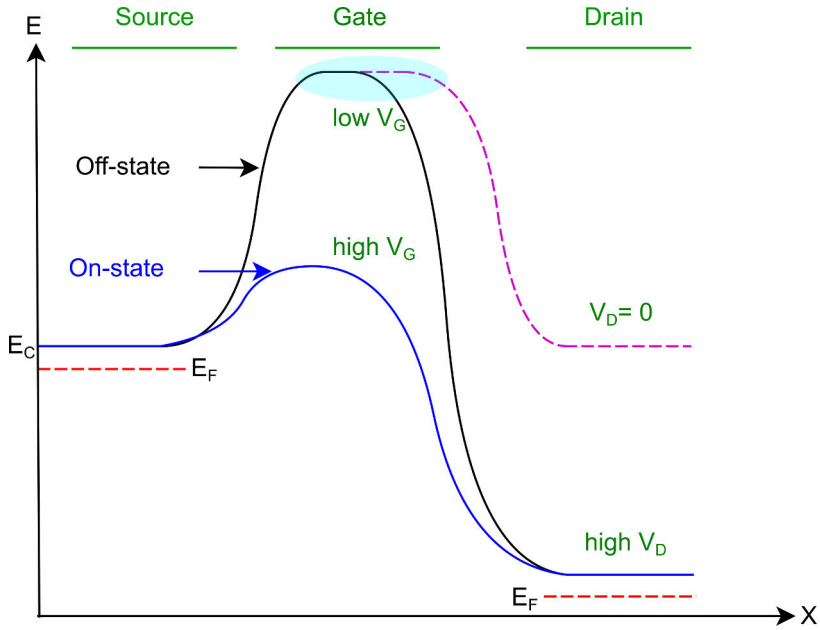

Figure 13. Schematic representation of the on- and off-state in the transistor. The gate and drain voltages are denoted by V_G and V_D, respectively. [70]

4 Experimental Methods

The characterization of clean and treated surfaces of semiconductors is very important to develop the electronic devices, and a combination of complementary surface-sensitive techniques are used for this aim because every method has own strengths and weaknesses. Surface science methods and electrical measurements complement each other in understanding semiconductor device properties. The following chapter gives description of the experimental techniques and methods employed in this study.

4.1 Ultra high vacuum (UHV)

Surface science techniques rely on highly surface sensitive measurements which provide information only from topmost atomic layers. Any contamination (atmospheric gases) on the tools or samples might affect measurement accuracy and hinder interpretations. It is essential to keep surface science instruments clean to ensure reliable and reproducible results, which can be justifiably linked to a clean semiconductor. It is essential to remember that any surface becomes quickly covered by an adsorbate layer, for example, in the air or in a poor vacuum (10^{-6} mbar and even a lower pressure). Therefore, ultrahigh vacuum (UHV) is needed to understand clean surface properties. In normal conditions, there is atmospheric pressure (1013.25 mbar) due to the presence of gas molecules such as N_2, O_2, and H_2O. When the number of molecules and/or atoms in a given space is reduced, a vacuum is created. The vacuum regime is classified into rough-, medium-, high-vacuum, and UHV ranges. UHV is defined as having a pressure of less than 1×10^{-7} mbar. In modern UHV chambers, however, background pressures can reach as low as 1×10^{-11} mbar to 1×10^{-12} mbar. [71, 72]

4.2 Surface preparation

The preparation of samples using wet chemical pre-treatment and low-temperature UHV-base surface treatments is the goal of this investigation. Depending on the substrate, the samples were first treated by a range of chemical treatments, such as Radio Corporation of America (RCA) or HCl- isopropanol (IPA) based.

The used UHV system contains two chambers: process and analysis chambers with background pressures in low 10^{-8} mbar and low 10^{-10} mbar ranges, respectively. This technology also enables a range of surface treatments (e.g., argon ion sputtering cleaning, heating, flash heating, gas exposure) to modify semiconductor surfaces. The analysis chamber includes several surface science instruments such as LEED, STM/STS, and XPS.

UHV also enables the deposition of different materials onto the substrate surface in clean and non-reactive environment. To do this, a tantalum (Ta) envelope evaporator was attached to the UHV chamber. Before any deposition, the evaporator is degassed to remove air contaminants. The relevant substance is then heated to evaporation temperature or even higher. At that time, the chamber is filled with an atomized haze. They then migrate toward the substrate surface and coat it.

ALD approach is applied for oxide layer deposition on the samples. ALD is a result of a sequence of recurrent, self-limiting chemical reactions. Each cycle involves the introduction of a precursor gas into the reaction chamber, where it reacts chemically with the substrate. The process is intended to generate a single atomic layer of the desired compound, such as HfO_2 or Al_2O_3. Each precursor pulse is followed by a chamber purge to remove any excess gases and byproducts of the reaction. The procedure is then restarted using a different precursor, and the cycle is continued until the required film thickness is reached.

4.3 Surface science techniques

4.3.1 Low-energy electron diffraction (LEED)

LEED, as a nondestructive technique, offers useful information on the surface crystal structure and reconstruction. Figure 14a schemes the layout of a LEED system consisting of an electron gun, set of grids, and a fluorescent screen. [73] The gun emits electrons (50-300 eV) along the surface normal. The sample is inserted at the center of the hemisphere. The set of hemispherical grids is concentric with the screen. Backscattered electrons from the surface move toward the sensitive screen, which has been biased with a high positive voltage. They experience also a retarding potential, present in grids, in their trajectories that causes screening of elastic and inelastic electrons. The sample is grounded to keep the sample neutralized.

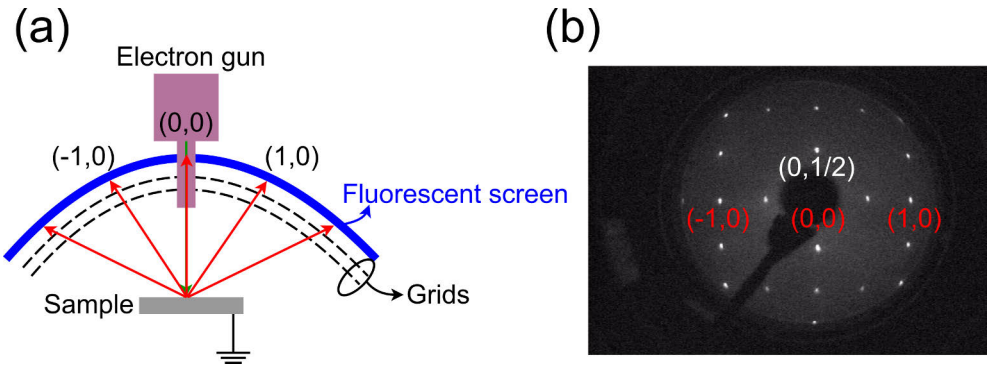

Figure 14. (a) A schematic drawing of the LEED experimental configuration [73] and **(b)** flash heated cleaned of Si(100) (2×1)+(1×2).

There is no energy difference between elastically scattered electrons at the surface and incident beams, thus the wave-vector magnitude is equal; $\|k_{in}\| = \|k_{out}\|$. The "in" and "out" indicate incoming and diffracted beams, respectively. The diffraction will happen in such a way that the Bragg condition for elastically scattered electrons is satisfied. [74] The diffraction pattern is a representation of the surface reciprocal lattice, as seen in Figure 14b, where the distance change is inverse to the real lattice change. The uppermost layers at the crystal surface explain the diffraction process. According to the de-Broglie relation, the estimated electron wavelength in the 50-300 eV range is 0.75-2.75 Å, resembling the atomic spacing on crystal surfaces. [75] LEED electrons are not expected to penetrate much into the semiconductor bulk. Small portion of electrons diffracts still back elastically toward the screen. The elastic electron mean-free path is short, typically less than 2 nm.

4.3.2 Scanning tunnelling microscopy/spectroscopy (STM/STS)

STM is capable for determining local electronic structures and providing atomic-scale resolution of surface in real space. [76, 77, 78] It takes advantage of the quantum tunnelling effect. The conventional configuration of the STM is schematized in Figure 15a. The most fundamental requirement for STM is an atomically sharp tip to achieve atomic resolution on the surface. The tip should be as close to the surface as possible (5-10 Å). Next, a bias is introduced between the sample and the tip. That is, both the tip and the sample should be conducting in nature. Then, there will be a tunnelling current that is passing between the tip and sample surface, which is strongly exponentially dependent on the distance (z) as well as the barrier height (Φ) between the tip and the sample, [79, 80] as follows:

$$I = e^{-\sqrt{\Phi}z} \tag{3}$$

This means that a small change in the distance can drastically reduce the current. STM operates in two different modes: constant-height and constant-current. The first mode, as the name implies, maintains a fixed distance between the tip and the sample surface while monitoring the tunnelling current to image the surface topography. The second mode, which is mostly used, keeps a constant tunnelling current during scanning and adjusts the height of the tip during surface scanning. To maintain a constant tunnelling current, the feedback loop controls the tip movement along the z-direction during the surface scanning (x- and y-direction) by a piezodriver. An image representing surface topography is created from the variation in the z-motion of the scanner.

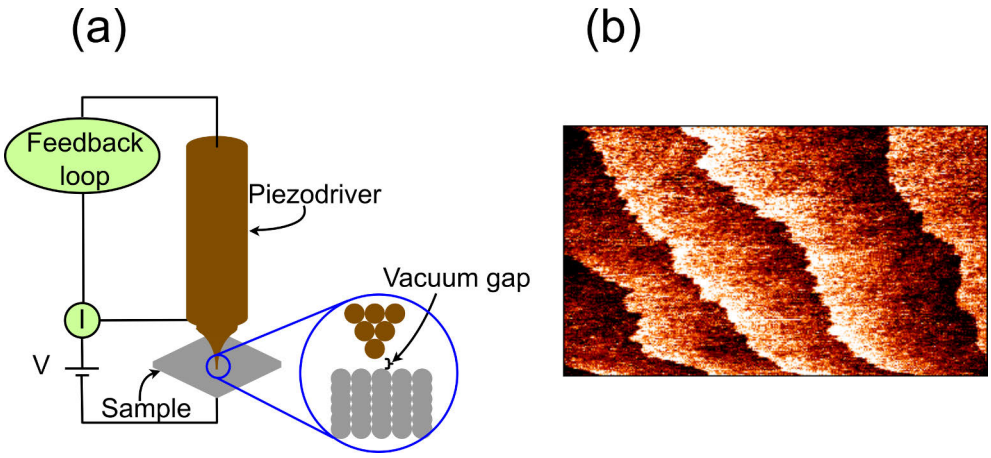

Figure 15. (a) Schematic illustration of STM setup [75] and **(b)** an STM image of Si(100) cleaned by flash heating.

As is seen in Figure 15a (zoomed in), there is a small gap (typically 0.3-1.0 nm) between the sample and tip. It indicates the presence of a potential barrier that limits the electrons to pass from the tip to the surface. One may gather information about both empty or filled electron levels at the sample surface, depending on the direction of the tunnelling current flow by varying the biased voltage. For instance, when a sample is subjected to a positive (negative) voltage, electrons can tunnel from the tip's (sample's) occupied states to the sample's (tip's) unoccupied states. [81, 82] Figure 15b depicts an STM image of a Si(100) surface that has undergone cleaning through flash heating.

STS measurements (as part of STM) can be used to determine the local electronic structure of the sample surface's band gap. The STS can display the band gap, band bending, and their changes caused by adsorbate atoms on the semiconductor surface. Typically, the tunnelling current is measured at a particular surface point while the

feedback loop is deactivated. This is done by recording the current as a function of the applied bias, which can be expressed as I(V) curves or the derivative dI/dV. In order to approximate the local density of states (LDOS) of a sample, a differential signal (dI/dV *vs.* V) is obtained through numerical analysis of the data. [75] Figure 16 illustrates an STS example with a clean Si surface bandgap before and after nitridation. [30] The Si surface band gap after flash heating cleaning is ~ 0.6 eV (see Chap. 2), but nitridation increases the surface band gap to ~ 1.4 eV. The conduction band above the gap is referred to as the positivity side of an STS curve, while the valence band below the gap is referred to as the negativity side.

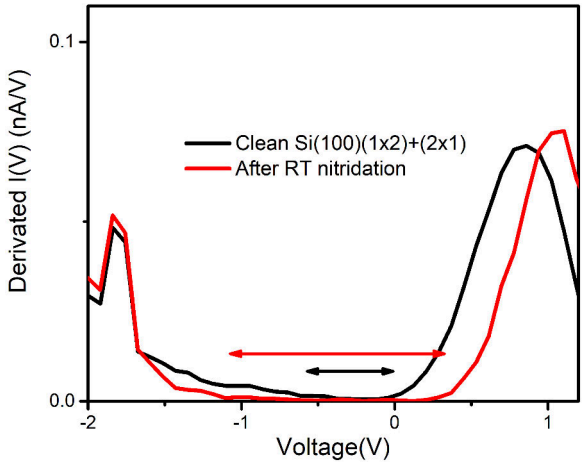

Figure 16. STS study of the surface band gap of flash-heated cleaned Si(100) before and after NH_3 nitridation. The figure was taken from I, licensed under CC BY 4.0 DEED (https://creativecommons.org/licenses/by/4.0/).

4.3.3 Photoelectron Spectroscopy (PES)

PES can be used to study surface chemical composition of surfaces. PES is based on the photoelectric effect discovered by H. Hertz in 1887. Einstein was awarded the Nobel Prize in 1905 for describing the fundamental concept of PES. [83] The photoelectric effect stands that when a photon hits a material, photogenerated electron from the material is emitted out. The equation for this process:

$$E_K = h\nu - E_B - \varphi \tag{4}$$

where hν is the photon energy, E_B is the electron binding energy relative to the Fermi level, E_K is the electron kinetic energy, and φ is the analyser work function. This only occurs when the photon energy of the radiation is higher than the binding energy of the electrons. Otherwise, it is impossible to remove the electron from the binding state to the free state (i.e., free electron in the vacuum). The remaining energy from

the radiation is transformed to the kinetic energy of the photoelectron emitted from the surface. The electron energy analyser can be used to measure the kinetic energy of the electron and determine the binding energy of the emitted electrons. PES consists of different types [84]: XPS and ultraviolet photoelectron spectroscopy (UPS). The differences between these PES methods arise from the varying energy ranges of the photons used in each method. The range of photon energies used in UPS is between 3-50 eV and this technique is beneficial in examining the structure of the valence band in materials. It enables the determination of the energy levels and density of electrons in the outermost atomic shell. On the other hand, XPS photon energy range is typically 100-1500 eV. For core level electrons or the inner shell electrons, high energy radiation is needed, afforded by X-rays. In commercial instruments, two types of X-rays are very common. They are magnesium kα (Mg-kα) and aluminium kα (Al-kα). The energies of Al-Kα and Mg-Kα are 1486.6 eV and 1253.6 eV, respectively. [74] One more source of photon is synchrotron radiation (SR-PES), which takes advantage of tunability of photon energy over a wide range of energies.

X-rays can penetrate into solids up to several micrometres. [85] However, electrons' mean free path is much smaller; electrons readily experience inelastic scattering in solids. Therefore, the signal is dominated by photoelectrons from the surface layers, (typically less than 10 nm), while the remaining electrons lose energy (phonon collision, plasmon excitations) and contribute to background signals. Thus, XPS is a remarkably surface-sensitive tool.

Core level spectra obtained from crystalline samples that have well-ordered surfaces exhibit a well-defined line shape. If a surface is amorphous, the XPS peaks are broadened. Core-level binding energies can undergo shifts in energy due to physical and chemical phenomena, resulting in a change in line shape or even a separate peak. The shifts of binding energy and peak position can be caused by either charge redistribution of the valence electrons in the chemical bonds due to presence of contamination, native oxides, adsorption of other elements, and structural changes (i.e., processes in the initial state) or by changes in the final-state screening of core hole (i.e., how other electrons screen the core hole). Therefore, a core-level spectrum can then be examined by determining such shifts (i.e., spectral components) in the peak area using the spectral fitting process. The fitting procedure deals with some parameters such as the background of the signals, the broadening of the peaks, spin-orbit splitting, and branching ratio, which are known and can be fixed in the spectral fitting. A crystal and its surface are characterized using these properties to provide chemical and structural information.

4.3.4 Photoluminescence (PL)

PL is known as an *ex-situ* and contactless optical method to examine the surface quality. [86, 87, 88] Although it has traditionally been employed to study the bulk-like properties of crystals, it is also useful for studying surfaces and interfaces. In this method, when light with an energy greater than the band gap energy strikes the material, electron-hole pairs are generated. [87] They can move from ground state to excited states and stay there for a relatively long time (10^{-9}-10^{-3} s) prior to recombination (returning to the ground state).

High-quality semiconductor crystals allow for the diffusion of electrons and holes in the range of several micrometres. The long diffusion length of carriers before the recombination means that carriers can reach the surface areas. That is the key here to understanding how PL can be used in surface studies. If the surface is of bad quality, carriers recombine at surfaces in a non-radiative manner via defect levels in the gap, decreasing the output PL intensity. Lower defect state density results in a higher PL intensity and a decrease in non-radiative recombination, while higher defect state density results in a lower PL intensity and an increase in non-radiative recombination, as seen in Figure 17. Direct bandgap materials are better suited to PL than indirect ones. Since indirect bandgap materials require additional excitation of phonons and their momentum relaxation for radiative recombination to occur.

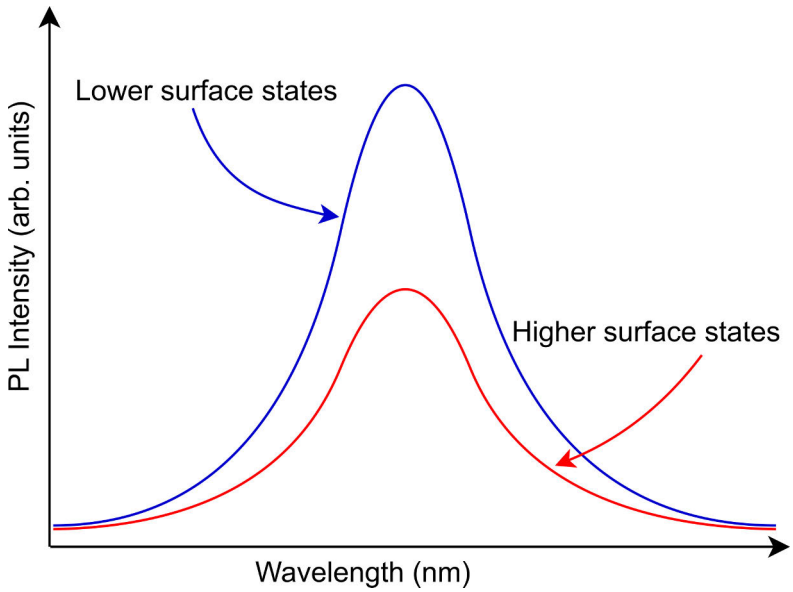

Figure 17. Schematic representation of PL spectra with high and low surface states.

4.4 Electrical measurements

4.4.1 Capacitance-Voltage (CV)

In metal-oxide-semiconductor (MOS)-based devices, CV measurements are used to optimize the interface design and performance. MOS capacitor consists of a semiconductor substrate separated by a thin oxide layer from a metal gate electrode. [41, 89] By applying voltage to the gate in relation to a semiconductor contact, an electric field is created that affects the charge distribution on the semiconductor substrate. Therefore, the intent of CV measurement is to determine the capacitance of the MOS as a function of the voltage across the gate. It can provide information about the defect densities in the band gap, doping concentration of the semiconductor, and also oxide thickness.

In this method, a combination of direct current (DC) and a low alternating current (AC) voltage is applied to the gate. The change in capacitance is measured as a function of DC voltage and a frequency of AC. According to the applied DC voltage to gate, there are three various operation modes in CV measurements including accumulation, depletion, and inversion region. Consider an n-type semiconductor in which the electrons and holes are the majority and minority carriers, respectively. As schematized in Figure 18, when a positive voltage is applied to the gate in n-MOS, the majority carriers (electrons) move from the bulk of semiconductor to be accumulated at the OSI, and holes are pushed away from the interface due to repelling. This step is called accumulation and the total capacitance represents the oxide capacitance (C_{ox}). With altering the positive voltage toward the negative sign, a depletion region is formed, meaning that number of electrons are pushed away from the interface. The total capacitance decreases due to the series connection of the oxide and semiconductor depletion-region capacitance. As the negative voltage increases, two different phenomena might happen depending upon the AC applied voltage: (i) low frequency (*lf*) and (ii) high frequency (*hf*).

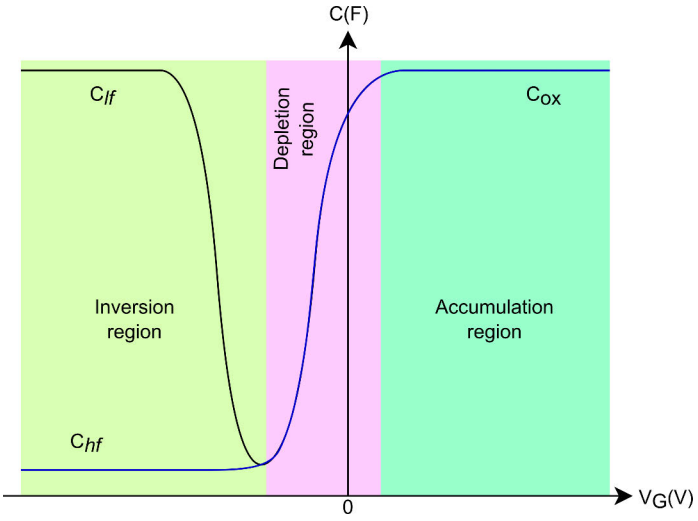

Figure 18. An n-MOS CV plot displaying capacitance response curves for *lf* and *hf* AC-signal frequencies. [41]

The minority carrier (holes) takes some time (order of microseconds) to be generated, travel toward the OSI, and then recombine back to the substrate. The inversion layer at the interface is generated when the frequency of the AC signal is lower than the generation-recombination time (GRT) related oscillation. In this case, the total capacitance is equal to the C_{ox}. When the frequency of the AC signal in *hf* is higher than the GRT phenomenon, the depletion region capacitance dominates keeping the capacitance at a minimum. The p-type semiconductor acts inversely.

Interface defect states can affect the properties of OSI by introducing additional capacitance components. Based on the applied AC voltages, these states can be either filled or emptied. [41] They do not contribute to the *hf* measurement and their effects appear in the *lf* signal, causing often a peak or shoulder in the depletion-region capacitance step. Interface defects cause the CV curve to stretch out across the voltage axis, as shown in Figure 19a. This stretching also appears at the *hf*-AC signal due to slow change in the DC voltage. In other words, the interface defect levels become filled and empty as a function of slow DC voltage causing stretching out (i.e., decrease in the slope of the depletion region step).

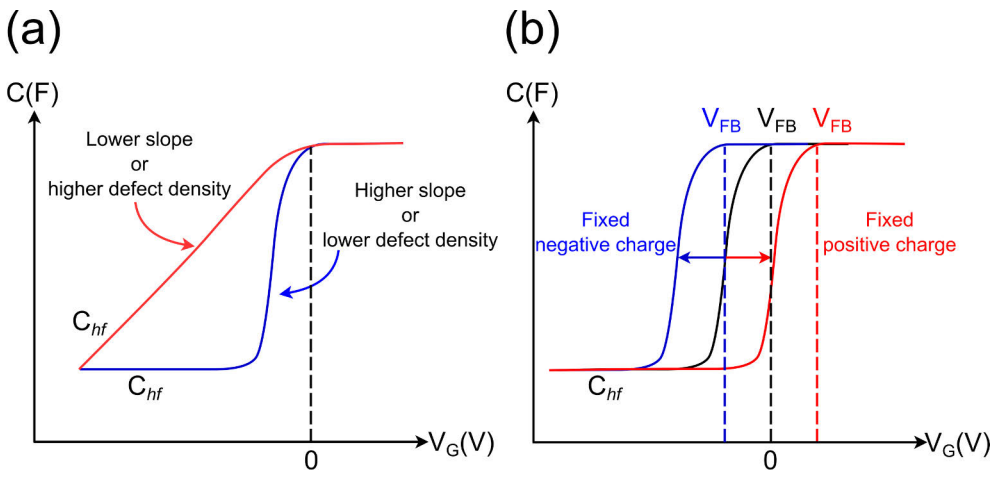

Figure 19. The CV graphs of an n-MOS **(a)** show the influence of interface trap densities at *hf* and *lf* and **(b)** shows the effect of fixed charges (positive and negative) at the interface, which causes the ideal CV to change. [52]

Using CV measurements, it is possible to determine the flat-band voltage of a semiconductor, where the semiconductor bands are not bent but are fully horizontal as a function of the distance. The flat-band voltage is often defined as the voltage where the capacitance value has decreased to half in the depletion region. [41] The flat band voltage can alter due to the formation of the fixed oxide charges and change the properties of the MOS structure as seen in the Figure 19b.

4.4.2 Specific contact resistivity (ρ_C)

To evaluate the ρ_C of MSI, two different methods, named (i) transfer length method (TLM) and (ii) circular TLM (c-TLM) are commonly used. In this work, the traditional TLM method has been applied. [41] Figure 20 illustrates the TLM, a ladder-like structure (length L and width W), which contacts spaced at varying distances.

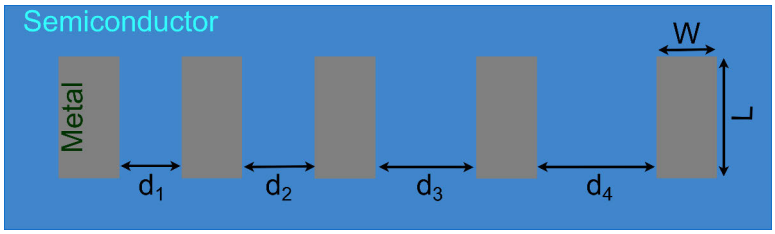

Figure 20. Top-view of TLM structure. [41]

An IV measurement is performed on adjacent contacts. The slope of the IV curves can then be used to calculate resistance. Finally, the total resistance as a function of distance (d) between any two contacts is plotted, as seen in Figure 21.

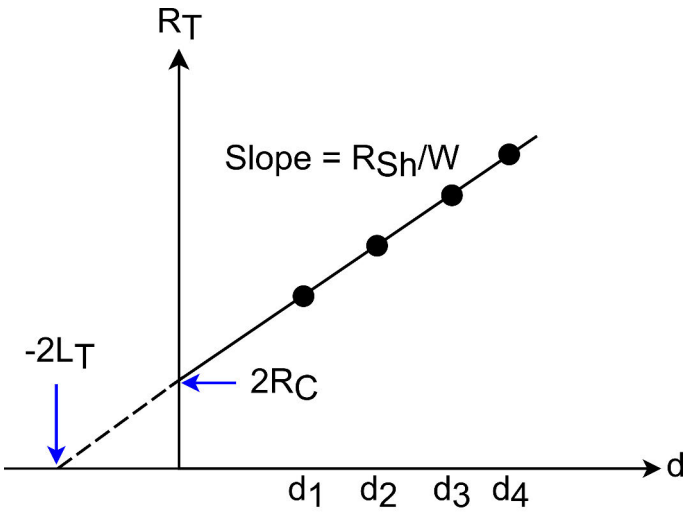

Figure 21. Plot to extract contact resstance and transfer length from the TLM method. [41]

The y-axis and x-axis intercepts give values of $2R_C$ and $-2L_T$, respectively, where R_C and L_T are the contact resistance and the typical contact length. The ρ_C is determined, as a process:

$$\rho_C = R_C W L_T \tag{5}$$

where W is the width of the metal contacts. The total resistance (R_T) is also extracted from the same plot, as follows:

$$R_T = R_C + \left(\frac{R_{sh}}{W}\right) \mathrm{d} \tag{6}$$

where R_{Sh} is the sheet resistance that is calculated from the slope of the linear fitting, as shown in the plot.

5 Summary of Results

This chapter presents an overview of the findings from this PhD work in the area materials science and engineering. On the basis of the introduction material in chapters 2, 3, and 4, interpretations made in each article are summarized next.

5.1 Effects of thermal vacuum nitridation of Si(100) surface via NH_3 exposure (Paper I)

To develop low power applications and to increase devices durability, the passivation of oxide/Si interfaces becomes even more relevant for the semiconductor industry in future. The high temperature oxidations (> 700 °C) have traditionally provided excellent passivation of Si device interfaces when combined with a proper post hydrogen annealing. The low temperature (LT < 450 °C) passivation methods, however, are also needed to reduce the interface defect densities, for example in the back-end-of-line processing steps. The effects of NH_3 nitridation on three different Si surfaces in the UHV chamber were examined in this paper: (i) nitridation of Si(100) cleaned by flash heating, (ii) nitridation of Si(100) cleaned by RCA+HF dip, and (iii) nitridation of Si(100) which includes the chemical oxide after the RCA treatment. We show that nitrogen incorporation is possible at LT without a plasma source.

5.1.1 Nitridation of Si(100) cleaned by flash heating

In this section, the nitridation effect (NH_3 of 5×10^{-3} Pa for 30 min) were studied using LEED, STM, STS, and XPS. The nitridation was done at (i) RT and (ii) 400 °C. The starting surface displayed a well-defined Si(100) (2×1)+(1×2) structure prior to nitridation, which is important to resolve the nitridation-induced effects. The results indicated that the surface properties changed due to the incorporation of the N atoms (confirmed by the XPS signal of N 1s) into the Si surface. STM showed the formation of the small islands on the terrace-step structure of a cleaned Si(100). STS confirmed that the band gap (from ~0.6 eV to ~1.4 eV) of the Si surface was modified by RT nitridation. As illustrated in Figure 22, the surface properties were also altered by the nitridation at 400 °C, with the surface bandgap increasing to 4.5 eV, the

surface lattice periodicity changing to a weak (2×1)+(1×2) pattern, and the XPS signal of the Si 2p region showing the formation of Si-N and Si-O-N.

Next, the nitridation was combined with wet chemically cleaned Si(100) surfaces to investigate its impact on electrical measurements such that the whole process was carried out at the LT.

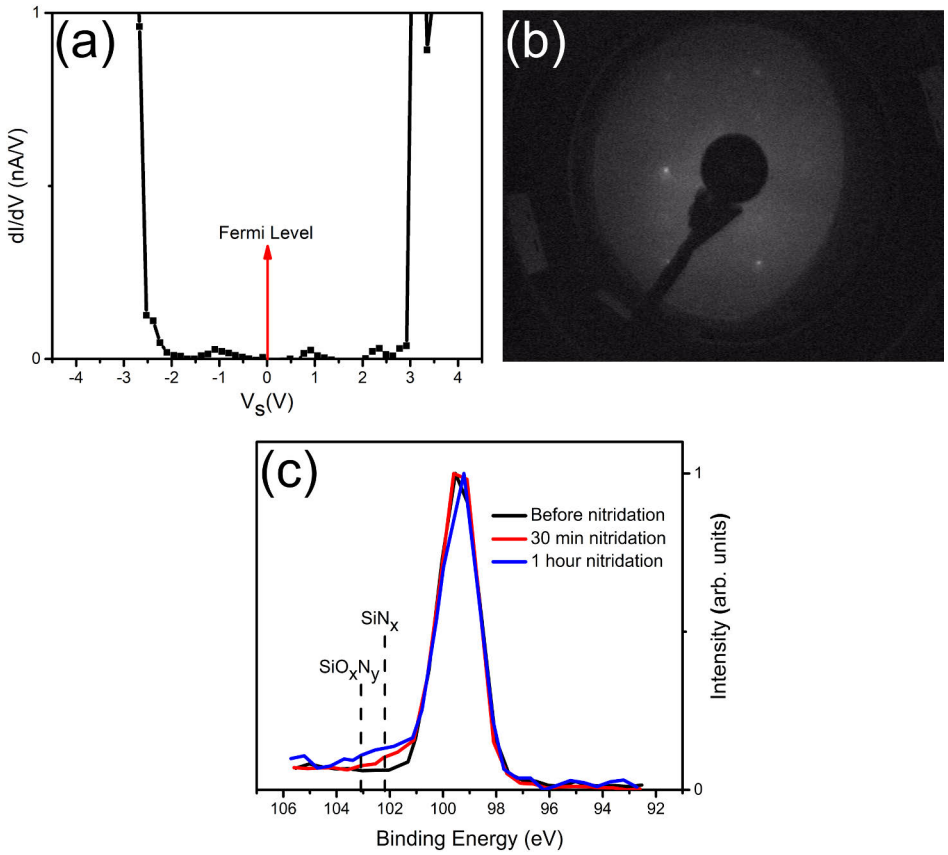

Figure 22. Surface-science measurements after nitridation: **(a)** STS indicates a surface band gap of around 4.5 eV, **(b)** LEED shows still a weak (2×1)+(1×2) pattern, and **(c)** XPS measurement of Si 2p, which have been normalized. The figure was taken from I, licensed under CC BY 4.0 DEED (https://creativecommons.org/licenses/by/4.0/).

5.1.2 Nitridation of Si(100) cleaned by RCA+HF dip

The electrical characteristics of the HfO_2/Si interfaces were studied using CV measurements. Three chemically cleaned Si(100) samples were prepared before HfO_2 layer deposition as follows: (i) reference without nitridation (Figure 23a), (ii) nitridation at 400 °C (Figure 23b), and (iii) nitridation at RT (Figure 23c). The MOS capacitors showed an accumulation capacitance dispersion, which indicated the

formation of the border traps deeper in the oxide side. [90, 91, 92] Inversion capacitance of the sample without and with nitridation at 400 °C was increased and became saturated indicating of formation of the fixed-negative charges at both interfaces. [93] In contrast, at RT nitridation the inversion capacitance did not increase, but the C step shifted toward the positive bias. Such a shift can be due to the presence of interface dipole, trap levels, and fixed negative charges, but the reason remains unclear.

Nitridation enhanced the depletion region's slope, which was quantified as the peak value of the differentiated CV curves at 1 MHz. It is 136 pF/V for the sample without nitridation, and 165 and 197 pF/V for RT and 400 °C nitridation, respectively. [94, 95] The slope increase indicates that the interface defect density decreases due to the nitridation. In consistency, a reduction in leakage current was also observed after nitridation, where the leakage current (at +2 V) was 8.8×10^{-9} A/cm^2 before nitridation, but was 6.5×10^{-9} A/cm^2 after nitridation.

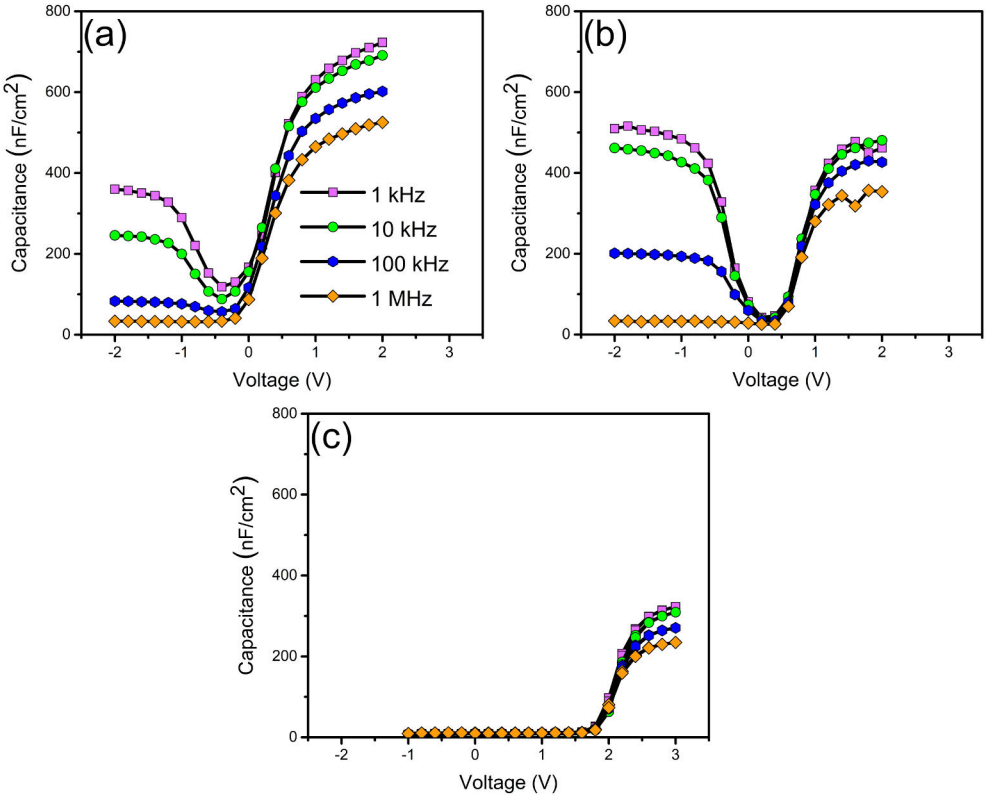

Figure 23. Capacitor measurements for metal (Au/Cr) / HfO_2 / Si(100) cleaned by RCA + HF dip: **(a)** without nitridation, **(b)** nitridation at 400 °C before ALD, and **(c)** nitridation at RT. The figure was taken from I, licensed under CC BY 4.0 DEED (https://creativecommons.org/licenses/by/4.0/).

5.1.3 Nitridation of chemically oxidized Si(100)

We have also studied how the nitridation affects the properties of intentionally oxidized Si surfaces: RCA without the final HF dip, since avoiding the oxidation of Si surfaces during manufacture is difficult. In fact, the RCA chemical oxide has been increasingly used because it enables the LT fabrication of SiO_2 intermediate layer at the Si device interfaces.

Nitridation of the RCA-chemical oxide covered Si(100) was carried out at 400 °C for 30 or 60 min. As seen in Figure 24a, N 1s XPS signal indicated the formation of the Si-N and Si-O-N bonds, and STS analysis (Figure 24b) supported that during nitridation, the donor-type level was introduced above the Fermi level near the conduction band, consistent with Lee *et al.*'s findings. [96] The Si 2p signal also showed the surface modification caused by the incorporation of N atoms at the SiO_2/Si interface.

There was no LEED pattern for the surface structure of oxidized Si(100) with and without nitridation. Nitridation can lower the number of fixed negative charges in SiO_2, particularly when done for 60 minutes, as well as the accumulated capacitance dispersion. The shifting of the C step to positive voltage can arise from the interface dipole and/or trap levels. Moreover, the nitridation decreased the leakage current. Thus, the nitridation is a potential method for the LT passivation tool arsenal for Si device interfaces.

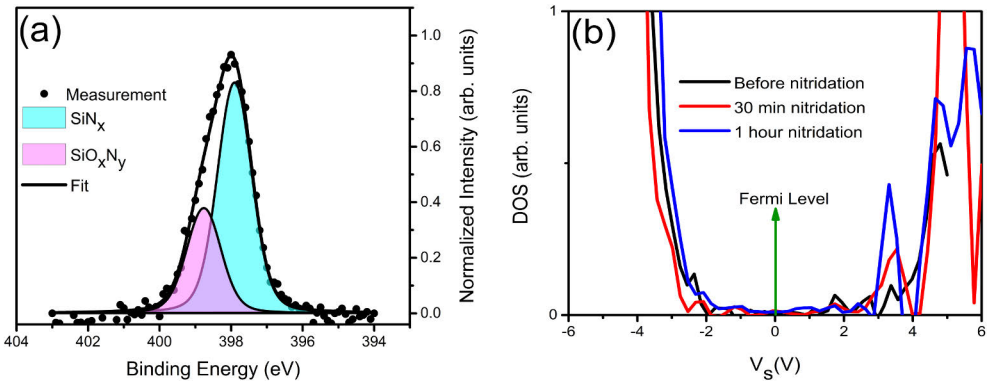

Figure 24. (a) N 1s XPS measurement of Si(100) after 1h nitridation and **(b)** STS curves show the generation of N-induced levels after nitridation. The figure was taken from I, licensed under CC BY 4.0 DEED (https://creativecommons.org/licenses/by/4.0/).

5.2 Properties and modification of native oxides of InP(100) (Paper II)

This paper involves the modification of the InP native oxide. InP crystals with native oxides provide an interesting platform because this material system has been previously found to cause less surface-induced degradation, as compared to many other semiconductor crystals covered by their native oxides. The reason(s) for the specific properties of the oxidized InP has remained unsolved. Likewise, the question of what kind of methods enable to modify the native oxide properties further, instead of trying to avoid the oxide formation, is still open. Such knowledge is relevant not only to the development of InP-based applications but also to understanding how other III-V native oxides could be modified to mimic the less harmful InP oxide case.

In this work, we clarified the above issues by characterizing different native oxides of both n- and p-types InP(100). The reference samples were InP pieces with the native oxides without any additional treatment. Some InP samples were exposed to NH_3 gas (or O_2 gas) in the UHV system. Before the NH_3 exposure (or O_2 exposure), the native oxides were not removed from InP (i.e., no pre-treatment). The pressure of NH_3 gas (or O_2 gas) was approximately 1×10^{-5} mbar. Separate n-InP sample was cleaned by a standard wet chemistry with HCl:IPA (1:3) for 3 min followed by 1 min IPA, and dried with N_2. This pre-cleaned n-InP piece was used to study the effect of air exposure.

The PL results of the chemically cleaned n-InP samples (Figure 25a) demonstrate that as the air exposure time increases, the PL intensity increases. It can be attributed to two factors, as schematically shown in the inset image in Figure 25a. First, partial oxidation of the P atoms results in a local nonstoichiometric $InPO_x$ that generates the band gap level (at the beginning of air exposure), while complete oxidation of InP has lower defect densities (longer air exposure). [97] Second, the effect of band bending, which causes the majority carrier to repel from the defect-rich surface as the upward band bending increases. According to the PL results, the nitridation (250 °C) of n-InP and oxidation of the p-InP (300 °C) improve further the native-oxide covered InP by decreasing the harmful non-radiative surface recombination.

InP native oxides were not removed by the LT treatment, but rather modified. The STS results indicated that the upward (downward) band bending occurred at the n-InP (p-InP) native oxides, after nitridation (oxidation). The band bending is an inherent property of native-oxide-covered n-InP and p-InP. Figure 25b illustrates the band bending at the n-InP. As shown, the Fermi level is around the midgap before and after nitridation, which does not reflect a flat-band situation for n-InP where the Fermi level is expected to be near the conduction band. As a result, such a Fermi level midgap position represents an upward band bending, which is compatible with the PL results.

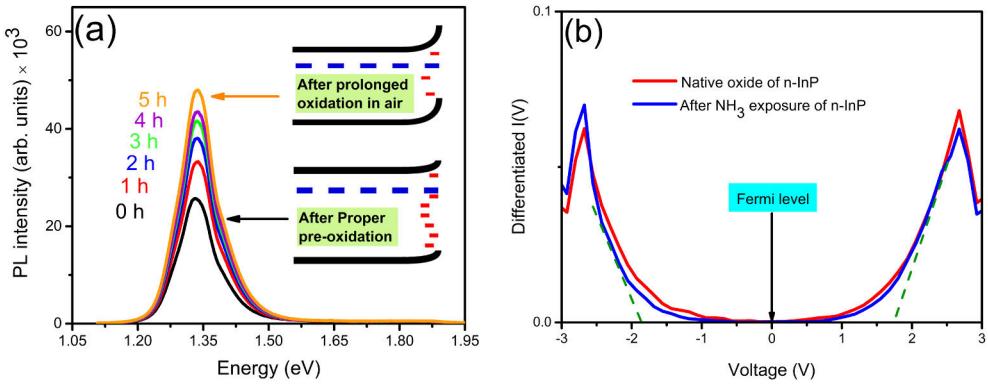

Figure 25. (a) PL measurements as a function of air-exposure of cleaned n-InP; the inset suggests the surface band behavior and defect density formation (blue-dashed and red lines represent the Fermi level and defect levels in the band gap) and **(b)** Differentiated STS I(V) curves before and after nitridation demonstrate that the Fermi level locates in the midgap. Reproduced from II with permission from the IOP publishing.

Leakage current measurements are in agreement with the PL results, indicating that the nitridated n-InP (oxidized p-InP) reduces the leakage current through the native oxide layer. This suggests that the nitridation is able to decrease the point defect densities. LEED and STM measurements support the previous findings in that the InP native oxide has an exceptional tendency to local crystallization. XPS analysis shows that LT NH_3 exposure without a plasma source enables N atom incorporation into the $InPO_4$/InP material.

5.3 Wet Chemical Treatment and Mg Doping of p-InP Surfaces for Ohmic Low-Resistive Metal Contacts (Paper III)

In the current industry, InP crystals are used in two main application areas: (i) infrared light emitters and detectors; (ii) colloidal quantum dot QLED television. The common challenge with these devices arises from surface areas of InP which form one of the most defect-rich part of the functional semiconductor material, although quality of InP surfaces has been found to be higher than for many other semiconductors. Defective InP surfaces and semiconductor surfaces in more general cause electrical and optical losses as well as malfunctions in the devices, also in future. Therefore, the InP surface cleaning and passivation have been intensively investigated. The experimental and theoretical results presented in this article contribute to solving the InP surface challenges, in particular, from the perspective of making low-resistive Ohmic contact for p-type InP. In most devices, a high-quality MSI is needed to transmit the electrical carriers into a semiconductor crystal with minimized losses.

We demonstrate a low-temperature (< 350 °C) method to engineer the surface properties of p-InP for decreasing the contact resistivity of Ni/p-InP contacts. Low processing temperatures are preferred for several reasons: to avoid degradation of InP crystal quality, to allow the back-end-of-line processing of devices, and to decrease the energy consumption in manufacturing. Furthermore, nickel (Ni) is also a proper metal for large-scale Si processing lines.

We have combined benefits of the wet chemistry and UHV technology to modify InP surface properties. The wet chemical treatment(s) is undoubtedly the most used method to clean and passivate semiconductor surfaces in both industry and academia because the method is simple and scalable.

In the beginning, we optimized an HCl-based wet chemically treatment for the p-InP surface using surface-sensitive measurements and found a very surprising property for InP which has not been reported earlier for chemically cleaned III-V semiconductor surfaces. Namely, a properly etched p-InP surface has a long-range ordered c(2×2) reconstruction (observed by LEED) directly without any post treatment like heating. STM displays that the surface contains smooth two-dimensional terraces indicating crystallinity. STS implies that no band bending occurs due to the existence of the Fermi level near the VB. This wet-chemistry induced InP(100)c(2×2) surface provides a high-quality reference contact of Ni/p-InP.

The UHV environment is then used in this work to modify the surface doping of p-InP with magnesium (Mg). The Mg layer (different in thickness) was incorporated on the surface using thermal annealing of Mg metal enveloped with tantalum. The envelope was normal to the InP surface. An obvious benefit of UHV is a very clean environment where the chemical environment of semiconductor surfaces can be controlled. Then Ni was deposited on the p-InP surfaces without and with Mg. Before the post heating, Ni/p-InP samples with low-temperature Mg-surface doping displayed a significantly lower contact resistivity than the lowest reference value without Mg (from 1.4×10^{-3} Ωcm^2 → 1.2×10^{-4} Ωcm^2). Some samples were heated in O_2 background, and then the Ni was deposited. The ρ_C before and after post heating was 2.9×10^{-5} Ωcm^2 and 4.4×10^{-6} Ωcm^2, respectively, the lowest values reported in this work. The Mg layer thickness was 4 nm. The TLM method was utilized to determine the ρ_C.

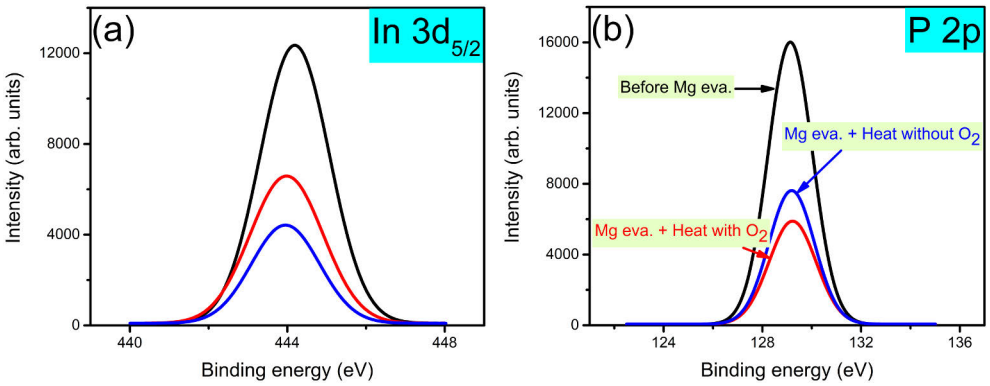

Figure 26. Effect of O_2 gas during heating of Mg(4 nm)/p-InP (350 ℃ for 60 min): **(a)** In 3d with and without O_2 gas and **(b)** P 2p with and without O_2 gas. Figure adapted from III with permission from John Wiley & Sons, Inc.

The XPS depth profile measurements show the inter-diffusion (or alloying) of Mg and InP elements in a controlled O_2 background (1×10^{-6} mbar) in the UHV chamber. In Figure 26a,b, the XPS results demonstrate that when O_2 gas is not present, In and P atoms diffuse out equally, whereas when O_2 is present, the In atoms diffuse out more than the P atoms. It provides more lattice sites for Mg atoms at InP surface and then decreases the contact resistivity of Ni/p-InP. The quantum mechanical simulations clarify the diffusion properties of the metal and InP elements at the interface and allow us to discuss possible mechanisms behind the decreased contact resistivity. There is an increase in In outdiffusion when the InP native oxide (interfacial $InPO_4$) and metal-indium alloys (In_xNi_y phases) are present, while the pure Ni, NiO, and MgO phases promote P outdiffusion. To describe the performance of metal/semiconductor contacts, surface recombination of the electric carriers is also important (see chap. 3). PL measurements revealed that Mg surface doping does not significantly enhance the surface recombination.

6 Conclusion

In this thesis, surface science techniques and electrical measurements complement each other to characterize OSI and MSI. The main purpose has been to develop the low-temperature methods to improve the interface properties, which are a weak part of many current and future devices. A variety of the preparation parameters was investigated in an iterative manner, including wet chemical cleaning, heating temperature in ultrahigh vacuum chamber, gas content and pressure, surface doping, and post-annealing temperature.

The nitridation of different chemically pre-cleaned Si(100) surfaces, which have either H-termination (due to the final HF dip) or oxidized topmost surface (i.e., without the final HF dip) have been investigated. The results indicated the incorporation of the N atoms at the surface or subsurface and the formation of the SiN_x and SiO_xN_y bonding, although low-temperature NH_3 exposure was used without a plasma source. The nitridation generates extra levels above the Fermi level in the SiO_2 layer side. The nitridation is, however, found to decrease the interface defect density qualitatively at HfO_2/Si(100) because the depletion region capacitance slope increases and the leakage current decreases.

The harmful impact of native oxides of III-V compound semiconductors has been a remained a long-standing challenge in technology. The InP native oxides are, however, known to be an exception because they cause less photoelectric losses. In the second article of this thesis, the characterization and modification of the InP native oxides, exposed to NH_3 or O_2 gas exposures, have been presented. Without removing the InP oxides, the PL of native-oxide covered InP crystals native-oxide-containing InP can be further improved by appropriate low-temperature gas exposure. According to the PL results, the nitridation (250 °C) of n-InP and oxidation of the p-InP (300 °C) improved further the native-oxide covered InP by decreasing the harmful non-radiative surface recombination. Surface-sensitive measurements support that an exceptional crystallization tendency of native InP oxide interface occurs.

The third article presents surface engineering of p-InP incorporating Mg atoms as a dopant to minimize the contact resistivity ρ_C. The surprising crystalline p-InP(100)c(2×2) surface was found via a mere wet chemical treatment based on HCl.

To our best knowledge, p-InP(100)c(2×2) is the first III-V reconstruction that is formed with a wet chemical immersion without any post-treatment. It provided a high-quality reference contact of Ni/p-InP, which was managed to decrease still by a factor of 10 via proper Mg surface doping.

As a final statement, the results of this PhD thesis support that bridging the semiconductor technology and surface science is useful to develop the different semiconductor interfaces for improved devices. Atomic-scale understanding and modification of semiconductor interfaces become increasingly important to the technology when the device size decreases, and devices' efficiency and durability are increased. Future work is needed to test the presented results in industrial device operation.

Acknowledgements

The thesis was completed in the Material Physics Group (MPG) of the Department of Physics and Astronomy at the University of Turku (UTU) between 2020 and 2024 under the Doctoral Programme in Exact Sciences (EXACTUS).

I would like to thank many people for their help during my PhD studies. Every single one of your contributions has been quite helpful to me. Please accept my apologies if you are not acknowledged here.

It is with great gratitude that I express my sincere thank to my supervisor Docent Pekka Laukkanen for his guidance, encouragement, and expertise. My study has been shaped and refined by his insightful feedback and continuous support.

I would like to extend my heartfelt gratitude to Professor Kalevi Kokko, the director of this work as the head of the group. The support he provided was always available whenever I needed it. This experience was fantastic with his encouragement and assistance.

Doctors Risto Punkkinen, Marko Punkkinen, Mikhail Kuzmin, and Sari Granroth deserve particular appreciation. Their tremendous support and generosity in managing all of the paperwork associated with the PhD studies have been enormously beneficial.

It is my delight to work with MPG members. Special thanks to Zahra (Elmira) Sadat Jahanshah Rad, Juha-Pekka Lehtiö, Esa Vuorinen, Mikko Miettinen, Doctor Antti Lahti, and Mikael Santonen for their contributions and camaraderie. This work has been made possible by their warm and friendly demeanor, along with their invaluable peer support.

All of you, from the Wihuri Physical Laboratory (Professor Petrina Paturi, Doctor Ilari Angervo) to the Intelligent Materials Chemistry Research Group (Professor Mikka Lastusari, Doctor Sami Vuori) and Microelectronic laboratory in ICT city (Tatu Peltola), from Finland to Sweden (Personnel at MAX-lab, Lund University), and EVEN Iran are greatly appreciated. It was a privilege for me to work with you.

In the course of my PhD studies at the University of Turku, I was lucky enough to meet an incredible group of friends who made my journey truly memorable at UTU. I am grateful to Shima Asjadiyan, Mahsa Shhsavan, Abdollah Noorizadeh, Li

Qing, Naman Naushahi, Moe Aye, Maryam Esmaeilzadeh, Vahid Abbasi, and Arman Hasani. Your presence and encouragement have been a constant source of inspiration and joy.

To the Materials Research Laboratory, University of Turku, Academy of Finland, I would like to express my sincere thanks for their priceless financial support during my studies.

" The invaluable support of my family made this entire journey possible." I would like to thank my parents and sister, whose unwavering support and belief in me have been the driving force behind my endeavors. You are all.

23.12.2023

Masoud Ebrahimzadeh

List of References

[1] Bondyopadhyay, Probir K. "Moore's law governs the silicon revolution." Proceedings of the IEEE 86.1 (1998): 78-81.

[2] Charles Jr, Harry K. "Miniaturized electronics." Johns Hopkins APL technical digest 26.4 (2005): 402-413.

[3] Wilmsen, Carl, ed. Physics and chemistry of III-V compound semiconductor interfaces. Springer Science & Business Media, 2013.

[4] Hasegawa, H., and M. Akazawa. "Interface models and processing technologies for surface passivation and interface control in III-V semiconductor nanoelectronics." Applied Surface Science 254.24 (2008): 8005-8015.

[5] Del Alamo, Jesús A. "Nanometre-scale electronics with III-V compound semiconductors." Nature 479.7373 (2011): 317-323.

[6] XCai, Xiangbin, et al. "Bridging the gap between atomically thin semiconductors and metal leads." Nature Communications 13.1 (2022): 1777.

[7] Collado, Laura, et al. "Unravelling the effect of charge dynamics at the plasmonic metal/semiconductor interface for CO_2 photoreduction." Nature communications 9.1 (2018): 4986.

[8] Iida, Kenji, and Masashi Noda. "Electron transfer governed by light-matter interaction at metal–semiconductor interface." npj Computational Materials 6.1 (2020): 5.

[9] Jock, Ryan M., et al. "A silicon metal-oxide-semiconductor electron spin-orbit qubit." Nature communications 9.1 (2018): 1768.

[10] Knobloch, Theresia, et al. "Improving stability in two-dimensional transistors with amorphous gate oxides by Fermi-level tuning." Nature Electronics 5.6 (2022): 356-366.

[11] Lüth, Hans. Solid surfaces, interfaces and thin films. Vol. 4. Berlin: Springer, 2001.

[12] Marmiroli, Nelson, Jason C. White, and Jing Song, eds. Exposure to engineered nanomaterials in the environment. Elsevier, 2019.

[13] Gao, Feng, ed. Advanced nanomaterials for solar cells and light emitting diodes. Elsevier, 2019.

[14] Duke, Charles B. "Semiconductor surface reconstruction: The structural chemistry of two-dimensional surface compounds." Chemical reviews 96.4 (1996): 1237-1260.

[15] Srivastava, G. P. "Theory of semiconductor surface reconstruction." Reports on Progress in Physics 60.5 (1997): 561.

[16] Yasir, Muhammad. "Atomic scale engineering and understanding of novel interfaces between oxide films and semiconductor crystals." (2017).

[17] Srivastava, G. P. "The electron counting rule and passivation of compound semiconductor surfaces." Applied surface science 252.21 (2006): 7600-7607.

[18] Laukkanen, P., et al. "Electronic and structural properties of the InP(100)(2×4) surface studied by core-level photoemission and scanning tunneling microscopy." Surface science 600.15 (2006): 3022-3027.

[19] Schmidt, W. G., et al. "InP(001)-(2×1) surface: a hydrogen stabilized structure." Physical review letters 90.12 (2003): 126101.

[20] John, A. Dean. "Lange's handbook of chemistry." Universitas of Tennese Knoxville, Fifthenth Edition, Mc. Graw Hill Inc, New York. Conference. 1999.
[21] Kim, Meeri. "Extending the metal-induced gap state model to include silicides." Scilight 2020.30 (2020).
[22] Spicer, W. E., et al. "Unified defect model and beyond." Journal of Vacuum Science and Technology 17.5 (1980): 1019-1027.
[23] Hasegawa, Hideki, and Hideo Ohno. "Unified disorder induced gap state model for insulator-semiconductor and metal-semiconductor interfaces." Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena 4.4 (1986): 1130-1138.
[24] Streetman, Ben G., and Sanjay Banerjee. Solid state electronic devices. Vol. 4. New Jersey: Prentice hall, 2000.
[25] Fenner, D. B., D. K. Biegelsen, and R. D. Bringans. "Silicon surface passivation by hydrogen termination: A comparative study of preparation methods." Journal of Applied Physics 66.1 (1989): 419-424.
[26] Lee, Sang Hee, et al. "Review of advanced hydrogen passivation for high efficient crystalline silicon solar cells." Materials Science in Semiconductor Processing 79 (2018): 66-73.
[27] Song, Lihui, Deren Yang, and Xuegong Yu. "Investigation on the impact of hydrogen on the passivation of silicon surface states in clean and copper contaminated conditions." AIP Advances 9.10 (2019).
[28] Nilsson, Anders, Lars GM Pettersson, and Jens Norskov, eds. Chemical bonding at surfaces and interfaces. Elsevier, 2011.
[29] Weldon, Marcus K., et al. "The surface science of semiconductor processing: gate oxides in the ever-shrinking transistor." Surface science 500.1-3 (2002): 859-878.
[30] Rad, Zahra Jahanshah, et al. "Decreasing Interface Defect Densities via Silicon Oxide Passivation at Temperatures Below 450 °C." ACS Applied Materials & Interfaces 12.41 (2020): 46933-46941.
[31] Mannarino, Manuel, et al. "Surface characterization of InP trenches embedded in oxide using scanning probe microscopy." Journal of Applied Physics 118.22 (2015).
[32] Cuypers, Daniel, et al. "Wet chemical etching of InP for cleaning applications: I. An oxide formation/oxide dissolution model." ECS Journal of Solid State Science and Technology 2.4 (2013): P185.
[33] Wang, Fengyou, et al. "Full-scale chemical and field-effect passivation: 21.52 % efficiency of stable MAPbI3 solar cells via benzenamine modification." Nano Research (2021): 1-7.
[34] Davis, Kristopher O., and Winston V. Schoenfeld. "Engineered interfaces using surface and contact passivation in silicon solar cells." The Electrochemical Society Interface 27.1 (2018): 63.
[35] Yao, Z-Q., et al. "High quality ultrathin dielectric films grown on silicon in a nitric oxide ambient." Applied physics letters 64.26 (1994): 3584-3586.
[36] Wang, X-S., et al. "Nitridation of Si(111)." Surface science 494.2 (2001): 83-94.
[37] Lu, H. H., et al. "Improved interfacial quality of GaAs metal-oxide-semiconductor device with NH_3-plasma treated yittrium-oxynitride as interfacial passivation layer." Microelectronics Reliability 56 (2016): 17-21.
[38] Liu, Chao-Wen, et al. "High-k gate dielectric GaAs MOS device with LaON as interlayer and NH_3-plasma surface pretreatment." Chinese Physics B 24.12 (2015): 127304.
[39] Akkaya, A., et al. "A Study on the Electronic Properties of SiO_xN_y/p-Si Interface." Silicon 10 (2018): 2717-2725.
[40] Alekseev, Prokhor A., et al. "Nitride surface passivation of GaAs nanowires: impact on surface state density." Nano letters 15.1 (2015): 63-68.
[41] Schroder, Dieter K. Semiconductor material and device characterization. John Wiley & Sons, 2015.
[42] Brillson, L. J. "The structure and properties of metal-semiconductor interfaces." Surface Science Reports 2.2 (1982): 123-326.

[43] Meyerhof, Walter E. "Contact potential difference in silicon crystal rectifiers." Physical Review 71.10 (1947): 727.
[44] Bardeen, John. "Surface states and rectification at a metal-semiconductor contact." Physical review 71.10 (1947): 717.
[45] Cowley, A. M. "Depletion capacitance and diffusion potential of gallium phosphide Schottky-barrier diodes." Journal of Applied Physics 37.8 (1966): 3024-3032.
[46] Datta, Suman, Wriddhi Chakraborty, and Marko Radosavljevic. "Toward attojoule switching energy in logic transistors." Science 378.6621 (2022): 733-740.
[47] Allen, Thomas G., et al. "Passivating contacts for crystalline silicon solar cells." Nature Energy 4.11 (2019): 914-928.
[48] Allen, Thomas G., et al. "A low resistance calcium/reduced titania passivated contact for high efficiency crystalline silicon solar cells." Advanced Energy Materials 7.12 (2017): 1602606.
[49] Ho, Johnny C., et al. "Controlled nanoscale doping of semiconductors via molecular monolayers." Nature materials 7.1 (2008): 62-67.
[50] Björk, Mikael T., et al. "Donor deactivation in silicon nanostructures." Nature nanotechnology 4.2 (2009): 103-107.
[51] Wijnheijmer, A. P., et al. "Enhanced donor binding energy close to a semiconductor surface." Physical review letters 102.16 (2009): 166101.
[52] Li, Sheng S. Semiconductor physical electronics. Springer Science & Business Media, 2012.
[53] Sah, Chih-Tang. Fundamentals of solid-state electronics. World Scientific, 1991.
[54] Chopra, K. L., S. Major, and D. K. Pandya. "Transparent conductors-a status review." Thin solid films 102.1 (1983): 1-46.
[55] Meiners, L. G., and H. H. Wieder. "Semiconductor surface passivation." Materials Science Reports 3.3-4 (1988): 139-216.
[56] Laukkanen, P., et al. "Passivation of III–V surfaces with crystalline oxidation." Applied Physics Reviews 8.1 (2021).
[57] Sharma, U., et al. "Advancement of gate oxides from SiO_2 to high-k dielectrics in microprocessor and memory." Journal of Physics: Conference Series. 2267, 1, IOP Publishing, 2022.
[58] Robertson, J., O. Sharia, and A. A. Demkov. "Fermi level pinning by defects in HfO_2-metal gate stacks." Applied Physics Letters 91.13 (2007).
[59] Huang, Anping, et al. "Fermi-level pinning in full metal/high-k/SiO_2/Si stacks." Journal of Applied Physics 122.19 (2017).
[60] Xu, Min, et al. "New insights in the passivation of high-k/InP through interface characterization and metal-oxide-semiconductor field effect transistor demonstration: Impact of crystal orientation." Journal of Applied Physics 113.1 (2013).
[61] O'reilly, E. P., and J. Robertson. "Electronic structure of amorphous III-V and II-VI compound semiconductors and their defects." Physical Review B 34.12 (1986): 8684.
[62] Lin, L., and J. Robertson. "Defect states at III-V semiconductor oxide interfaces." Applied Physics Letters 98.8 (2011).
[63] Komsa, Hannu-Pekka, and Alfredo Pasquarello. "Identification of defect levels at $In_xGa_{1-x}As$/oxide interfaces through hybrid functionals." Microelectronic engineering 88.7 (2011): 1436-1439.
[64] KC, Santosh, et al. "Electronic properties of InP(001)/HfO_2 (001) interface: Band offsets and oxygen dependence." Journal of Applied Physics 115.2 (2014).
[65] Galatage, R. V., et al. "Effect of post deposition anneal on the characteristics of HfO_2/InP metal-oxide-semiconductor capacitors." Applied Physics Letters 99.17 (2011).
[66] Dong, H., et al. "Indium diffusion through high-k dielectrics in high-k/InP stacks." Applied Physics Letters 103.6 (2013): 061601.
[67] Dingemans, Gijs, and W. M. M. Kessels. "Status and prospects of Al_2O_3-based surface passivation schemes for silicon solar cells." Journal of Vacuum Science & Technology A 30.4 (2012).

[68] Mokkapati, Sudha, and Chennupati Jagadish. "III-V compound SC for optoelectronic devices." Materials Today 12.4 (2009): 22-32.
[69] Punkkinen, Marko Patrick John, et al. "Oxidized In-containing III-V(100) surfaces: Formation of crystalline oxide films and semiconductor-oxide interfaces." Physical Review B 83.19 (2011): 195329.
[70] Lundstrom, Mark S. Fundamentals of Nanotransistors. Vol. 6. World Scientific Publishing Company, 2017.
[71] Wilson, Rod. "Appendix 1: Vacuum Technology for Applied Surface Science." Surface Analysis-The Principal Techniques (2009): 613-647.
[72] Jousten, Karl, ed. Handbook of vacuum technology. John Wiley & Sons, 2016.
[73] Vickerman, John C., and Ian S. Gilmore, eds. Surface analysis: the principal techniques. John Wiley & Sons, 2011.
[74] Sohail, Hafiz Muhammad. Experimental and Theoretical Studies of Metal Adsorbates Interacting with Elemental Semiconductor Surfaces. Diss. Linköping University Electronic Press, 2014.
[75] Hirvonen Grytzelius, Joakim. Thin Mn silicide and germanide layers studied by photoemission and STM. Diss. Karlstads universitet, 2012.
[76] Hamers, R. J. "Atomic-resolution surface spectroscopy with the scanning tunneling microscope." Annual Review of Physical Chemistry 40.1 (1989): 531-559.
[77] Besenbacher, Flemming. "Scanning tunnelling microscopy studies of metal surfaces." Reports on Progress in Physics 59.12 (1996): 1737.
[78] Chen, C. Julian. "Scanning tunneling microscopy: A chemical perspective." Scanning microscopy 7.3 (1993): 4.
[79] Simmons, John G. "Generalized formula for the electric tunnel effect between similar electrodes separated by a thin insulating film." Journal of applied physics 34.6 (1963): 1793-1803.
[80] Simmons, John G. "Electric tunnel effect between dissimilar electrodes separated by a thin insulating film." Journal of applied physics 34.9 (1963): 2581-2590.
[81] Hjort, Martin. Surface studies of III-V nanowires. Division of Synchrotron Radiation Research, Department of Physics, Lund University, 2012.
[82] Vaara, Riikka-Liisa. Rare-earth-metal-induced Nanoscale Structures on Si(111) Surface Studied by Scanning Tunneling Microscope and Low-energy Electron Diffraction. Turun Yliopisto, 2004.
[83] Alov, N. V. "Fifty years of X-ray photoelectron spectroscopy." Journal of Analytical Chemistry 60 (2005): 297-300.
[84] Laukkanen, Pekka. Atomic and electronic properties of GaAs(100) and InAs(100) semiconductor surfaces. University of Turku, 2005.
[85] Bogan, Justin. Growth and chemical characterisation studies of Mn silicate barrier layers on SiO_2 and CDO. Diss. Dublin City University, 2012.
[86] Perkowitz, Sidney. Optical characterization of semiconductors: infrared, Raman, and photoluminescence spectroscopy. Elsevier, 2012.
[87] Hasegawa, H., et al. "Surface passivation of III–V semiconductors for future CMOS devices-Past research, present status and key issues for future." Applied surface science 256.19 (2010): 5698-5707.
[88] Gfroerer, Timothy H. "Photoluminescence in analysis of surfaces and interfaces." Encyclopedia of analytical chemistry 67 (2000): 3810.
[89] Cui, Zheng, ed. Solution processed metal oxide thin films for electronic applications. Elsevier, 2020.
[90] Stemmer, Susanne, Varistha Chobpattana, and Siddharth Rajan. "Frequency dispersion in III-V metal-oxide-semiconductor capacitors." Applied Physics Letters 100.23 (2012).
[91] Lin, Jun, et al. "A study of capacitance-voltage hysteresis in the HfO_2/InGaAs metal-oxide-semiconductor system." Microelectronic Engineering 147 (2015): 273-276.

[92] Chang, T. C., et al. "Study on SONOS nonvolatile memory technology using high-density plasma CVD silicon nitride." Electrochemical and solid-state letters 7.6 (2004): G113.
[93] König, Dirk, et al. "Modulation doping of silicon using aluminium-induced acceptor states in silicon dioxide." Scientific Reports 7.1 (2017): 46703.
[94] Engel-Herbert, Roman, Yoontae Hwang, and Susanne Stemmer. "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces." Journal of applied physics 108.12 (2010).
[95] Cheng, Cheng-Wei, George Apostolopoulos, and Eugene A. Fitzgerald. "The effect of interface processing on the distribution of interfacial defect states and the CV characteristics of III-V metal-oxide-semiconductor field effect transistors." Journal of Applied Physics 109.2 (2011).
[96] Lee, Eun-Cheol. "Nitrogen-induced interface defects in Si oxynitride." Physical Review B 77.10 (2008): 104108.
[97] Punkkinen, M. P. J., et al. "Stabilization of unstable and metastable InP native oxide thin films by interface effects." Applied Surface Science 567 (2021): 150848.

TURUN
YLIOPISTO
UNIVERSITY
OF TURKU

ISBN 978-951-29-9578-3 (PRINT)
ISBN 978-951-29-9579-0 (PDF)
ISSN 0082-7002 (Print)
ISSN 2343-3175 (Online)

Painosalama Oy, Turku, Finland 2023