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OPTIMIZING POLYCRYSTALLINE SILICON FOR ENERGY-EFFICIENT RADIOFREQUENCY DEVICES WITH A MULTISCALE SIMULATION APPROACH

Mikael Santonen

TURUN YLIOPISTON JULKAISUJA – ANNALES UNIVERSITATIS TURKUENSIS
SARJA - SER. AI OSA - TOM. 735
ASTRONOMICA - CHEMICA - PHYSICA - MATHEMATICA — TURKU 2025

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The originality of this publication has been checked in accordance with the University of Turku quality assurance system using the Turnitin OriginalityCheck service.

ISBN 978-952-02-0128-9 (PRINT)
ISBN 978-952-02-0129-6 (PDF)
ISSN 0082-7002 (PRINT)
ISSN 2343-3175 (ONLINE)
Painosalama, Turku, Finland, 2025

UNIVERSITY OF TURKU
Faculty of Science
Department of Physics and Astronomy
Materials Science
SANTONEN, MIKAEL: Optimizing polycrystalline silicon for energy-efficient radiofrequency devices with a multiscale simulation approach
Doctoral dissertation, 128 pp.
Doctoral Programme in Exact Sciences (EXACTUS)
April 2025

ABSTRACT

Increasing demand of applications involving high-frequency devices such as wireless communications exposes limitations, problems, and different sources of signal loss. These issues continue to provide interesting and wide-reaching topics for silicon research, despite it being one of the most researched materials.

The main focus of this work is to investigate silicon substrates on which such devices are built. These devices typically also feature oxide layers to insulate the parts that carry the signal. In higher frequencies (radio frequency devices, RF), we encounter increasing losses in the substrate due to a charge layer forming near the interface of silicon and oxide. One solution to mitigating losses is the introduction of a polycrystalline silicon layer between the silicon substrate and the oxide.

Due to the mismatches of differently oriented grains in the polysilicon, the modeling and investigation of polysilicon is more complicated than single-crystalline silicon. With a set of computational methods, simulations and theoretical modeling, we investigate polysilicon and how the properties of polysilicon can be used to prevent the harmful substrate losses that degrade device performance.

Classical molecular dynamics simulations (LAMMPS) are used to investigate the growth of the polysilicon, with a particular focus on the miscoordinations of the silicon atoms at the grain boundaries. Ab initio quantum mechanical calculations (VASP) connect structural miscoordinations with resulting electronic properties. An iterative Poisson solver is developed and used together with theoretical modeling of polysilicon resistivity to investigate the oxide-(poly)silicon interface. An extension for existing resistivity models is developed to examine the effect of grain size distributions on polysilicon resistivity. Finally, device simulations are used to investigate the loss behavior of different polysilicon films. These different methods form a linked simulation chain, where the results of the previous link provides input for the next step starting from the atomic scale all the way to the device level.

KEYWORDS: Silicon, Polysilicon, Device loss, Fixed oxide charge, Parasitic surface conduction, Molecular dynamics, Resistivity modeling, Ab initio, Device simulation

TURUN YLIOPISTO
Matemaattis-luonnontieteellinen tiedekunta
Fysiikan ja tähtitieteen laitos
Materiaalitiede
SANTONEN, MIKAEL: Optimizing polycrystalline silicon for energy-efficient radiofrequency devices with a multiscale simulation approach
Väitöskirja, 128 s.
Eksaktien tieteiden tohtoriohjelma (EXACTUS)
Huhtikuu 2025

TIIVISTELMÄ

Korkeataajuuksisten laitteiden kysynnän jatkuva kasvu ja kehitys, esimerkiksi langattomassa tiedonsiirrossa, nostaa esille rajoitteita ja ongelmakohtia, jotka johtavat heikentyneeseen tehokkuuteen. Vaikka pii onkin yksi maailman tutkituimmista materiaaleista, nämä ongelmat tarjoavat edelleen mielenkiintoisia ja laajalti hyödyttäviä tutkimusaiheita.

Tämän työn ensisijainen tehtävä oli tutkia piisubstraatteja, joiden päälle rakennetaan erilaisia korkeilla taajuuksilla operoivia mikropiirejä. Nämä laitteet sisältävät piin lisäksi tyypillisesti myös oksidikerroksen, jonka tehtävänä on eristää signaali. Korkeilla taajuuksilla havaitaan kuitenkin taajuuden mukana kasvavia häviöitä. Nämä häviöt johtuvat piisubstraattiin, oksidirajapinnan läheisyyteen, syntyvästä haitallisesta varauskerroksesta. Eräs keino häviöiden pienentämiseen on monikiteisen piikerroksen (polypii) lisääminen piipohjan ja oksidin väliin.

Monikiteinen pii koostuu eri suuntaisista rakeista. Näiden rakeiden välissä on raerajoiksi kutsuttuja alueita, jotka tekevät monikiteisestä piistä monimutkaisemman materiaalin kuin kiteinen pii. Eri simulaatio- ja mallinnusmenetelmiä hyödyntäen muodostimme laskennallisen mallinnusketjun, jolla tutkimme monikiteistä piitä ja miten sen ominaisuuksia voidaan käyttää vähentämään korkeataajuuksisten laitteiden häviöitä.

Klassista molekyylidynamiikkaa (LAMMPS) käytetään monikiteisen piin kasvun tutkimiseen, keskittyen erityisesti sidosvirheisiin raerajoilla. Ab initio kvanttimekaanisia laskuja (VASP) käytetään tutkittaessa virheistä syntyviä elektronisia ominaisuuksia. Iteratiivinen Poisson ratkaisin kehitettiin jota yhdessä monikiteisen piin resistiivisyyden mallintamisen kanssa, käytetään tutkittaessa oksidi-(poly)pii-rajapintaa. Olemassa olevaan resistiivisyysmallinnukseen tehtiin laajennus, jonka avulla voimme ottaa myös raekokojakauman huomioon. Lopulta erilaisten polypiikerrosten häviöitä
tutkitaan laitesimulaatioilla. Eri menetelmistä muodostetaan simulaatioketju, jossa edeltävän menetelmän tuloksista saadaan sisään syötettävää dataa ketjun seuraavalle osalle.

ASIASANAT: Pii, Monikiteinen pii, Laitehäviöt, Kiinteä oksidivaraus, Parasiittinen pintajohtavuus, Molekyylidynamiikka, Resistiivisyysmallinnus, Ab initio, Laitesimulaatiot

Acknowledgements

This thesis was done at the Department of Physics and Astronomy in the Materials Research Laboratory between 2022 and 2025. Firstly, I am extremely grateful to Kalevi Kokko, who supervised my work all the way from my Bachelor's thesis to this doctoral research. His guidance and expertise helped me countless times throughout this endeavor. Huge thanks to Marko Punkkinen as well for his support and role as the supervisor of my doctoral work.

The bulk of the research was done in the Business Finland-funded BEETLES-project. Collaboration in the project was very important. I would like to extend my thanks to Okmetic and particularly to Heikki Holmberg and Katja Parkkinen. I would also like to thank Antti Kuronen from the University of Helsinki and Jan Saijets from VTT, who provided help in their respective areas of expertise. I also had the chance to visit KTH Stockholm during this project. I am thankful to Levente Vitos for hospitality and help. Huge thanks to Antti Lahti, with whom I worked together on the project. He provided great support and fruitful collaboration at the office and at our weekly meetings.

After the project finished, the financial support from the Finnish Cultural Foundations regional fund allowed me to write my thesis and therefore I would like to acknowledge them. The computer resources of the Finnish IT Center for Science (CSC) and the Finnish Computing Competence Infrastructure (FCCI) project (Finland) are also acknowledged.

The support of the research group has been important. On the experimental side of things, I would like to thank Zahra Jahanshah Rad and Mikko Miettinen for their help, especially in preparing the publications. Thanks also to Pekka Laukkanen for his support. I had the pleasure to share the room with the previously mentioned Antti Lahti and Kalevi Kokko as well as with Masoud Ebrahimzadeh and Johanna Laaksonen. Thank you for the comfortable working environment. Finally, I would like to thank my family and friends for their support throughout the process.

3.4.2025

Mikael Santonen

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1 Introduction

With the ever-increasing demand for energy-efficient, compact, and performant integrated circuits, further and further research is needed into the parts that make up these circuits. Investigations into substrate losses at microwave frequency range revealed another use case for silicon, in this case in its polycrystalline form. The fixed oxide charges that form into the insulating oxide layer introduce a compensating charge carrier layer (parasitic charge) into the substrate. These parasitic charges can be a significant source of losses in high frequency circuits. To mitigate this parasitic charge, a polysilicon layer can be used [1].

Tools of computational materials science provide a great way of investigating materials from various size scales. This work employs a multiscale approach from the atomic-level of structural and electronic properties to the device-level performance to improve the substrate consisting of (poly)silicon. The ultimate goal being more performant chips.

In the first chapter, I will introduce the key materials (silicon, polysilicon, silicon dioxide), the problems that this work investigates to solve (parasitic charge), some background into the source of these problems (silicon-oxide-interface), a brief overview of the methods used to investigate these problems (atomistic simulation, resistivity modeling, device simulations), and how these methods are linked to form a theoretical/simulation-based framework to improve (poly)silicon substrates. The methods can roughly be divided into atomistic-level simulations and device-level investigations. The atomic simulations provide details about the structural and electronic properties of polysilicon. These simulations, background on how they work and how they are used in these work are covered in Chapter 2. Chapter 3 is focused on the more macroscopic side of investigations. There we delve into how different parameters affect the distribution of charges in the substrate and how this distribution affects device performance. This chapter features its own set of simulation/theoretical methods, which are covered correspondingly. Finally, Chapter 4 provides a summary of the publications and Chapter 5 provides some thoughts on this work as a whole with concluding remarks, potential future investigations, etc., after which the publications can be found.

1.1 Silicon

Silicon, one of the most common materials found on earth, has many useful properties and its versatility makes its use cases uncountable. A notable highlight is its use in electronics. It functions as the foundational base on top of which, both figuratively and literally, a huge part of electronics is built.

1.1.1 Semiconductors

Silicon is a semiconductor, which is the source of its versatility in its electrical properties. The conductive properties of a material can be described and analyzed by its band structure. The conduction process happens through the net movement of charge carriers. This charge carrier often is the electron, a fermion, meaning it obeys the Pauli exclusion principle: two electrons cannot be found in the same electronic state at the same time. An atom has a discrete set of these electronic states, which can be occupied by an electron. When these atoms come together to form a solid, they form what can be essentially considered to be continuous "bands" of allowed electronic states. The distribution and amount of these electronic states at different energy levels is described by the density of states (DOS) function. Electrons start filling these states starting from the energetically lowest states. Important thermodynamic quantity related to the filling of these states is the Fermi level (E_F). It is an energy level, which corresponds to the theoretical level at which an electronic state has a 50% chance of being filled. The probability distribution of electronic state occupation is temperature dependent. At 0 K, states below E_F are filled and states above are not. As the temperature increases, some energetically higher states are occupied by thermally excited electrons. The probability distribution describing this is called the Fermi-Dirac distribution. [2]

For a metal (a conductor), the filling stops at a point in the band structure, where there are still many states energetically directly above i.e. the Fermi level is within a continuous band. This allows for easy conduction, since electrons have many easily available states for movement. However, if the filling stops at the edge of one of these bands, the next available states can be many eV away in the next band. This energy gap is called the band gap. Insulators exhibit large enough band gaps that conduction is very limited. Semiconductors, on the other hand, are often described as the middle ground between the conductors and insulators. They still exhibit a band gap but gap values are typically smaller than those of insulators. [2]

The Fermi level of a semiconductor is typically located somewhere in the band gap. The band below is called the valence band and the one above the conduction band. Importantly, the position of the Fermi level relative to these bands (and therefore the electrical properties) can be easily modified by introducing impurity atoms (dopants) to the material. Typical dopants used in silicon are for example ar-

senic, phosphorus, and boron. Arsenic and phosphorus atoms feature five valence electrons (silicon features four). When introduced into the system, they form bonds with silicon atoms but one valence electron is left over. The dopant atom introduces electronic states into the gap, from which the leftover electron can be excited to the conduction band with much less energy than overcoming the full gap. This results in a positive dopant ion and a free electron for current transport. The bands are shifted such that the Fermi level is closer to the conduction band. This is called n-type (n^-) doping. Boron, on the other hand, has three valence electrons. An electron from the valence band can fairly easily excite to the acceptor state to fill the hole, which results in a positively charged hole in the valence band and a negatively charged dopant atom. These holes in the valence band are free charge carriers for current transport. This in turn is called p-type (p^+) doping. Since the process of excitation requires energy, the amount of free carriers is a function of temperature, at least until the full ionization of all the dopant atoms. [2]

Interfaces and junctions can also affect the position of the Fermi level relative to the bands. Band bending at interfaces and junctions of semiconductors and other materials is key for the operation of many devices, such as transistors, diodes and solar cells. [2]

1.1.2 Structure

The energetically most favorable crystal structure of silicon is the cubic diamond structure. In it, a silicon atom is bonded to four different silicon atoms in a tetrahedron. Solid silicon can be commonly found in three categories (Fig. 1) relevant for this work. The most disordered of these is amorphous silicon (a-Si), which doesn't exhibit any long-range ordered structure. Single-crystal silicon, on the other hand, is ordered in the same continuous diamond structure throughout. Polycrystalline silicon is ordered in the medium range, but features many differently oriented regions called grains. The structure is ordered within each grain but the discontinuities where the differently ordered grains meet, called grain boundaries, introduce different miscoordinations. These grain boundaries are a key part for the purposes of this work, and they are the part that causes its properties to differ from single-crystal silicon. The properties inside the grains are essentially identical to single-crystal silicon.

1.1.3 Polycrystalline silicon

Polycrystalline silicon (polysilicon, poly-Si, p-Si) is a form of silicon that consists of many differently oriented crystalline grains. It has been used, for example, as the "metal" gate in MOS-transistors (MOS, *metal-oxide-semiconductor*) and solar cells because of the abundance, safety, and processing costs of silicon. In these cases, polysilicon is often used because of the cost-effectiveness compared to pure

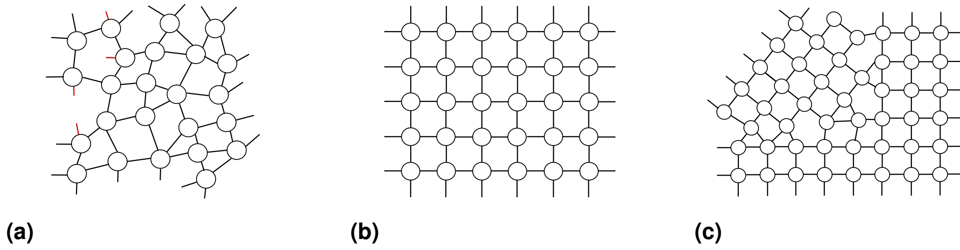
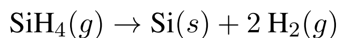


Figure 1. Relevant structural types of silicon represented with a 2D model. a.) amorphous silicon contains some short range ordering (preference for four-coordinated atoms and certain bond length) but no long range structure is present b.) Single-crystalline silicon consists of a cubic diamond structure throughout c.) polycrystalline silicon consists of many differently ordered crystalline grains.

single-crystalline silicon. The polysilicon in these applications is often with large grain sizes, heavily doped. The grain boundary is seen as a downside. In this work, however, the polysilicon we target should feature plenty of grain boundaries and a lot of resulting trapping states to best capture parasitic charges and reduce the losses that arise from the parasitic conduction (Section 1.3).

Polysilicon is often grown with a chemical vapor deposition process. The deposition is often done at low pressure (on the order of 10^{-4} atm) around 625°C (low pressure chemical vapor deposition, LPCVD). The process is quite sensitive to temperature and good control of temperature is necessary. The growth rate increases fairly linearly as a function of temperature. At lower temperatures (below 575°C), the rate quickly becomes too low to be practical. At higher temperatures, the depletion of silane causes unevenness of deposition rate in the chamber, which results in wafers of undesirable and uneven quality. [3]

The growth process works by introducing silane gas to the growth chamber, which breaks down on the surface in a chemical reaction into solid silicon and hydrogen gas.



$$\mathrm{SiH_4}(g) \rightarrow \mathrm{Si}(s) + 2\,\mathrm{H_2}(g)$$

The properties of the resulting polysilicon wafers, such as the grain size, depend on the temperature, deposition rate, and partial pressures of the gases, which consists of the silane and potential carrier and dopant gases. The effect of temperature and deposition rate is linked. While higher temperatures provide more energy for the diffusion of atoms, it also provides higher deposition rates, which reduces the surface diffusion length of an adsorbed atom. However, the overall relation is that higher temperatures produce larger grain sizes. Grain sizes also tend to increase as the film gets thicker. Carrier gasses affect the structure by introducing more hydrogen, which impedes with the arrangement of silicon atoms on the surface. Dopant gases similarly can impede the arrangement of the silicon atoms at low deposition rates,

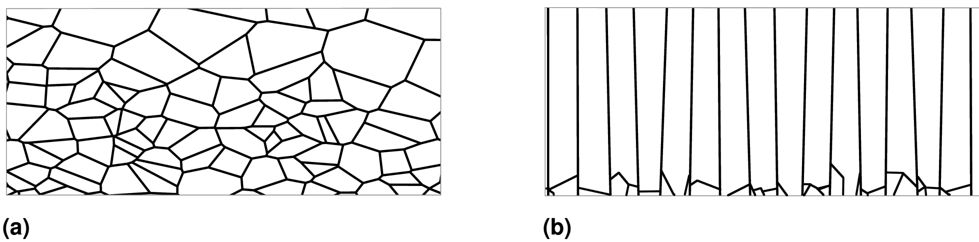


Figure 2. Representation of the side profile of different types of polysilicon. Differing properties can be obtained with different growth conditions. a.) shows a more random grain structure, prevalent particularly at the earlier stages of growth and at lower growth temperatures. b.) shows a columnar structure into which the growth often develops as the film thickness grows.

resulting in smaller grain sizes. [3]

Different methods can be used to enhance the deposition. For example, by introducing high energy plasma into the deposition chamber, the decomposition of the precursor molecules can be made easier (plasma-enhanced chemical vapor deposition, PECVD). This allows for lower deposition temperatures, around 200-400°C. [3]

While the initial growth of polysilicon consists of a nucleation phase, where the grains initially start forming and are small, the polysilicon type can vary quite a bit after this depending on the parameters of growth. Fig. 2 shows two different poly types as examples. On the left, a more random grain structure can be found. The right of the figure shows a columnar-type polysilicon. This type can be found particularly as the film thickness grows and the growth favors certain grain orientations. [3]

The mobility of carriers in the grains is comparable to single-crystal silicon but the grain boundaries introduce discontinuities, which reduces the mobility and alters the properties from that of the single-crystal silicon. How much does the grain boundary affect? It is a question of which types of grain boundaries are present and which types of additional electronic states do they produce.

1.1.4 Grain boundary

Grain boundaries are the result of discontinuities between neighboring grains, whose orientations cause a mismatch. Different defects, miscoordinations and dangling bonds cause trap states, which reduce the amount of free charges and lowers the mobility of the remaining free charges. In solar cell or MOS applications, the effect of these trap states are typically reduced by passivation (for example with hydrogen) or thermal treatment. Here however, we want to maximize the amount available trapping states to capture the parasitic charges.

Since the grain boundary is typically a narrow structure, typically under 1 nm in width, experimental investigations on specific grain boundaries and boundary types

are often quite difficult. Computational methods therefore are a particularly useful tool. Many investigations into energetics, stable structural configurations, electronic structure, effect on macroscopic properties, etc. have been carried out over the past several decades using various methods such as classical molecular dynamics, tight-binding model based, (Metropolis and kinetic) Monte Carlo, as well as density functional theory calculations [4; 5; 6; 7; 8; 9; 10].

Different types of grain boundaries produce different electronic states. Understanding the source of the states and how they are formed provides a way of optimizing polysilicon for high frequency devices. Grain boundary engineering is a field of research that investigates the potential applications and processing to best use grain boundaries of many materials, from different metals to the polysilicon of our work. The goal is obtaining a large amount of desired grain boundaries, which can feature many interesting mechanical or electrical properties that can be used to our advantage to modify the bulk properties of a given polycrystalline material. [11]

The collection of different grain boundary types is unique to a material and is largely determined by the underlying bulk structure, energetics and structural aspects of the mismatch between the grains. Categorizing grain boundaries can be a bit complicated given the complex nature of real-world boundaries. Grain boundary categorization, however, tries to capture the nature of a grain boundary that arises from two differently oriented grain boundaries. First, one can look at how the neighbor grain is rotated in relation to the reference grain. We can find two main rotations: tilt boundaries are grain boundaries in which the rotation axis is parallel to the grain boundary plane, while in twist boundaries the rotation axis is normal to the boundary plane. The rotation type is then paired with the angle of rotation. Low angle, more symmetric boundaries feature low grain boundary energy, while high angle and more random boundaries feature high energies [11]. Fig. 3 shows an example of the atomic structure of a tilt boundary.

Coincident site lattice (CSL) is a type of mathematical model often used for grain boundary categorization. CSL works by overlaying the neighboring grains on top of each other and looking for overlapping sites. The sigma notation of CSL (reciprocal density of overlapping sites) tells how well the lattices overlap. Low sigma values (starting from $\Sigma3$) correspond to high degrees of overlap and increasing sigma values mean decreasing amount of overlapping sites. However, there is some dispute on the usefulness of CSL beyond a simple, fairly easy to understand, preliminary categorization tool [12]. Grain boundaries in nature typically don't feature neatly definable boundary planes and are more complicated.

The main source of electronic states in the gap, which can serve as trapping states for the free charge carriers, are from miscoordination and distortions in the bond angles and lengths. High-symmetry grain boundaries feature very little electronic activity in the gap, since there is relatively little disturbance, while more random and disordered boundaries feature more activity. The silicon atom in its ordered structure

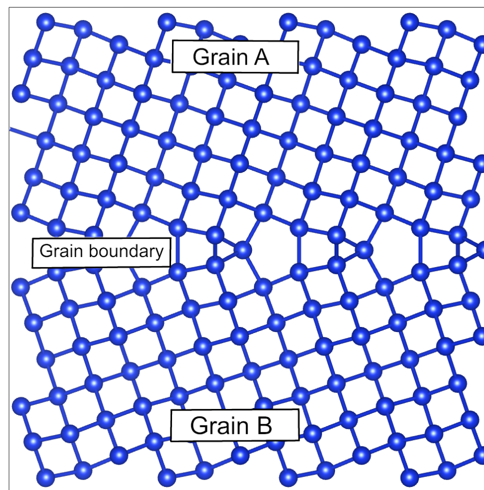


Figure 3. Example of the atomic structure of an tilt grain boundary found in polysilicon. At the top and bottom are differently oriented grains and the grain boundary is in the middle as the discontinuity between them.

is bonded with four other silicon atoms. When the two neighboring grains meet, the mismatch can cause some atoms to have only three bonds. This atom would then feature what is often called a dangling bond. Atoms can also overcoordinate i.e., bond with five or more atoms. Example cases analyzed from the grain boundaries found in the growth simulations are shown in Fig. 4a. The top one shows the normal four-bonded case. At bottom left is the three bonded, which is missing one bond (dangling) and the structure overall has flattened (bond angles have changed). Bottom right features a five-bonded example.

Linking certain grain boundary types and particularly defect types to certain electronic states remains a difficult task but the overall effect is shown in the trap state model of Fig. 4b. Typical electronic trap states can be divided into the so-called shallow traps and deep traps. In shallow traps, the conduction and valence band tails extend into the gap. The deep trap states are states found deeper in the gap. Deep traps are harder to detrap, since the energy required is higher than for the trapped particles right next to the corresponding band. Depending on the position of the trap in the gap, a trap state can trap either an electron or a hole. [13; 14; 15] Shallow traps have been modeled with exponential functions decaying from the corresponding band and deep traps as Gaussian peaks near mid-gap in theoretical modeling of polysilicon resistivity and RF-simulations [16; 17] (in this work used in Chapter 3).

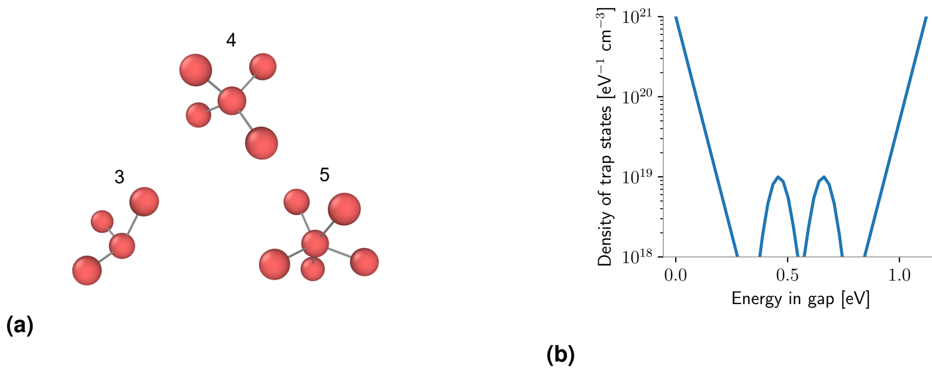


Figure 4. a.) shows differently coordinated atoms. The four coordinated silicon is the one found in monocrystalline silicon in its diamond structure. Grain boundaries and other defects can introduce different miscoordinations, which can alter the bond angles, bond lengths, and number of bonds. Examples of three coordinated and five coordinated atoms found at the grain boundaries of the simulations are presented below the four coordinated example. Miscoordinated atoms can introduce different electronic states into the band gap, which act as trapping states. b.) shows a model density of states of a polysilicon grain boundary band gap, which contains trapping states from different miscoordinations. Shallow traps are states extending from the valence and conduction bands into the gap. Deep traps are peaks found inside the gap, near to the center.

1.2 Interfaces

Interfaces are unavoidable when forming electronic devices/microcircuits, since different parts of the device perform different functions. The device requires some base on which to build, the substrate. The signal is transported to different parts with highly conductive metal strips and insulating layers make sure that the signal doesn't go to places where it shouldn't.

However, because in interfaces we are transitioning between materials with potentially very different structural and electrical properties, the interface can be a source of different, potentially harmful, phenomena. Interfaces can have significant impact on the atomic structures on both sides of the interface, which can lead to different electronic properties. Since the devices are getting increasingly smaller and more complex, the amount of bulk material is reduced, as is the distance between components. The properties of interfaces will therefore increasingly have an impact on the behavior of a device, potentially in degrading ways. To mitigate potential issues, good understanding of the interfaces, often at the atomic level, is required.

In this work there are two key interfaces at play: the interface of silicon dioxide and (poly)silicon as well as the interfaces found in polysilicon: the grain boundaries. Oxide-silicon interface is key as it introduces the fixed oxide charges, which is detrimental to device performance. Polysilicon grain boundaries introduce differences in the electrical properties when compared to monocrystalline silicon, which for the purposes of this work are to our benefit. The detrimental effects of one interface are

counteracted by another interface. [3; 18]

1.2.1 Silicon dioxide and fixed oxide charge

Silicon dioxide is an insulator. The main purpose of it in devices relevant to this work (mainly the coplanar waveguide) is to isolate components such that a significant amount of signal doesn't end up in the silicon substrate causing losses or in other components causing interference with its operation. It is widely used for its relatively easy manufacturing, temperature stability, well established and researched processing, as well as the compatibility with the silicon substrate. The oxide layer is manufactured onto the silicon substrate, typically either via thermal oxidation or chemical vapor deposition. In thermal oxidation, the oxidation is done at high enough temperature (over 800°C) such that the oxide layer forms thicker than the native oxide at room temperature. This can be done in a water vapor (wet oxidation) or oxygen molecule (dry oxidation) environment. In chemical vapor deposition, a suitable gas converts on the surface into solid silicon dioxide and leftover gasses. [3] Polysilicon adds an extra consideration when compared to monocrystalline silicon by containing grains of differing orientations as well as the grain boundaries. Since different orientations feature different oxidation rates and the grain boundary region tends to oxidize faster than grains, the result can be quite an uneven oxide layer. [3]

Particularly when operating at high frequencies, the interface of the silicon and the silicon dioxide becomes important. Fixed oxide charges are a type of charge locked in place when the oxide is formed on top of the silicon. This charge is thought to form intrinsically due to the interface and not as the result of some external contamination. [19] The fixed charges are located on the interface and in the oxide at the immediate vicinity (within the first 25 Å) of the silicon. They are formed in the initial steps of the oxidation and are due to different structural defects. Similarly, some interfacial trap states are also formed. These can also feature trapped charges, but they are considered distinct, since they can have charge transfer to the silicon, trap state passivation, etc. unlike with the fixed oxide charges. [20]

Typical densities of fixed oxide charges Q_f range from 10^{10} to 10^{12} cm^{-2}. With silicon dioxide, it is positive in sign. The resulting density of fixed charges is influenced by factors such as the orientation of the silicon substrate ($Q_{f,100} < Q_{f,110} < Q_{f,111}$), conditions of oxidation (temperature, pressure), and annealing treatments. [21] Different oxides can also similarly form fixed charges and therefore present similar problems [22].

1.3 Main problem: Parasitic surface condition

The source of the problem at the core of this work is a phenomenon called parasitic surface conduction. The parasitic surface layer that forms near the oxide-substrate

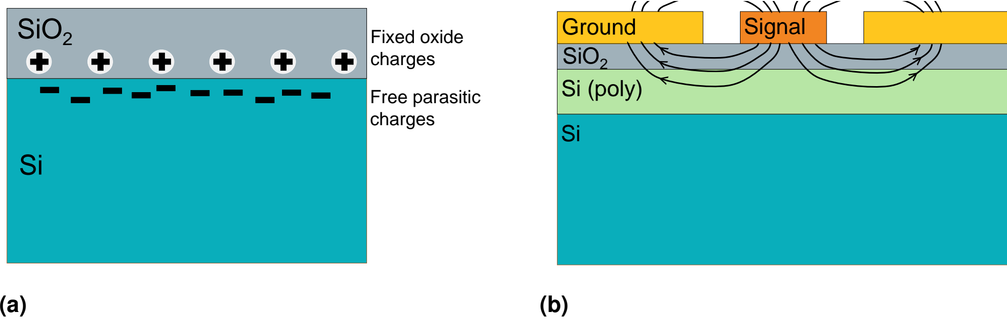


Figure 5. a.) The parasitic charge layer forms as the fixed oxide charges draw free electrons in the silicon substrate towards the interface to compensate for the positive fixed oxide charge b.) Penetrating electric fields of a high frequency signal moves the free charges in substrate causing losses. A polysilicon layer is added to mitigate these losses by trapping free electrons.

interface is a significant source of signal loss and other unwanted device behavior, particularly as we move to higher frequencies.

A typical device is formed on a silicon substrate. An insulating layer, often silicon dioxide, is formed on top of it and conducting elements, in turn, are formed on top of it. When an alternating current signal is going on the top, electric field can penetrate to the substrate. The oxide layer prevents some of this, but as we increase the frequency, we also increase how much it can penetrate. To make sure the penetrating electric field causes as little loss as possible, we need the substrate layer to be resistive. High-resistivity silicon (HR-Si), however, did not improve the performance. As shown in Fig. 5a.), a positive fixed oxide charge layer forms right on the interface. A compensating negative charge layer forms as free electrons in the substrate move towards the interface. Regardless of the nominal resistivity of the silicon, this parasitic layer lowers the local resistivity. When the electric field starts moving the parasitic charges, the result is ohmic losses. A polysilicon layer is introduced between the HR-Si and the oxide to capture the compensating mobile electrons. Example coplanar waveguide is shown in Fig. 5b.), where the parasitic charges are trapped in the polysilicon layer and the penetrating electric field causes less loss. The goal is to find what type of polysilicon is best for the job, what are the trapping state properties, what type of structure produces the wanted trapping states and how do we produce these. [15]

1.4 Methods used

This work is predominantly a computational investigation into polysilicon and its use in radiofrequency devices. Computational materials science uses different theoretical and empirically fitted models to model the behavior of different materials and interactions between them. This approach provides a way to examine different

problems in ways not possible by conventional experimental methods. As with any tool, knowing the limitations is key to effective use. Chapter 2 and Chapter 3 give a run-through of the methods used in this work, as well as how and what they are used for. The results are compared to experimental findings from the literature and our research group's and collaborators experimental work to validate the approaches used.

For investigations of polysilicon as the mitigator of parasitic surface conduction-related losses in high-frequency device applications, we use several computational tools and theoretical models. Investigations have been carried out at different scales. At the atomic scale, classical molecular dynamics simulations (LAMMPS) have been used to investigate the structural properties and the growth process behind these different structures. Ab initio calculations (VASP) provide a way to investigate the electronic properties that different structures produce. Charge distribution under the influence of the fixed oxide charge has been investigated with a self-written iterative charge distribution solver. Together with theoretical modeling of polysilicon resistivity, we obtain the local electrical properties as a function of depth into the substrate. These results can be used in device simulations, which provide information about the actual device performance. The methods come together to form a linked simulation chains with which polysilicon can be optimized. Fig. 6 shows the simulation chain and how the different methods feed into each other. Going through the simulation chain, the first block (growth simulations) is covered in Section 2.1, second (grain boundary analysis) in 2.2, third (distribution of the parasitic charge) in 3.1, fourth (resistivity modeling of polysilicon) in Sections 3.2–3.4, and final block (device simulations) in 3.5.

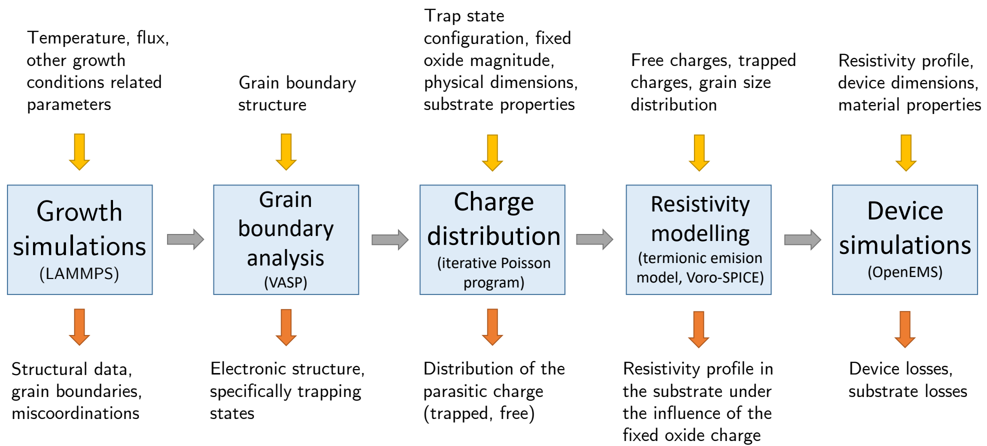


Figure 6. Chain of methods and investigations that provide a computational/theoretical approach to optimizing polysilicon for mitigating substrate losses in radiofrequency device applications. Each link is an independent module. When the whole comes together, each subsequent module can be used to provide input for following modules, thus linking the investigations from growth parameters all the way to devices, which gives information on how well the mitigation has worked. The blocks are covered and discussed in the following sections (left-to-right): I) Section 2.1, II) Section 2.2, II) Section 3.1, IV) Sections 3.2–3.4 and V) Section 3.5.

2 Atomic scale simulations

Different kinds of atomistic simulations have widespread use cases. This work takes advantage of the two extreme ends. The investigation of the growth process involves simulations of upwards of several million simulated atoms, which limits the accuracy with which we can handle all the interactions. Investigation on the electronic properties of grain boundaries and trap states, on the other end, target accuracy with first-principles calculations, which posits a practical limit of few hundred atoms.

The two methods employed here are classical molecular dynamics (LAMMPS) and quantum mechanical ab initio calculations (VASP). While they differ in their operation, accuracy and use case, they do share some similarities, which can be highlighted here to illustrate how atomistic simulations work. After this, we can proceed to look at the differences, basic operation / working principles and what each of them were used for.

As a rough overview, an atomic scale simulation typically features the following inputs: definition of the system, how the interactions will be calculated and what to simulate. The definition of a system can encompass many aspects. We first form a simulation cell in which the calculations happen. Atoms can then be placed in the simulation cell by giving initial positions, generating blocks of crystalline structures etc. The interactions between atoms, depending on the method, can be calculated, for example using classical interatomic potential or from first principles with quantum mechanics.

2.1 Classical molecular dynamics

Molecular dynamics is a set of methods, which model the movements and time development (the dynamics) of a group of atoms. The time development is done by dividing the simulation into discrete time steps and solving for the motion of the atoms, interactions between them and forces acting upon them modifying their motion. Molecular dynamics can be divided based on how they calculate the interactions in the system. First-principles calculations produce the most accurate results but are limited in their applicability due to the computational load. Classical molecular dynamics take a simpler approach and achieve computationally lighter way of calculating the dynamics of a system.

In this work, molecular dynamics was used to investigate the growth of polysili-

con. The polystructure, however, presents a problem. While deposition of crystalline silicon can be done in quite a small simulation cell, for a simulation cell to contain even a few grains and their corresponding (physically reasonable) grain boundaries, larger cells with larger amounts of atoms are required. This limits our calculations to the more computationally lightweight interatomic potentials and makes classical molecular dynamics the suitable method for the task.

The program used is the Large-scale Atomic/Molecular Massively Parallel Simulator (LAMMPS) [23]. It is a classical molecular dynamics simulator, which as the name suggests also has a focus on parallelization. This "spreads" the calculation onto many processor cores, which allows us to run quite large calculations with large amount of atoms in reasonable computational time. The classical molecular dynamics approach comes with a downside: we only focus on the dynamics of the system via the (semi)classical interatomic force calculations, on the resulting structural properties and ultimately get no insight into the electronic properties of the system.

Even with the lightweight potentials, the simulations are limited to the first few hundred Ångströms of polysilicon growth, with the growth happening in a timescale of few tens of nanoseconds. Since the growth process is random, we need several simulations for the same system to get enough data for good statistics. Therefore, realistic polysilicon growths up to the typical thicknesses of polysilicon layers (on the micrometer scale) are not achievable through simulations. However, aiding us is that the focus in this work is the grain boundary, which unlike the grain sizes shouldn't be quite as limited, since the simulated grain boundaries can be of comparable size as those in real polysilicon.

2.1.1 Calculation of the dynamics

To present an idea on how a molecular dynamics calculation works, I will introduce the basic loop and some key concepts (specifically with the used code LAMMPS in mind). Each atom in the system has a collection of properties. LAMMPS features many presets for these but the basic atom contains the following info: unique ID, atom type, position coordinates, velocity, and force. For a given time step, the goal is to efficiently calculate the forces and update the velocities, while ensuring the thermodynamic specifications of the system. To speed up calculations, forces are calculated only for atoms within a cutoff distance. A data structure called a neighbor list is used to quickly loop through the atoms in range. The potential energy of the atoms is calculated based on interatomic potentials, which contain a set of predetermined (often empirically fitted) parameters. The energy is dependent on the atom positions. In practice this is typically done with relative positions: the potential energy of an atom is a function of interatomic distances and bond angles of neighbor atoms. The forces $\mathbf{F}$ can then be solved based on the total potential energy U, which

also connects the forces to the dynamics with Newton's laws (N II: force F is equal to mass m times acceleration a).

$$-\nabla U = \mathbf{F} = m\mathbf{a} \tag{1}$$

The trajectories of the atoms are calculated by numerically integrating Newton's equations of motion. This is most commonly done with the Velocity Verlet method. First, the velocity $\mathbf{v}$ is updated based on the forces half-step forward in time (Eq. (2), t for time, Δt for time step). The half-stepping is done to avoid the so-called self-starting problem (non-half step version requires info of the previous time step). The half-step velocity is used to update the position $\mathbf{r}$ at full-step (Eq. (3)). The updated position can be then used to calculate the forces (Eq. (4)) at full-step using the interatomic potential. Finally, Eq. (5) gives the full-step velocity, thus completing a single time step. [24]

$$\mathbf{v}(t + \frac{\Delta t}{2}) = \mathbf{v}(t) + \frac{\mathbf{F}(t)}{m}\frac{\Delta t}{2} \tag{2}$$

$$\mathbf{r}(t + \Delta t) = \mathbf{r}(t) + \mathbf{v}(t + \frac{\Delta t}{2})\Delta t \tag{3}$$

$$\mathbf{F}(t + \Delta t) = \mathbf{F}(\mathbf{r}(t + \Delta t)) \tag{4}$$

$$\mathbf{v}(t + \Delta t) = \mathbf{v}(t + \frac{\Delta t}{2}) + \frac{\mathbf{F}(t + \Delta t)}{m}\frac{\Delta t}{2} \tag{5}$$

2.1.2 Interatomic potentials

Despite the rapid improvements in computing, solving the properties of a system using quantum mechanical first-principles calculations is often still computationally too heavy. An interatomic potential attempts to approximate the interactions by calculating the energy of the system based on atomic coordinates. The interacting forces are then given by the gradient, as shown in the previous section. Although the first interatomic potentials were simple two-body potentials, for a lot of cases many-body potentials are necessary.

Since most of the meaningful interaction between atoms is local in nature, we can typically reduce the number of operations significantly by only calculating interactions inside a cut-off radius. With silicon, one might find cut-off radii of around few ångströms. While some well established many-body potentials from the 1980s still find wide use, improved potentials such as charge-transfer potentials and machine learning potentials are increasingly being used and developed. However, the added complexity often makes the potentials computationally heavier and the added accuracy might introduce problems with transferability for cases not found in the training sets. [25]

The main goal with molecular dynamics in this work was to investigate the growth process of polysilicon. The first task in forming the simulation setup was to find a suitable potential. LAMMPS offers support for many potentials to choose from. While the grain sizes in the simulations would inevitably be relatively small, we still need to operate with the largest cells possible to form at least some grain structure. This guides us to choosing a fast potential over the more computationally heavy ones.

The potential for the molecular dynamics simulations was chosen to be the Stillinger-Weber [26; 27]. The choice was made based on a set of preliminary test simulations with a set of different potentials. More information on the selection will be presented further on in Section 2.1.4.

Stillinger-Weber is a three-body interatomic potential, meaning that the energy is dependent on the interatomic distances r_{ij} (double summation in Eq. (6)) of a pair of atoms but also the bond angles θ_{ijk} of atom triplets (triple summation in Eq. (6)). The bonds are handled by the two-body term (Eq. (7)), whose form is that of the widely studied general Lennard-Jones potential with the addition of an exponential term, which ensures a smooth cut-off. This is particularly useful in molecular dynamics, since the gradient of the energy formula is needed for force calculations. The three-body term compares the bond angle of a given configuration to the ideal angle $\cos\theta_0$ to favor the desired geometry, which in the case of silicon is given by the tetrahedral configuration. Similarly to the two-body term, the exponential terms are used to ensure smoothness in the cut-off for the three-body term.

$$U = \sum_i \sum_{j>i} \phi_2(r_{ij}) + \sum_i \sum_{j\neq i} \sum_{k>j} \phi_3(r_{ij}, r_{ik}, \theta_{ijk}) \tag{6}$$

$$\phi_2(r_{ij}) = A_{ij}\epsilon_{ij} \left(B_{ij} \left(\frac{\sigma_{ij}}{r_{ij}}\right)^{p_{ij}} - \left(\frac{\sigma_{ij}}{r_{ij}}\right)^{q_{ij}} \right) \exp\left(\frac{\sigma_{ij}}{r_{ij} - a_{ij}\sigma_{ij}}\right) \tag{7}$$

$$\begin{aligned} \phi_3(r_{ij}, r_{ik}, \theta ijk) =& \lambda_{ijk}\epsilon_{ijk} \left(\cos\theta_{ijk} - \cos\theta_{0,ijk}\right)^2 \\ & \cdot \exp\left(\frac{\gamma_{ij}\sigma_{ij}}{r_{ij} - a_{ij}\sigma_{ij}}\right) \exp\left(\frac{\gamma_{ik}\sigma_{ik}}{r_{ik} - a_{ik}\sigma_{ik}}\right) \end{aligned} \tag{8}$$

Index i denotes the central atom under calculation and j, k go through all the neighbor atom pairs. ϵ and σ are the energy and length units of the form, typically given in eV and Å. The rest of the parameters are unitless. a scaled with the length unit ($a \cdot \sigma$) gives the cut-off distance after which the value of the term is zero. These three (σ, ϵ, a) are used in both two- and three-body terms of U. The two-body term on top of these has four parameters A, B, p, q and the three-body two with λ and $\cos\theta_0$. Based on a set of criteria, a search of these parameters was done by Stillinger and Weber to best describe interactions both in solid and liquid silicon [26]. New parametrizations have been done with different focus such as amorphous, surfaces etc. [28; 29], as well as parametrizations for different materials [30; 31].

Alongside with the Tersoff form [32], the Stillinger-Weber form is still widely used for molecular dynamics simulations of silicon. Taking the gradient of the potential energy formula U gives us a way to calculate the forces with the atomic positions (Eq. (1)).

2.1.3 Thermodynamics

While the interatomic potential handles the interactions between atoms in a system, we also need some way to control temperature and temperature changes as realistically as is computationally sensible for a given problem. The thermodynamic ensemble of the system tells us the conditions of the system with regard to the external environment and how the macroscopic thermodynamic observables are derived from the microstate configurations of the system. Different ensembles are often called based on the three primary fixed variables of the given system. They can range from completely isolated to open. The simplest case is the isolated system where the amount of particles N, volume V, and energy E stay fixed (microcanonical ensemble, NVE). When the system is in thermal equilibrium with an external heat bath, we consider the canonical ensemble (NVT, where T is temperature). One can also control pressure p of a system via a barostat. NpT-ensemble is an ensemble related to situations with constant applied pressure. Thermostats are the part of molecular dynamics code in charge of the temperature control. Different thermostats have been developed for temperature control with differing capabilities on how well they reproduce an ensemble and how accurately they handle the dynamics of the system. Since the growth process is a temperature sensitive process, proper temperature control is key for the simulations. [24]

The simplest way for temperature control is via temperature scaling. By comparing the kinetic energy of the system at a given time step to the average kinetic energy of atoms at the target temperature, we can find a scaling factor. When the velocities of the atoms are updated based on the interatomic forces, we also modify them with the scaling factor. Such a method can be used for quick temperature changes, but overall it provides a fairly unrealistic simulation of temperature.

Another set of thermostat methods are the stochastic methods, which target the velocities of the Maxwell-Boltzmann distribution by modifying velocities of randomly chosen atoms. Since these methods introduce random, artificial disturbances to the atoms, they are unable to accurately sample dynamical properties of the system making them unsuitable for accurately investigating transport related phenomena like diffusion. [33; 34]

One of the most used thermostats is the Nosé–Hoover. Unlike many methods in computational physics, it is one of the more accurate/reliable temperature control methods but it does not come with a significant computational load compared to other methods. It allows for deterministic handling of temperature control unlike

the stochastic methods and it correctly samples the canonical ensemble (NVT). It belongs to a class of thermostats called extended system thermostats. Extended referring to the addition of an additional fictional "particle" with which the real particles in the simulation can exchange energy. Interaction with the heat bath (the fictional extension) can slow "too fast" atoms or give them energy to target the desired temperature. Modified versions of the equations of motion (velocity Verlet algorithm in Equations (2)–(5)) are derived for the extended system.

$$\mathbf{F} - \zeta m\mathbf{v} = m\mathbf{a} \tag{9}$$

$$\frac{d\zeta}{dt} = \frac{1}{Q}(K - \frac{3N+1}{2}kT) \tag{10}$$

The friction term ζ tells how much to modify the system. It depends on the difference between the total kinetic energy K of the system and the energy at the target temperature T given by the equipartition theorem ($\frac{3N}{2}kT$ from atoms plus the additional degree of freedom from the extension). Q is the "mass" of the fictitious particle. It is an adjustable parameter, which tells how strongly the thermostat should move the system towards the desired temperature. Choosing too low and high values lead to unphysical behavior. [24; 35; 36]

One of the most common methods for thermostating in molecular dynamics is with multiple chained extension variables with different "masses" (Nosé–Hoover chains). These chains eliminate problems encountered with small systems using a single variable Nosé–Hoover. Nosé–Hoover chains provide a deterministic, time-reversible and reliable way of controlling temperature in molecular dynamics simulations. [37]

2.1.4 Growth simulations

To investigate the growth of polysilicon, molecular dynamics deposition simulations were done. The outline of the deposition simulation is the following: a long simulation cell is initiated with enough space to contain the deposited pillar up to the target growth height. At the very bottom, an initial growth substrate is placed. The first few atom layers are locked in place to lock in the substrate. New atoms are introduced into the system from the top of the simulation cell at a given frequency and given a (mostly) downward velocity. This simulates a physical growth process and as such it should be noted that it differs slightly from the silane-based chemical process as outlined in Section 1.1.3.

The first step in forming the simulation setup was the choice of potential. There are a large collection of easily available potentials for silicon to use with LAMMPS: The Stillinger-Weber, multiple parametrization of the Tersoff, EDIP, as well as several machine learning potentials. Initial testing for bulk properties (such as lattice

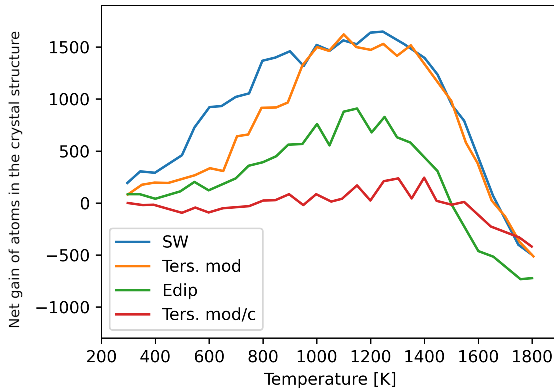


Figure 7. Deposition test for four of the chosen test potentials on how well the given potential handles the epitaxial growth of the crystalline structure. The vertical axis shows the change in the number of Si atoms in the crystalline phase at the end of the simulation compared to that at the beginning of the simulation. This was tested at various temperatures from room temperature to around the melting point. Stillinger-Weber and the modified Tersoff produce best growth of crystalline silicon, while the Tersoff modified version c shows very little growth. The different potentials peak at similar temperatures and as the temperature gets close to melting, we see reduced amount of atoms in the crystalline structure as atoms from the initial substrate are disturbed from the crystal structure due to the high temperatures. The melting temperature of the Edip-potential is several hundred Kelvin below the predicted values of the other potentials, which results in it dropping at a lower temperature.

parameters and elastic constants) and literature review cut down the number of candidates. First deposition tests were done on single-crystalline substrate with four candidates (shown in Fig. 7).

Stillinger-Weber was ultimately chosen. It should be noted that these classical interatomic potentials are all limited in their accuracy and using a different potential will potentially produce different results. However, more accurate methods are not suitable for these growth simulations. In a comparative study of different interatomic potential, Stillinger-Weber was found to handle different defects decently [38]. Since our focus is on the grain boundaries, this gives some support for the resulting data obtained with the Stillinger-Weber potential.

The key parameters in the deposition simulations are: simulation cell size (deposition area), deposition rate, initial velocity of the deposited atoms and growth temperature. Initial scan for suitable parameter ranges was done by deposition onto pre-made polysilicon substrate.

To investigate the limitations imposed by simulation cell sizes and to find suitable parameters, test simulations were done with different deposit rates (Δt) and surface areas (A). The resulting crystallinity was estimated at the end of the deposition. Fig. 8 shows the data points and a fitted surface. While at large enough simulation cells flux ($\Phi = \frac{1}{\Delta t A}$) is the determining factor for resulting crystallinity (as is ex-

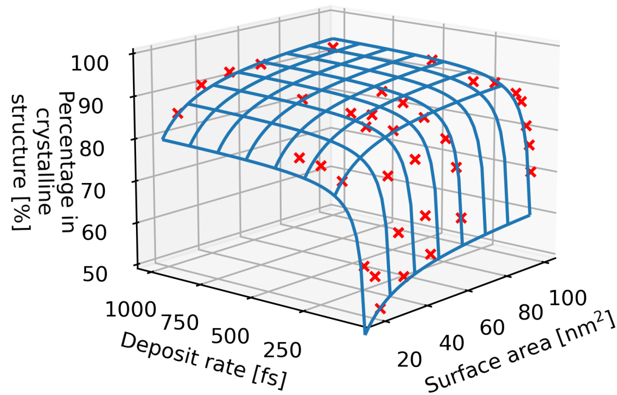


Figure 8. Resulting crystallinity percentage after deposition at different deposit rates to different surface areas (size of the simulation cells). Red crosses mark the data points and the blue surface is fitted to them. At larger simulation cell sizes, flux largely determines the resulting growth. However, at small simulation cells, deposition rate and surface area become independent variables. Care is needed to find a large enough cell with the consideration that larger cell sizes result in heavier calculations.

pected) but with smaller cells same flux produced different results. Reasons for this behavior are investigated in publication III.

It should be noted here that the cell sizes of computationally reasonable simulations will be smaller than the typical average grain size in polysilicon, and the resulting polysilicon film will be much thinner. This limits our growth simulation investigations to the very start of the polysilicon growth. From it, we are able to analyze the initial formation of the polylayer as well as the important part of polysilicon for this work, the grain boundaries.

Velocity and temperature scans were done next. These provided a range in which to operate. Temperature test showed similar polygrowth over the range 800-1100 K and simulations outside this range were found to less ideal when the goal is to grow polysilicon.

After suitable parameter ranges were established, the final problem was to grow polycrystalline silicon from non-poly substrates. Growing polycrystalline silicon from a crystalline surface proved to be a difficult task. In growth done on single-crystal silicon surface, the deposited silicon atoms diffusing on the surface will end up in the energetically favorable sites formed by the underlying crystal structure. Given good parameters for growth, the result is epitaxial growth of the existing single-crystalline structure. In real-world growth, the surface can never be as clean as in the simulation, whether it be in terms of oxygen or silicon defects. [3]

By depositing silicon onto a single-crystalline layer with a thin amorphous surface layer on top, eventually with good parameters some crystalline pockets start to form, which end up then developing into full polycrystalline structures. This ended up as the simulation setup used for the publication. The initial substrate consists of a partly locked-in-place single-crystalline base (around 10 Å) with an amorphous layer (around 15 Å) on top of it. Realistic amorphous silicon can be generated by melt and quench at cooling rates below 10^{11} K/s [39]. A block of desired size is first melted by running the simulation at temperatures above the melting point and then cooled. The obtained amorphous block was joined to on top of the single-crystalline block. The cell is then relaxed by energy minimization to more properly "join" the two blocks. This cell was then used for investigating the growth process of polysilicon. The findings and the final simulation setups with parameters are detailed in the first publication [40].

2.1.5 Identifying structures

Important part in the analysis of the simulations is to distinguish the crystalline and non-crystalline parts (grain and grain boundary). For this, a structural identification algorithm was used. Common neighbor analysis (CNA) is a commonly used method. Categorization of an atom works by looking if atom pairs are bonded based on their interatomic distance, which is compared to a cut-off distance. The cut-off distance is dependent on the structure type (and the material). For example for FCC it is the radial distance to the midpoint between the first-nearest neighbor shell and the second-nearest shell. Based on amount of shared neighbors, total number of bonds in the local neighborhood and length of longest bond chains between common neighbors, a local bond environment fingerprint is calculated. The fingerprint can be compared to the known environment fingerprints and the atom can be categorized based on the recognized structure or lack thereof. However, even with the improved implementations of CNA with adaptive cutoffs, the cutoff based methods have trouble with for example thermal vibrations and strain. [41]

Another approach to structural identification is the polyhedral template matching (PTM). It attempts to solve problems relating to CNA. While ideally all atoms on the same "neighborhood level" (nearest neighbors, second nearest, etc.) should be the same distance away from the central atom, thermal and strain related displacements complicate matters. PTM works by forming a set of n (number dependent on structure type) relative positions of the neighbors of the central target atom. The smallest possible polyhedron containing this entire set of neighbor atoms is constructed with tetrahedrons. The constructed polyhedron is compared to reference polyhedra with root mean square deviation (RMSD). If a matching reference polyhedron is found and the match is high enough (RMSD is chosen tolerance), the atom gets categorized as belonging to that structure type. An additional benefit of PTM is that it also

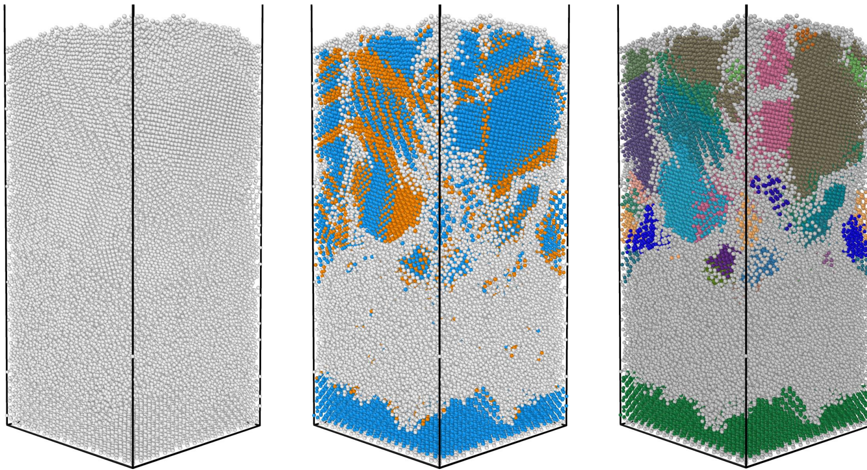


Figure 9. An example of structural identification for a 10x10x20 nm^3 simulated polysilicon growth done at 900 K. On the left is the silicon block after the growth simulation. The polyhedral template matching algorithm is used to identify the local structural environment of each atom. This is shown in the middle box, with atoms in cubic diamond structure colored in blue and the hexagonal diamond is colored in orange. In the bottom of the box, we can see the initial single-crystalline substrate on which the growth is done. On top of it is the amorphous layer, which develops into crystalline pockets and ultimately to the polysilicon layer. Local lattice orientation is also calculated for each atom with which we can cluster similar atoms to highlight the different grains in the box. This is shown in the box on the right, where each color represents a grain.

provides a way of calculating local lattice orientations, which can in turn be used to cluster similarly oriented atoms into groups, i.e., we can also identify grains. Fig. 9 shows an example of structure identification for a simulated polysilicon growth. [42] Most of the identifications of this work have been done with polyhedral template matching but common neighbor analysis was used for some quick preliminary scans, since it is significantly faster.

For the electronic states that are responsible for the carrier trapping, we need to focus on the miscoordinations, since perfectly ordered crystalline silicon doesn't produce these. For the more detailed and granular analysis of the local structures found near and in the grain boundaries, a method called SOAP (smooth overlap of atomic positions) can be used. SOAP is a descriptor of local atomic environments. It considers a local atomic density represented with Gaussians centered on the atomic positions. A basis set of spherical harmonics and radial basis functions is formed and used to form an expansion of the atomic density. Using the coefficients, one can create a descriptor (called the power spectrum) of the local atomic environment that is invariant to rotation. [43] With SOAP analysis, we can identify different, prevalent miscoordination environments from the simulations that could be further investigated using more accurate methods such as density functional theory.

2.2 Density functional theory

The key to mitigating the parasitic losses with polysilicon are the trap states. While with molecular dynamics and the growth simulations we are able to estimate the amount of miscoordinated atoms, structural types of miscoordinations etc., they do not give us any insight on the electronic properties of these, which is essential in figuring out the trapping properties.

The program used for investigating electronic properties is VASP. It is a first-principles (ab initio) quantum mechanical calculation program. Ab initio/first-principles meaning that the desired calculated properties of the system are derived from theoretical formulas and basic details such as atom positions. This is in comparison to methods leaning on empirically inspired/fitted approaches, such as the interatomic potentials used in the classical molecular dynamics calculations of LAMMPS (Section 2.1). While the added complexity of ab initio quantum mechanical calculations bring significant computational intensity, the added accuracy is necessary for determining the electronic states of a system.

2.2.1 Density functional theory

The electronic state of a system is given by electron wave functions Ψ. The wave function is given by the Schrödinger equation, which is a partial differential equation of the following (time-independent) form

$$\hat{H}\mathbf{\Psi} = E\mathbf{\Psi} \tag{11}$$

$$(\hat{T} + \hat{V}_{ei} + \hat{V}_{ee} + \hat{E}_{ii})\mathbf{\Psi} = E\mathbf{\Psi}, \tag{12}$$

where the Hamiltonian operator $\hat{H}$ of the system consists of kinetic energy $\hat{T}$, electron-nucleus interaction $\hat{V}_{ei}$, electron-electron interaction $\hat{V}_{ee}$ and nucleus-nucleus interaction $\hat{E}_{ii}$ parts. E is the energy of the system.

Solving the electronic state for systems beyond the simplest of cases proves to be not possible. The many-body problem encountered in many places is also present here. A proper quantum mechanical system contains a large amount of electrons, which all affect each other in a complex web of correlated interactions.

Density functional theory (DFT) approaches the solving of electronic properties of the many-body system differently. Instead of the electron wave function, we work with electron densities and functionals of the densities. The foundational theoretical work by Hohenberg and Kohn [44] proved some very important core theorems of DFT. It was proven that all properties of a system are uniquely determined by the ground state electron density $n_0(\mathbf{r})$ and that there is a functional for energy $E[n(\mathbf{r})]$, which alone is enough to determine the ground state density and energy. Despite huge effort such an exact functional has not been formulated and therefore exact density functional theory cannot be used for practical calculations.

The key approach in making density functional calculations practical and the widely used tool in materials science is the Kohn-Sham approach (Eqs. (13)–(15)) [45]. Instead of solving a system of many interacting electrons, we shift to a system of non-interacting electrons in an effective potential V_{eff}.

$$E_{KS} = T[n(\mathbf{r})] + \int V_{ext}(\mathbf{r})n(\mathbf{r})d\mathbf{r} + E_{cl}[n(\mathbf{r})] + E_{xc}[n(\mathbf{r})] \quad (13)$$

$$V_{eff}(\mathbf{r}) = V_{ext}(\mathbf{r}) + V_{cl}[n(\mathbf{r})] + V_{xc}[n(\mathbf{r})] \quad (14)$$

$$\left(\hat{T} + V_{eff}(\mathbf{r})\right)\psi_i(\mathbf{r}) = \varepsilon_i\psi_i(\mathbf{r}) \quad (15)$$

Total energy functional of the Kohn-Sham system is shown in Eq. (13). It consists of kinetic energy T, interaction with external potential V_{ext}, classical electrostatic interaction E_{cl}, and the exchange-correlation E_{xc}. From it, we can derive the effective Kohn-Sham potential V_{eff} Eq. (14), which in turn is used in the Kohn-Sham equations (Eq. (15)). They are a set Schrödinger-like (Eq. (11)) one-electron eigenvalue equations. We solve the equations for the Kohn-Sham orbitals ψ_i and their energy eigenvalues ε_i. The solving is done in an iterative loop, where an input electron density is used to calculate the effective potential V_{eff}, the K-S orbitals ψ_i and the energies ε_i. Output density is obtained from the squared magnitudes of the K-S orbitals. The iteration is considered converged when the input and output electron densities match to a desired level (self-consistent). The converged ground state density can then be used to calculate the energy of the system, forces, density of electronic states, and other useful quantities.

With this Kohn-Sham system, we can exactly handle the kinetic energy part T, interaction with an external field V_{ext} (electron-nucleus) and the classical electrostatic part E_{cl}/V_{cl}. The remaining problem is the exchange-correlation E_{xc}/V_{xc}, which contains the troubling many-body effects of electron exchange and correlation. The major upside of the formulation is that the remaining exchange-correlation part is often nearly local in nature. This has allowed for useful and widely used approximate forms to be constructed (such as local density approximation (LDA) and generalized gradient approximation (GGA)) and made it the tool of choice when accurate atomic calculations are needed. [46]

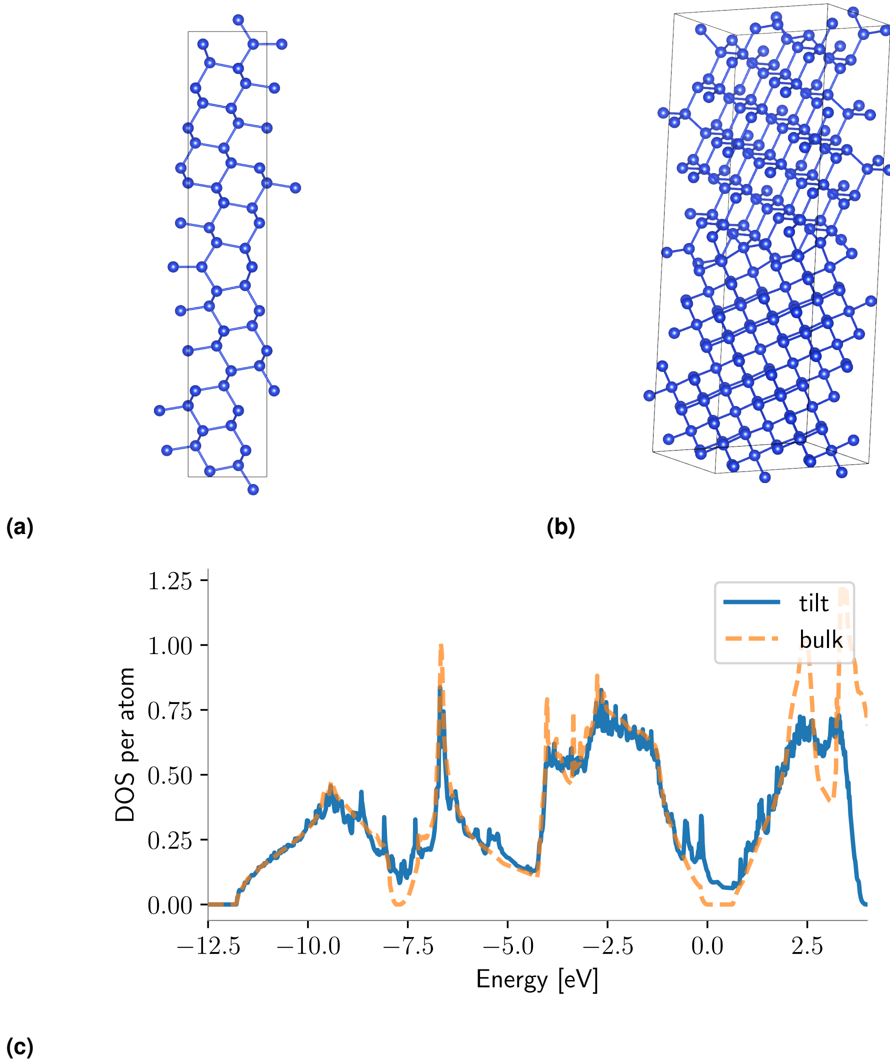
2.2.2 Electronic properties of grain boundaries

The main purpose of the VASP calculations in this work is to establish connections between identified structural types and corresponding electronic states, especially the trapping states found in the band gap. The problem is how to transfer the structural types found in the growth simulations to periodic VASP cells and then analyze electronic structure to make the connection.

Rataphan et al. [47] collected a table of commonly found grain boundary types in polysilicon with their prevalence and boundary energies. This provides a starting point. Periodic cells containing these grain boundary types can be generated using Aimsgb [48], which is a Python library for generating the atomic coordinates for a periodic grain boundary system given its grain crystal structures, degree of fit Σ (discussed in Section 1.1.4), boundary plane and axis.

An example calculation is shown in Fig. 10. It features a periodic cell containing a $\Sigma 11$ tilt grain boundary with a (3,-1,1) grain boundary plane. The generated positions are first relaxed. The density of states of the relaxed structure is calculated. The resulting density of states shows that the grain boundary has introduced electronic states in the band gap, which would mean that this particular grain boundary type could a desirable type for trapping the parasitic charge and therefore mitigating losses.

Another consideration is how to link the environments analyzed with SOAP (as discussed shortly in Section 2.1.5) with the electronic states that they produce. To keep the project (Fig. 6) on schedule and due to the large number of DFT calculations required to obtain a statistically reliable polysilicon trap density (as discussed in the next section), a model trap density from the literature [17; 49; 50] was used instead.



(c)

Figure 10. a.) shows an example of a grain boundary type found in polysilicon ($\Sigma 11$ tilt with a (3,-1,1) boundary plane) as a periodic grain boundary model of 44 atoms generated with Aimsgb [48] after relaxation with VASP. The box features two grains with grain boundaries in the middle and at the periodic top/bottom. b.) shows the box replicated along the two horizontal unit cell axes to better show the boundary. c.) shows the calculated density of states of a.) in blue. The orange shows density of states of bulk silicon for comparison. The density of states shows that the grain boundary has introduced electronic states into the band gap (energy from 0 to around 0.7 eV).

3 Devices under the influence of the fixed oxide charge

Referring back to the simulation chain Fig. 6, the main output from the investigations of Chapter 2 used as an input here is the trapping states configuration of the polysilicon layer. To determine how the fixed oxide charge affects the performance of the device, we need to figure out I.) how the charge distributes in the substrate, how much gets trapped and how much is left free to downgrade device performance, II.) how the electric field penetrates into the substrate and interacts with the remaining free charges. The charge distribution is solved using a self-made iterative Poisson-based solver. Based on these results and theoretical modeling of polysilicon resistivity, we get a local resistivity depth profile, which can be used as input in device simulations. The simulations in turn give us information on how the signal of the device penetrates into the substrate and ultimately the loss characteristics of a device. This can be then used to test out different configurations with different polysilicon properties to find the optimal polysilicon to mitigate the parasitic substrate losses.

3.1 Iterative charge distribution solver

Calculation of the charge distribution is done for the simulation box shown in Fig. 11. The box is discretized into an evenly spaced computational grid. At the top, we have the oxide in the form of the positive fixed charge. The simulation box side-to-side goes from grain center to grain center, i.e., the width of the box is the average grain size of the polysilicon. At the center, we have the grain boundary, which contains the trapping states. The polysilicon layer has some thickness, after which we have the high resistivity silicon layer (HR-Si).

First, we set some initial guess charge distribution $\boldsymbol{\rho}_0$ into the system. We solve the discrete Poisson equation (Eq. (16)). Section 3.1.1 gives a short introduction how this is done. The solution gives us the band bending potential $\boldsymbol{V}_{bb}$ of a given step.

$$\nabla \cdot \varepsilon \nabla \boldsymbol{V}_{bb} = -\boldsymbol{\rho}_i \tag{16}$$

An example solution (in 1D) is shown in Fig. 12. The bands bend downwards due to the positive oxide charge and slowly return to the bulk state as we move further away from the fixed charge. Solution of the Poisson equation gives us this band

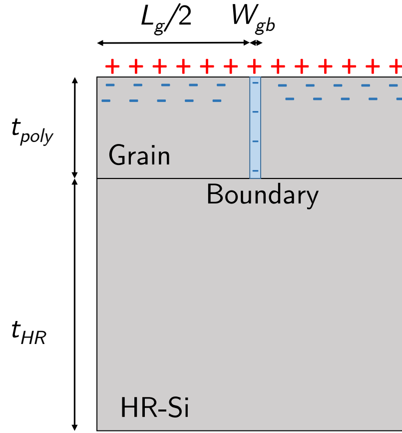


Figure 11. Simulation box for determining the charge distribution in the substrate under the influence of the fixed oxide charge. Configuration is determined by the grain size L_g, grain boundary width W_{gb}, thickness of the polylayer and the high-resistivity silicon layer t_{poly}, t_{HR}, amount of fixed oxide charge (marked with red plus signs) and trapping state density at the boundaries. The result from the calculation is the distribution of the compensating charge (marked with blue minus signs) whether it be trapped at the boundaries or as free carries.

bending for a given input charge distribution $\boldsymbol{\rho}_i^{inp}$. Based on it, we generate a new output charge distribution $\boldsymbol{\rho}_i^{out}$.

The charge distribution $\boldsymbol{\rho}_i^{out}$ for a given iteration step i is generated based on Eq. (17) for each grid point. The Fermi-Dirac distribution $f(E)$ tells us what is the probability of an electronic state at a given energy and temperature to be occupied. Density of states $g(E)$ tells us how many states are available for a given energy. Multiplying them gives us the density of electrons at a given energy level and to get the full density, we integrate over the energies.

Density of states g is dependent on the point in the simulation box. In the HR-Si, the density of states g_{Si} is given by Eq. (19), where g_C and g_V are the effective density of states for the valence and conduction bands (in eV$^{-3/2}$ cm^{-3}) and E_C, E_V are the energy levels of the bottom of the conduction band and the top of the valence band. [2] At the grain boundaries, we also have the gap states, which acts as trapping states. This density of states (g_t) is given by Eq. (20), where the trap states are exponential tails extending from the valence and conduction bands into the gap. $N_{t,A/D}$ gives the maximum density for acceptor (A) and donor type (D) traps respectively, $W_{t,A/D}$ tells how deeply the states extend to the gap.

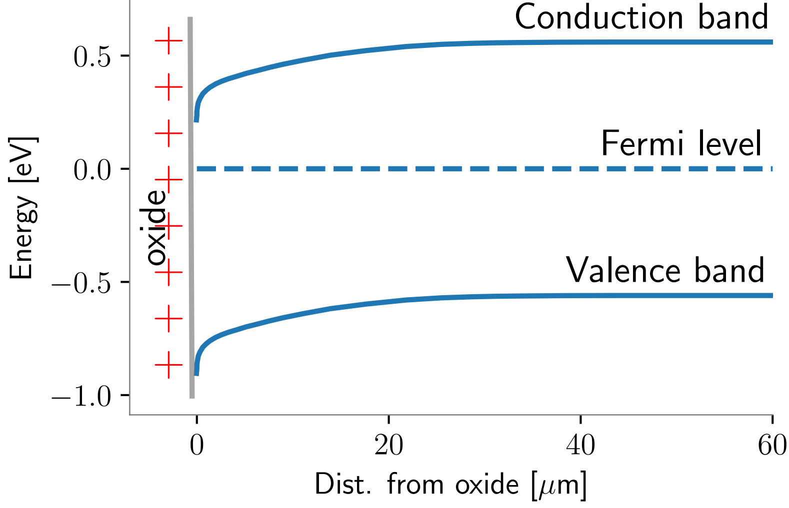


Figure 12. Band bending in the silicon substrate under the influence of the fixed positive oxide charge.

$$\rho_i^{out} = \int_E f(E)g(E)\,dE \tag{17}$$

$$f(E) = \left(\exp\left(\frac{E-E_F}{k_BT}\right)+1\right)^{-1} \tag{18}$$

$$g_{Si}(E) = \begin{cases} g_C\sqrt{E-E_C}, & E_C < E \\ 0, & E_V \leq E \leq E_C \\ g_V\sqrt{E_V-E}, & E < E_V \end{cases} \tag{19}$$

$$g_t(E) = N_{t,A}\exp\left(\frac{E-E_C}{W_{t,A}}\right) + N_{t,D}\exp\left(\frac{E_V-E}{W_{t,D}}\right), E_V < E < E_C \tag{20}$$

The total generated charge of $\boldsymbol{\rho}_i^{out}$ generated this way inevitably ends up not being equal magnitude to the positive oxide charge Q_{fo}. The system however should be neutral

$$|\boldsymbol{\rho}_i^{out}| = Q_{fo}.$$

To ensure this, we scale the generated charge distribution with scaling factor a_s

$$a_s = \frac{Q_{fo}}{|\boldsymbol{\rho}_i^{out}|}.$$

We ideally want the scaling factor to end up being $a_s = 1$ in converged calculations, which would mean that the calculation generates the physically correct amount of negative charge to compensate the fixed positive charge.

The basic idea of the process is to feed a charge distribution in, solve the Poisson equation and generate a new charge distribution, which we can again feed into the Poisson equation, iteratively improving the charge distribution. It is however practical to employ some sort of mixing to aid in convergence. Eq. (21) shows a simple linear mixing.

$$\boldsymbol{\rho}_{i+1}^{inp} = (1-\alpha)\boldsymbol{\rho}_i^{inp} + \alpha\boldsymbol{\rho}_i^{out} \tag{21}$$

In linear mixing, we choose some value $0 < \alpha < 1$, which tells us how much of the newly generated charge distribution to take when we mix it with the old one. More complicated mixing schemes, such as Pulay mixing [51] (also known as DIIS), can further aid in convergence (at least speed wise). It forms the new charge distribution from a linear combination of previous distributions, which are weighted based on their residuals $R_i^{\rho} = \boldsymbol{\rho}_i^{out} - \boldsymbol{\rho}_i^{inp}$.

The final step in the iteration loop is a convergence check. In this case, the potential is compared

$$R_i^V = |\boldsymbol{V}_i - \boldsymbol{V}_{i-1}|.$$

If the potential change R between iteration steps is below a set tolerance, we can stop the iteration.

3.1.1 Numerical methods for differential equations

Numerical solving of differential equations is a wide sub-field of countless applications. The following subsection goes shortly through how a problem, such as the Poisson equation (Eq. (22), in 2D), is put into a discrete form and solved using a computer.

$$\nabla^2 V = \frac{\delta^2 V}{\delta x^2} + \frac{\delta^2 V}{\delta y^2} = -\frac{\rho}{\varepsilon} \tag{22}$$

The first step is to approximate the derivatives. For a uniform grid spacing h, the approximate derivative is given by:

$$\frac{\delta^2 V(x)}{\delta x^2} + \frac{\delta^2 V(y)}{\delta y^2} \approx \frac{V(x+h) - 2V(x) + V(x-h)}{h^2} + \frac{V(y+h) - 2V(y) + V(y-h)}{h^2} \tag{23}$$

Since matrices are convenient with computers, the equation is put into matrix form. However, to complete the matrix, boundary conditions (BC) need to be handled. The simplest being the Dirichlet boundary, in which the value of V is fixed to

Figure 13. A 3x3 discrete grid with points indexed from 1 to 9 and a grid spacing of h. The approximate derivative at point 5 is given by the values at points 2,4,5,6 & 8 according to Eq. (23).

some value V_0 at the boundary points. One can establish finite difference formulas for points in the grid edges using forward/backward difference instead of the central difference of Eq. (23)). This way, we can also use the value of the derivative at the edge points as a boundary condition (Neumann BC). This could be used to, for example, ensuring that outgoing electric field is zero. By setting the value of the voltage to be the same at opposing edge points, one can also establish periodic boundary conditions. [52]

As an example, for a 3×3 grid indexed as shown in Fig. 13 using the Dirichlet boundary condition (voltage at boundary points is $V_{bc} = V_0$) and Eq. (23), the matrix becomes Eq. (24) with zeros omitted for visual clarity. Obviously a grid containing a single non-boundary point is hardly practical but using this approach it can be quite easily extended to larger grids, other boundary conditions, and to 3D.

$$\begin{pmatrix} 1 & & & & & & & & \\ & 1 & & & & & & & \\ & & 1 & & & & & & \\ & & & 1 & & & & & \\ 0 & 1/h^2 & 0 & 1/h^2 & -4/h^2 & 1/h^2 & 0 & 1/h^2 & 0 \\ & & & & & 1 & & & \\ & & & & & & 1 & & \\ & & & & & & & 1 & \\ & & & & & & & & 1 \end{pmatrix} \begin{pmatrix} V_0 \\ V_0 \\ V_0 \\ V_0 \\ V_5 \\ V_0 \\ V_0 \\ V_0 \\ V_0 \end{pmatrix} = -\frac{1}{\varepsilon} \begin{pmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \\ \rho_7 \\ \rho_8 \\ \rho_9 \end{pmatrix} \tag{24}$$

Once the matrix form has been established for the finite difference Laplacian and the charge distribution, the matrix equation can be solved to get the solution to the

Poisson equation.

$$\mathbf{Ax} = \mathbf{b},$$

where $\mathbf{A}$ is the discrete Laplace operator, $\mathbf{x}$ is the potential we are solving for and $\mathbf{b}$ is the charge distribution divided by permittivity of the material. For this type of matrix equation there exists a large amount of methods, such as LU-decomposition.

The initial testing was done with a finite difference solver but actual calculations for this work were done using FiPy [53], whose implementation differs from the presented but the basic ideas are the same: discretizing variables, forming discretized operators of the differential operators and solving the discretized equation. FiPy provides efficient Python-based tools for meshing, discretization and solving. Partial differential equation solving in FiPy is done with the finite volume method (FVM). An upside of finite volume over finite difference is the flexibility in the mesh. The mesh consists of a discrete amount of non-overlapping polyhedral cells with a cell center and edge nodes. The Poisson equation is written in the integral form by taking integrals (over a test volume) of Eq. (16). The right side is constant inside a given cell. The left side is substituted with the surface integral form by using Gauss's theorem. The left side can then be discretized to be the sum of the outward fluxes of all the edge nodes of a cell. Similarly to FD, we end up with a set of linear equations that can be easily solved by a computer to obtain the values at the mesh points. [54; 53]

3.1.2 Quantum correction for the charge distribution

In 2D materials and other such cases, the quantum nature becomes notable and the charge distribution differs from the classical. [55] While Schrödinger-Poisson solvers are used in different TCAD programs and different applications [56; 57], we desired a bit more simple approach than the full quantum mechanical one. To achieve this, our solved charge distribution can be corrected for quantum effects with an approach based on Thomas-Fermi equations [58; 59]. Instead of needing to bring wave functions and calculation of the Schrödinger equation (which needs to be done at every iteration) into the mix, we can operate with the potential V (from the Poisson equation) and the electron density n, which are something we operate with anyway.

$$\frac{d^2V^*}{dx^2} - \frac{\beta}{2}(\frac{dV^*}{dx})^2 = \frac{4m_e}{\beta\hbar^2}(V^* - V + \frac{1}{2\beta}) \tag{25}$$

Based on the Thomas-Fermi model, an equation (Eq. (25)) can be derived [60], which gives an effective potential V^* of an input potential V. m_e is the mass of the electron, $\beta = 1/kT$ with T being temperature and k is the Boltzmann constant, and $\hbar$ the reduced Planck constant. With the modified potential, we can generate the electron density as we did with the original potential, but now we approximately take

quantum effects into account. The effect of the quantum correction in our case was however fairly minimal.

3.2 Theoretical modeling of polysilicon resistivity

The basic idea of current transport in polysilicon is the following: trap states at the grain boundaries trap charge carriers. This depletes a part of the grain and reduces the amount of free charges that are available for current transport. The trapped charges form a potential barrier at the grain boundary, which impedes transport from one grain to the next. To contribute to current transport, the remaining free charge carriers need to overcome these barriers with high enough thermal energy or by tunneling through. Key variables determining resistivity in polysilicon are doping, grain size, temperature as well as the trapping state densities and energetics of the grain boundaries.

At low doping concentration, conductivity is low, since the amount of free charges is very limited. Medium doping range sees a very sharp increase in conductivity with increased doping. The largest changes are found around the point where traps are becoming fully filled. At high doping, the impact of the grain boundaries is reduced and the resistivity is close to similarly doped single-crystal silicon, albeit slightly higher due to scattering etc. Since the main impeding part is the grain boundary, with large grain sizes we approach resistivity values of single-crystal silicon. Small grain sizes feature relatively larger amount of grain boundary along the current transport path and thus larger resistivity. Naturally, higher temperatures provide more thermal energy for free charge carries, which aids in current transport. Impact of temperature and its importance in determining resistivity is linked with the potential barrier height. At low barrier heights, less thermal excitation would be needed to overcome the barrier. The trapping properties are the result of different structural miscoordinations of the grain boundaries and as such differently grown polysilicon will trap different amounts of charge. The amount of charge trapped mainly determines the height of the potential barrier and how much free charge is left in the grain to contribute to current transport. [3; 61]

3.2.1 Thermionic emission based models

The foundational work relating to the theoretical modeling of polysilicon resistivity was in large part laid by Seto in his 1975 work [61] on a thermionic emission model. Thermionic emission is considered to be the dominant mechanism for current transport in polysilicon at room temperature and above. While later works, for example by Lu et al. [62], have improved upon it, the basic idea of free charge carriers thermally overcoming the barrier (formed by the trapped charge carriers) has remained at the core. The process in the paper of Seto has been done with hole dominated polysil-

icon but the derivation works the same for electrons and since the parasitic surface conduction introduces electrons the considerations are done here with electrons in mind.

To obtain analytical formulas for polysilicon resistivity, we firstly have to separate the problem into two: a case where all of the grain has been depleted or a case where trap states become completely filled without full depletion. In the first case, the grain is fully depleted and the charge distribution is modeled with an even positive charge, whose magnitude is dependent on the doping concentration. The grain boundary is negatively charged with the corresponding amount of trapped electrons. We can solve for the potential barrier V_B with the Poisson equation. Solution for V_B becomes

$$V_B = \frac{qL_G^2 N}{8\varepsilon}, \tag{26}$$

where q is the elementary charge, L_G is the average grain size, N is the doping concentration and ε is the permittivity in silicon.

For current transport to occur, charge carriers need some way to overcome the barriers at grain boundaries. Drifting charge carriers thermally overcoming the barrier is the dominant mechanism at room temperature and above. Other mechanisms such as tunneling, thermally-assisted tunneling, trap-assisted tunneling and diffusion have not been considered in this model (their effect is discussed in Section 3.2.2).

To estimate the current density from grain center to grain center, the system is considered to be a symmetrical Schottky barrier [63]. Using the thermal emission theory for Schottky barriers, one can estimate the current density. The current density of thermal emission J_{te} (Eq. (27)) at a given temperature T is given by the amount of free charge carriers n left in the neutral region of the grain, the Richardson constant A (which describes the emission of a give material), and the grain boundary barrier V_B.

$$J_{te} = nAT^2 \exp\left(-\frac{qV_B}{kT}\right) \tag{27}$$

The net current density (Eq. (28)) in the polysilicon grain-boundary-grain system is given by the difference between the left-to-right and the right-to-left thermionic emission current densities for a given applied external voltage V_A.

$$J = nq\sqrt{\frac{kT}{2\pi m_e^*}} \exp\left(\frac{-qV_B}{kT}\right)\left(\exp\left(\frac{qV_A}{kT}\right) - \exp\left(\frac{-qV_A}{kT}\right)\right) \tag{28}$$

The parameters in the Richardson constant are elementary charge q, Boltzmann constant k, temperature T and the effective mass of electrons in silicon m_e^*.

If the applied voltage is small (relative to the thermal voltage kT/q), the current density formula can be simplified for a linear current-voltage relation, which allows us to estimate the overall resistivity (Eq. (29)) by Ohm's law.

$$\rho = \frac{V_A}{JL_G} = \frac{\sqrt{2\pi m_e^* kT}}{q^2 n L_G} \exp\left(\frac{-qV_B}{kT}\right) \tag{29}$$

Once the doping concentration is above a certain point (dependent on the trapping properties of the grain boundary), the traps become fully filled and only a part of the grain is depleted. Given the effective trapping density Q_t^* (given by the trapping density Q_t and probability of occupation at a given temperature T), the width of the depleted region W_d is estimated by ensuring charge neutrality between the negatively charged grain boundary of trapped electrons and the both sides of the boundary with positively charged regions depleted grain (which have doping concentration of N when undepleted)

$$2W_d N = Q_t^*$$

Similarly to the case with the fully depleted grains: the potential barrier height can be obtained from the Poisson equation, free charge left in the grain is estimated, thermionic emission current density is calculated and resistivity is obtained.

When comparing with experiments, the model produces too high current densities due to different factors (diffusion, lattice/impurity atom/grain boundary scattering etc.) that reduce the amount of free carriers that contribute to the net current transport [64]. Simple models typically employ the use of a scaling factor f to scale down the current density. Values of $f = 0.25$ [61], $f = 0.16$ [65] and $f = 0.06$ [62] are used. Each of the works establishes their models slightly differently, and approximations are made to obtain analytical forms. The models are designed at and for different variable ranges, handle the trapping states differently and try to match to different experimental data leading to difference in the factors.

3.2.2 Additional mechanism of current transport

The thermionic emission model is able to model resistivity of polysilicon well and it has been compared to experimental measurements of polysilicon resistivity over a varied range of doping concentrations, grain sizes and temperatures [61; 62]. Since the model also provides an analytical form, it works nicely for our needs. However, there remains a lot of considerations that contribute to the conductive properties of polysilicon, particularly in terms of providing more detailed physical understanding of the current transport (and removing the need for the scaling factor mentioned in the previous section). Fig. 14 illustrates some of these. In this subsection, I will present a short review of different mechanism and models [64; 66; 67; 68].

To obtain an analytical model, certain approximations are needed. These approximations come of course with a downside of limiting the applicability of the formulas to certain doping ranges, grain sizes, temperature ranges etc. Models that instead rely on iterative/numerical solving can have wider applicability [62].

After the thermionic emission based models had been established, one major goal was to get rid of the unphysical aspects such as the scaling factor f and obtain a model, which works with only physical inputs. Thermionic emission-diffusion models add the diffusion contribution to current transport by continuity equations. Several works [64; 66; 67] have derived a thermionic emission-drift model, which model the polysilicon resistivity and matches experimental measurements without needing the scaling factor. Such models also require numerical solving, unlike the analytical forms of the thermionic emission models. At lower potential barrier heights, thermionic emission remains the key mechanism. When the barrier is large, thermally overcoming the barrier becomes harder and the charge differences between the undepleted grain and depleted regions around the grain boundary become more significant. [64; 66; 67]

The mobility of charge carriers is lower in the grain boundary region compared to the bulk of the grain. This is in large part due to the potential barrier. The grain boundary can also contain a significant amount of scattering centers, which lower the mobility further. [64]

At low temperatures, few factors complicate matters. Reduced thermal energy naturally means that thermally overcoming the barrier becomes harder. Thermionic emission therefore decreases and the importance of tunneling becomes increased. However, another factor at play is the increase of unionized dopant atoms, which reduces the amount of charge carriers, both free and trapped. Increase in charge carriers with temperature means the height of the potential barrier increases with temperature. Tunneling current is found to be most significant relative to thermionic emission at around 150 K [69]. While thermionic emission is the most significant mechanism for the current transport, leaving these considerations out results in incorrect temperature dependence for the grain boundary limited carrier mobility. The model of Seto, for example, suggests that the dependence is positive but experimental data suggests that temperature dependence is quite weak to even negative [70].

Behavior of dopant atoms can be a significant consideration. Different dopant atoms produce different results. For example, arsenic doped polysilicon features higher resistivity than phosphorus doped polysilicon at similar doping levels. The source of the difference is in large part due to the segregation of dopant atoms to the grain boundaries: dopant atoms get trapped at grain boundaries passivating both dopant atoms and traps. The rates of segregation depend on dopant type and doping concentration. Our reference polysilicon samples, however, feature boron, which does not exhibit noticeable segregation [71] simplifying our modeling. Models incorporating dopant segregation have been established, which work to explain the dif-

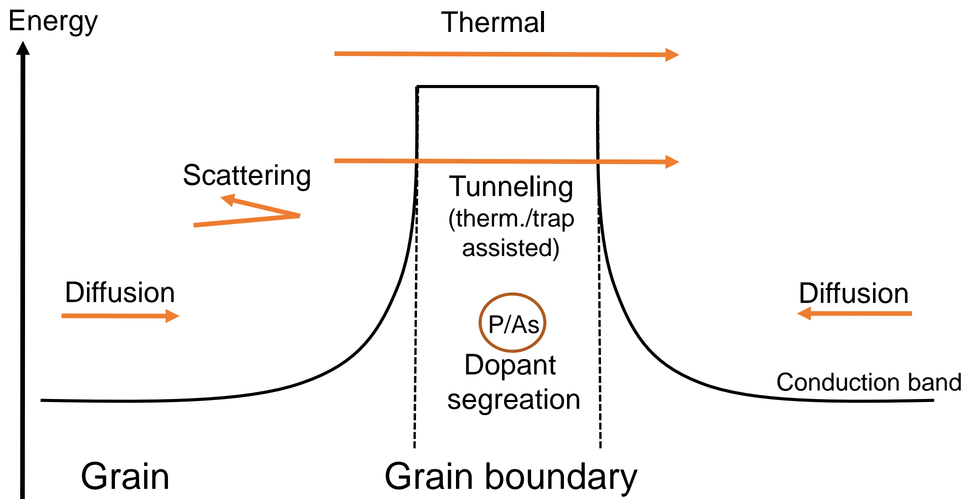


Figure 14. Different mechanisms relating to the current transport in polysilicon. The most dominant mechanism at room temperature is the thermal overcoming of the barrier in which electrons with high enough thermal energy can go over the boundary barrier to the next grain. Tunneling with or without the assistance of thermal energy and trap states is also present. On top of the net transport of electrons due to external fields, diffusion drives free electrons towards the depleted parts of the grain (near the grain boundary). Dopant atoms like phosphorus and arsenic segregate towards the grain boundary and become passivated. Grain boundaries also feature scattering sites.

ferences found in resistivity between different dopants and the impact of annealing [68].

The dynamics of the trapping process is often left out of considerations. The trapped charges however do have a lifetime associated with them. Thermionic emission model can be modified to take the rate of capture and the rate of release of the charges into account. [65].

3.3 Voronoi-SPICE for resistivity and grain size distributions

The established models of polysilicon resistivity are derived in 1D from grain center to grain boundary to grain center. In other words, the modeled polysilicon is of uniform grain size and shape. The grains are oriented so that the grain boundary is perpendicular to the direction of the current flow.

The resistivity of inhomogeneous materials has received plenty of attention, particularly through the different effective-medium approximations, which attempt to model macroscopic properties of composite materials through the properties of the

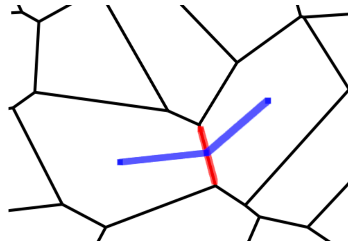


Figure 15. Zoomed in Voronoi diagram with an example of the relevant measures highlighted: grain size estimated from a grain center to the boundary center and to the next grain center (blue), and the grain boundary length (red). These are used to calculate the resistor values for a resistor network that established the connection between grain size distribution and resistivity.

components, their shape, ratio, etc. [72].

The present subproject aimed to investigate the effect of grain size variation and its impact on our polysilicon samples. This was done by extending the existing model with a computational grain structure, whose grain-to-grain connections can be modeled with resistors (resistive grain boundary). These can together form a resistor network, which when simulated gives the resistivity of the grain structure. This can then be compared to the 1D models with uniform grain size.

The process is the following: the grain size distribution of polysilicon is estimated from SEM images through manual segmentation and image analysis, Voronoi tesselation is used to model the grain structure with corresponding size distributions, individual connections between grains are analyzed (Fig. 15) and resistor values are calculated based on existing resistivity models for polysilicon and finally the resistors are connected to a network, whose overall resulting resistivity gives us the effect of the size distribution on resistivity.

3.3.1 Voronoi

Voronoi is a method of dividing a plane into regions [73]. It can be used as a mathematical representation of many different partitioned objects, such as the polycrystalline structure of the polysilicon. Voronoi is used here to generate mathematical polycrystalline structures with controllable grain size distribution.

Voronoi tesselation takes a set of points as input. Based on these points, the plane is divided into regions. Each point (seed point) generates a region. The division is done by expanding radially outward from the seed points. Once bordering regions meet, the expansion stops in that region. The expansion continues until the plane is filled. Mathematically expressing the same: a Voronoi region of a given seed point is a set of points, whose distance to the seed point is shorter than to any other seed points. The distance metric used commonly is the euclidean distance but other distance metrics can be used, which naturally produce different results.

Using a regularity parameter, we can produce Voronoi diagrams with different size distributions in a controlled manner [74] that are then used to form the resistor networks.

3.3.2 Grain size analysis

Grain size analysis of the samples was done based on SEM images of Si wafers with poly-Si film on top. Based on these, we can estimate the grain size distribution found on the surface of the sample. Since the polysilicon of our samples is columnar in nature, the size distribution remains fairly similar throughout large parts of the sample depth-wise. Samples of different poly-Si thicknesses provide a way to also give some estimation on the relation between depth in the sample and grain size distribution.

The analysis was done with Fiji [75], which is a scientific image analysis tool with wide extensibility and large amount of packaged image analysis tools. Since the amount of samples was small, it was still reasonable to manually perform the segmentation. This was done by drawing the outlines of the grains and calculating the areas based on the manually drawn image mask. Given the nature of the data, a log-normal distribution was then used for fitting. The fitted parameters can then be used to generate matching grain size distributions in with Voronoi tesselation. An example of the whole process is shown in Fig. 16.

3.3.3 SPICE

SPICE [76] is a widely used circuit simulator with many implementations. A Python interface PySpice [77] for Ngspice [78] is used in this work. SPICE contains the possibility to simulate a wide range of different components and device models. The networks created here are, however, simple resistor networks solvable through basic electrical laws, but to automatize the process and facilitate investigations with hundreds of grains, the circuit simulator is used to solve for the overall resistance.

3.4 Resistivity profiles

Since the ohmic losses from the parasitic charges is the problem under investigation, the local resistivity profile of the substrate provides a simple input for the device simulations. To produce resistivity profiles with different input configurations (trap states, polylayer thickness, grain size etc.), the charge distribution is determined as described in Section 3.1. It gives the amount of charge trapped, free charge remaining and the potential barrier as a function of distance from the oxide interface. These together with the modeling of polysilicon of resistivity (Section 3.2) allow us to estimate the resistivity profile. The profile can also incorporate the grain size distribution

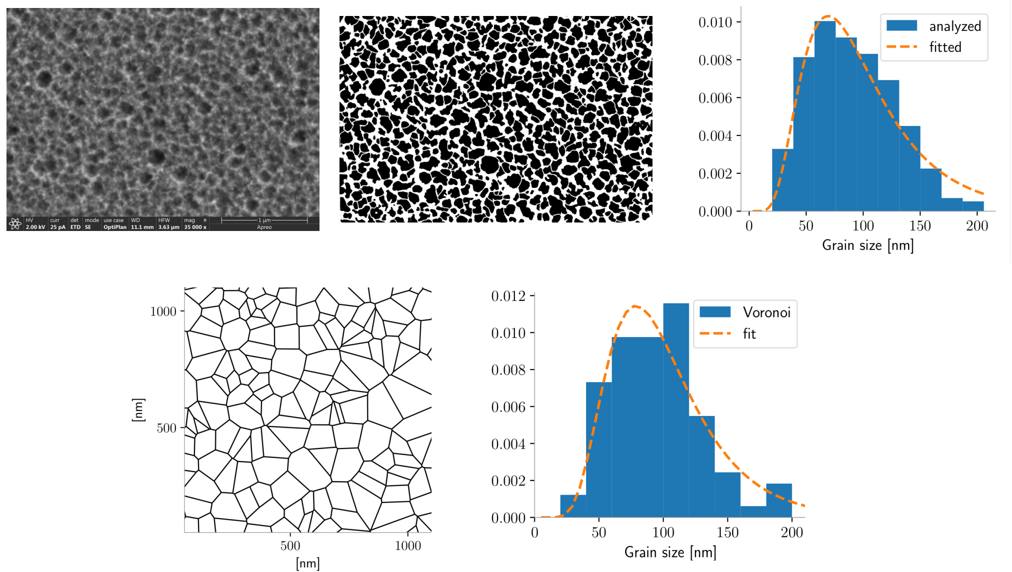


Figure 16. Top row shows the experimental side of the grain size analysis. Starting from the left: we have first the SEM image. The SEM image is manually cleaned for segmentation (middle top) and the grain sizes are analyzed. The resulting distribution is shown top right as the blue histogram. A log-normal distribution is fitted (orange, dashed). We target the parameters of the log-normal (in this case $\mu = 4.5$, $\sigma = 0.5$) with the generated Voronoi diagrams. A single example case is shown on the bottom left and bottom right shows the grain size distribution of the Voronoi diagram.

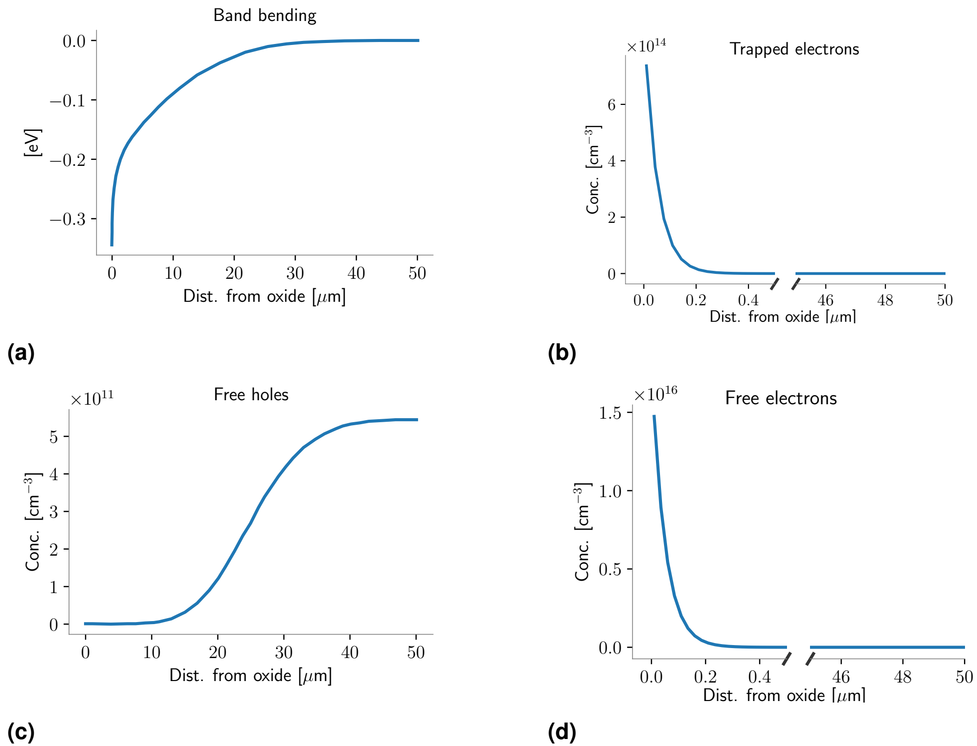
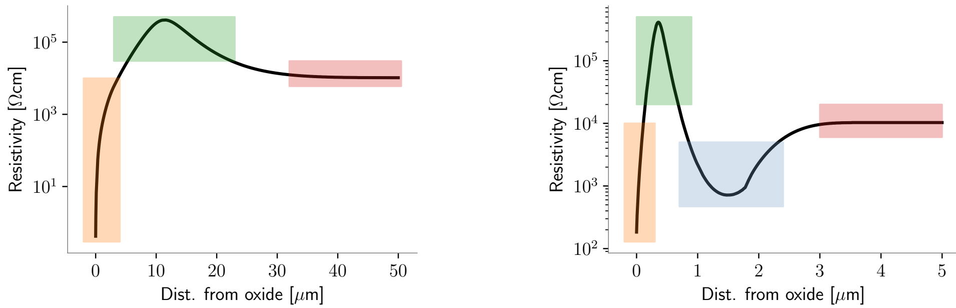


Figure 17. Different variables relating to the charge profile under the influence of the positive fixed oxide charge (in this case $Q_f = +10^{11}$ cm^{-2}), obtained as a function of distance from the interface. Fixed oxide charge bends bands (a.) and draws electrons towards the surface, some of which gets trapped (b.) and some remains free (d.). Holes deplete from the vicinity of the positive oxide charge (c.).

using the method outlined in Section 3.3.

As an example, for a positive oxide charge ($Q_f = 10^{11}$ cm^{-2}), the resulting band bending would be like in Fig. 17(a.). The electrons form a charge layer next to the interface to compensate for the positive charge. Depending on the trapping properties some of it is left free degrading device performance (Fig. 17(b. & d.)). The holes are repulsed away from the interface (Fig. 17(c.)). The depleted layer can extend several μm, while the electrons are concentrated largely within the first few hundred nanometers from the interface.

The resulting resistivity profile is shown in Fig. 18a. In this example, there is still a significant amount of free charge left in the grains, which results in a sharp dip in resistivity near the interface. Moving away from the interface, we have a region with very few charges for conduction, since the electron concentration is localized closer to the interface and holes have drifted further away. Finally, after some twenty or so micrometers the hole concentration returns to normal and gives the nominal



(a) **(b)**

Figure 18. a.) An example of the resulting resistivity profile calculated from the charge profile shown in Fig. 17. The configuration features $N_t = 10^{17}$ cm^{-3}eV^{-1} and $W_t = 35$ meV for the traps (Eq. (20)) in the $2\,\mu\mathrm{m}$ of polysilicon (0 to $2\,\mu\mathrm{m}$ from the oxide), grain size of 100 nm, and boron concentration of $1.3 \cdot 10^{12}$ cm^{-3}. The highlighted orange region corresponds to the lowered resistivity due to the parasitic layer (free electrons), the green region shows the depleted region and in the red region the resistivity returns to the nominal value produced by the free holes (from light boron concentration). b.) Example with much higher trap state density leads to less dip in the parasitic layer (orange), green region once again is the depleted region. Configuration for this example is from [17]. The polysilicon layer thickness of $2\,\mu\mathrm{m}$ contains a lot of traps ($N_t = 2 \cdot 10^{22}$ cm^{-3}eV^{-1}) in the first micrometer and no traps in the second half. The boron concentration is higher in the polylayer ($1.4 \cdot 10^{14}$ cm^{-3}), which leads to the dip in the blue region, from which the resistivity returns to the nominal resistivity (red) of the high resistivity silicon (10 kΩcm, impurity atom concentration $1.3 \cdot 10^{12}$ cm^{-3}).

resistivity of the high-resistivity silicon layer, in this case 10 kΩcm.

The resistivity profile is strongly dependent on the configuration (trap state density and depth distribution, polysilicon layer thickness, dopant distribution, fixed oxide charge magnitude, etc.). To highlight this, another example is shown in Fig. 18b calculated using the configuration from [17]. The resulting resistivity profile is very different for the same positive fixed oxide charge magnitude.

3.5 Device simulations

Final step in the simulation chain: to examine the real world measurable problem (the substrate loss), we need to see how the substrates and their resistivity profiles perform when a waveguide is built on top of them and high frequency signal is sent through the signal guide. For this, device-level simulations are done. The program used for these calculations is openEMS [79]. It is a 3D electromagnetic field solver, which uses the finite difference time domain method for solving discretized Maxwell's equations for small-signals.

The goal here is to set up a coplanar waveguide (CPW) simulation, calculate the resistivity profiles of different poly-Si films, use the profiles to define the substrate in the CPW simulation and obtain the S-parameters, which give the loss profile of a given configuration.

3.5.1 RF and the coplanar waveguide

Radio frequency (RF) refers to high frequency alternating current (mega-gigahertz region). It is a field of research distinct from direct current and low frequency alternating current devices with unique considerations. RF-devices built on silicon substrates are at the heart of wireless communication. Therefore, the goal is to make sure that the substrate is the best it can be. RF-engineering is a wide field with considerations unique to it. In this work, we do not go very deep into the RF side, but we need some way to estimate the loss, when a given substrate configuration is used. For this, we need to consider the waveguide.

Waveguides are structures that are used to efficiently transmit signals by guiding the wave in the given direction incurring ideally as little loss as possible on the way. A simple waveguide is the microstrip line. It features a stack of a ground and a signal guide separated by a dielectric. The coplanar waveguide instead places two ground strips on top on both sides of the signal guide. This helps to contain the signal, which is particularly useful in compact devices, where the coupling of nearby components can affect device performance. [80] An illustration of an CPW structure can be found in Fig. 20. The relevant parameters shown in the figure are discussed in Section 3.5.4.

3.5.2 Losses in coplanar waveguides

There are several types of losses encountered with CPWs. Firstly, the non-ideal CPW contains a metal signal guide, whose conductivity is finite. Due to the resistance of the metal, some loss to heat is inevitable (ohmic conductor loss). Another consideration with metals is the so-called skin effect. When an AC-signal is applied, the current density in the metal tends to concentrate near the surface. This reduces the effective area of conduction, thus increasing resistance. The depth decreases as the signal frequency increases. The effect is dependent on the material. [81]

The response of the dielectric also differs from the ideal case and results in losses. The permittivity of a dielectric is a key measure in how a material responds to an electric field. While permittivity is often treated as constant, more accurate, particularly with higher frequencies, is to represent it as a frequency-dependent complex variable (Eq. (30)).

$$\varepsilon(\omega) = \varepsilon'(\omega) - i\varepsilon''(\omega) \tag{30}$$

$$\tan\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'} \tag{31}$$

The real part ε' is the measure of how well the material stores electromagnetic energy. The imaginary part ε'' is related to the conversion of the electromagnetic energy to other forms of energy, mainly heat, during different polarization processes. It is therefore also sometimes called the loss factor. The permittivity has a complicated frequency dependence as different mechanism of polarization such as dipolar, atomic and electronic operate differently at different frequency ranges [82].

The loss tangent $\tan\delta$ in (Eq. (31)) is the ratio between the lossy part and the lossless part of the permittivity. The loss tangent is often presented in material datasheets as a measure of the expected dielectric loss for a given material when used in a transmission line. Besides the mechanisms outlined above, the dielectric still has some, albeit low, conductivity, which contributes to losses in the dielectric (σ in Eq. (31)).

Radiation losses can also be a source of losses but its contribution is often quite insignificant compared to the other sources. This radiation can also produce interference in other components nearby, which has an adverse effect on the signal. This interference is commonly called crosstalk.

Finally, the loss process, which is the focus of this work, is the ohmic loss process in the substrate. Due to the parasitic surface layer (Section 1.3) there is an increased large amount of free charges available. With high enough frequencies, the electric field penetrates through the dielectric and “wiggles” the free charges. When the parasitic surface layer is present, the substrate ohmic losses can become a quite significant source of losses.

Since in AC-circuits we are dealing with waves with magnitudes, phases, their reflections etc., the input-output behavior is more complicated than in a simple DC circuit. We need a convenient way to characterize devices. Scattering parameters (S-parameters) are one commonly used way for this and a lot of properties of a device can be calculated from its measured S-parameters. A simple two-port setup would feature an input port and an output port, which gives us a 2×2 S-matrix. S_{11}, the reflection coefficient, would give the reflected wave in relation to the inputted wave at the input port. S_{21} would be given by applying a wave at port one and measuring how much of it makes to be measured at port 2. This provides the insertion loss, how much loss occurred because of the device between the ports. When measured in a range of frequencies, it gives us the loss profile of the device. The losses are often given in dB following Eq. (32). [83]

$$L_{in} = 20 \log_{10} |S_{21}| \text{ dB} \tag{32}$$

S-parameters are something we can both simulate with the device simulations and measure experimentally. This provides a direct comparison to real world measurements. Fig. 19 shows an example of an investigation of losses with different trap state densities. Highest overall resistivity is found with the case of highest trap state density, since the amount of free charges is reduced most by trapping. The bottom figure shows that this then corresponds to the least amount of losses. Reducing trap state density lowers resistivity, particularly in the region nearest to the interface, which introduces more losses. This type of approach can be used to test different configurations of the substrate to optimize it for reduction of losses.

3.5.3 Finite difference time domain

OpenEMS [79] simulates devices using the finite difference time domain (FDTD) method. As outlined in Section 3.1.1, a commonly used way of solving different problems is the finite difference method. Here instead of the Poisson equation, Maxwell's equations are solved on a discrete grid with derivatives in the equations replaced with discretized finite difference forms. Now we have an additional dimension in time. Partial derivatives with respect to time are also handled with the finite differences.

The method relies on the so-called Yee algorithm: on a discrete spatial grid and a discrete time, the Maxwell's equations are formulated into update equations using the finite difference approach. For a given node, first the magnetic field H at time step $t + \frac{\Delta}{2}$ is solved using the known previous magnetic field of the node at $t - \frac{\Delta}{2}$ and neighboring node electric field values at t with the finite difference Faraday's law. Electric field is then updated to $t + 1$ with the neighboring magnetic field values and electric field value of the node at t with the finite difference Ampere's law.

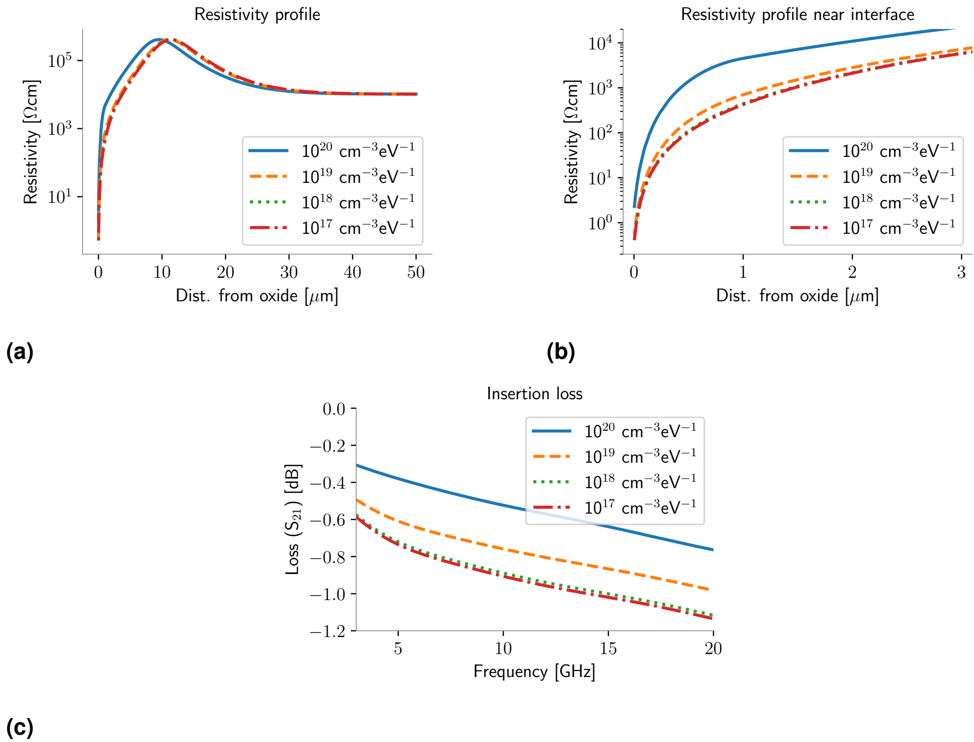


Figure 19. As an example investigation: the effect of different trap state densities is shown. Different colors and values in the legend correspond to the maximum value of the density ($N_{t,A}, N_{t,D}$ in Eq. (20)) of an exponential conduction and valence band tail distribution. Resistivity profiles are shown in the top figures, with the left being the entire simulated depth and right zoomed to the crucial area within the immediate vicinity of the interface. The bottom shows the resulting loss (S_{21}) as a function of frequency.

Since the method only considers the nearest neighbors when calculating for a given node, the relation of the grid node distance (spatial step) and the time step is notably important. The field can ideally, at most, propagate one spatial step within a time step or else we might not produce sensible results. The Courant number S_c is key in this

$$S_c = \frac{c\Delta t}{\Delta x}. \tag{33}$$

The distance of propagation in relation to the node distance Δx is given by the speed of the electromagnetic wave c in a given material and time step Δt. For stability and accuracy, we want the Courant number below one. A convenient upside is that calculations can be done using the Courant number without explicitly declaring Δt or Δx. When a suitable pulse, such as a Gaussian, is introduced, one can obtain the response of the system over a large range of frequencies with only one simulation. [84; 85]

3.5.4 Simulation setup & parameters

Cross section of the device under simulation is shown in Fig. 20. It shows the key parameters. Firstly, the waveguide dimensions such as the width of the signal and ground guides and the spacing between them is vital information of the CPW. Oxide thickness is the thickness the electric field needs to penetrate to cause losses in the substrate. At high frequencies, the oxide cannot completely prevent the substrate loss problem, and increasing the thickness can introduce disadvantages, such as the cost and practicality of manufacturing thicker oxides, and increasing the size of a device.

For the substrate losses, we focus on the amount free charges left for conduction. In terms of these simulations, this is modelled with the resistivity profile (Section 3.4), which serves as the input to the device simulations. The continuous resistivity profile (function of depth) is used in the simulations with discretized and averaged curve placed into silicon blocks of different resistivities. On the substrate side, the key parameters are the trap state densities, grain size, thickness of the poly-layer and dopant concentration, which determine how this resistivity profile looks like for a given fixed oxide charge.

The magnitude of the fixed oxide charge is one of the inputs, which allows us to test different cases. This work has mostly dealt with silicon oxide, where the charge typically is in the order of $Q_f = +10^{11}$ cm^{-2}. Other oxide types also produce these fixed oxide charges. For example, Al_2O_3 would be negative in sign and often an order of magnitude larger than in silicon oxide [22].

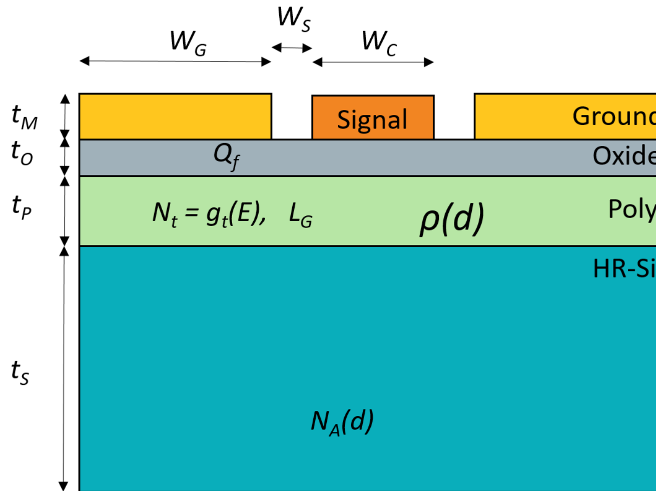


Figure 20. Coplanar waveguide under simulation. Relevant measures of the waveguide are the central signal guide width W_C, spacing W_S, width of the ground guides W_G, thickness of the metal guides t_M, thickness of the oxide t_O, polylayer thickness t_P and silicon substrate thickness t_S. Q_f is the amount of fixed charge at the oxide-substrate interface, which tells how much compensating charge is needed on the substrate side. The resistivity profile $\rho(d)$ of the substrate (poly+HR) is also dependent on the dopant concentration N_A, which in case of silicon-polysilicon can be depth dependent [86], the grain size L_G and the trapping state density of the polylayer $g_t(E)$.

3.5.5 Problems and further considerations with device-level simulations

Probably the most important note here is about the way that the substrate is modelled. The modelling behind the resistivity profiles is a steady-state DC model. It ignores potential mechanisms involved when dealing with alternating signal.

At higher frequencies, the “reaction time” of a charge carrier is too slow to react to the quickly changing signal. As Rack et al. investigated [15], the amount of compensating charge in the first micrometer depth from the interface remains fairly constant at the gigahertz region (the relevant region for this work) but at lower frequencies the amount of compensating charge changes quite noticeably during one period of the wave signal.

Lifetime of trapping is also a consideration that could warrant investigation. Particularly when combined with the consideration noted in the first paragraph. How much does the distribution of trapped charges change when the external field drives free charges deeper into the substrate, where more traps are left unfilled, and how likely are they to stay trapped there when the field changes direction?

4 Summary of publications

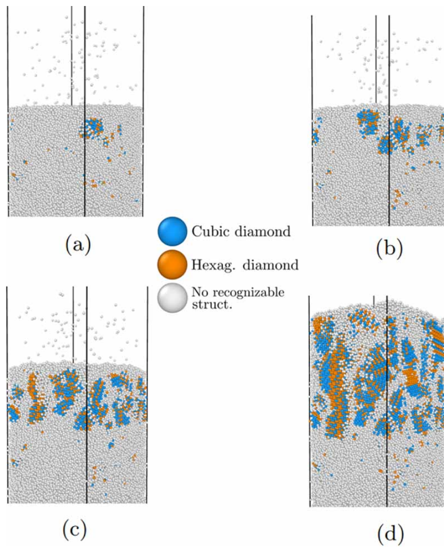
The first three publications deal with the atomic side of this work (Chapter 2). In the fourth one, we move to electronic properties (Sections 3.2 and 3.3). While the overall goal is to create a multi-scale computational framework, due to the lack of experimental data suitable for comparison and validation and time constraints, the following publications do not cover resistivity profiling and device simulations. For the sake of completeness, these topics are discussed in the introductory sections of the dissertation. (Sections 3.1, 3.4 and 3.5).

4.1 Growth simulations

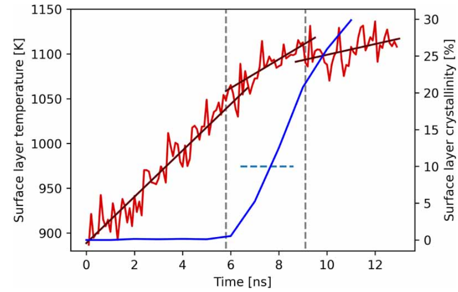
In the first publication [40], we present the work related to the deposition simulations of polysilicon. The practical considerations on setting up the simulations are covered such as the choosing the interatomic potential (Stillinger-Weber) and the important parameters. Parameter scans for suitable value ranges were done to choose temperatures, cell sizes and deposition rates. Potentially most interesting out of this was the test on the flux of the deposited atoms, which provided data that was analyzed further later in Publication 3 (Section 4.3). A suitable simulation substrate for the actual growth simulations was developed: a single-crystalline layer with the few bottom-most atom layers fixed and a thin amorphous silicon layer on top of it.

With the presented simulation setup we investigate the growth process by depositing silicon atoms on to the described substrate at the chosen parameter ranges. Particularly, the focus is on the initial formation of the polystructure (Fig. 21a). This is supported with a nucleation investigation using single-crystalline seed cores in an amorphous medium, which is shortly compared to classical nucleation theory. The key here is the threshold radius of the nuclei beyond, which the nuclei tend to develop further and below which they tend to decay.

To provide further explanation on why the polysilicon develops the way it does and to explain some found structures, we also further investigate the temperature and its distribution in the silicon bulk during growth. The analysis of the data provides us with details on how the temperature distribution and changes in it relates to the different growth stages we observed during the simulations (Fig. 21b).



(a). Formation of the polysilicon layer during the deposition simulation.



(b). Development of the average temperature at top most 2 nm during the growth in red. Blue shows the crystallinity degree in the same block. The figure is divided into three to highlight three different stages of growth.

Figure 21. Figures from Publication I [40] (licensed under CC-BY-4.0).

4.2 Analysis of simulated polystructures

The focus in the second publication [87] shifts to investigating the resulting simulation boxes after the deposition has finished. Polyhedral template matching is used to structurally analyze the simulation data of simulated polylayers grown at different temperatures. The grain size distribution is investigated both before and after simulated heat treatment. We see an increase in grain size after heat treatment, particularly for the larger grains. The orientations of the grains are investigated from polyhedral template matching data as well and compared to experimental XRD results. The comparison shows similar results but there are some differences, for which potential explanations are discussed.

Since the key part in mitigating parasitic surface charges are the grain boundaries and their miscoordinations, a lot of focus has been put on the analysis of the boundaries. Firstly, the thickness of boundaries are investigated and how the distributions of boundary thickness behave as function of depth in the polysilicon layer.

Finally, using the local atomic environment descriptor SOAP, the amount/density of the most common miscoordinations (3- and 5-bonded silicon atoms) are investigated for different growth simulation parameters (Fig. 22). This is particularly interesting for us, since these miscoordinated atoms are the primary source of the desired trapping states at grain boundaries, which can be used to mitigate the parasitic surface charge.

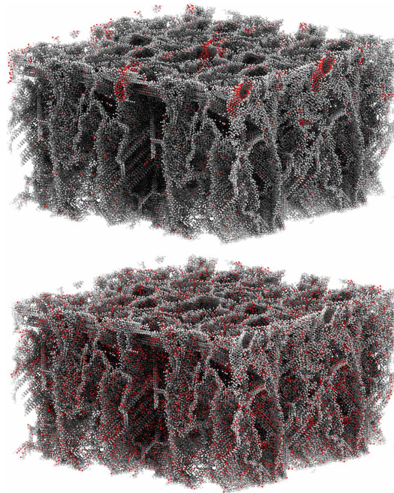


Figure 22. The local atomic environment analysis of our largest simulation cell (400 nm^2) allows us to highlight the three-bonded (top) and five-bonded (bottom) silicon atoms. These miscoordinated atoms are largely responsible for the electronic states in the gap that trap the parasitic charges. Figure from Publication II [87] (licensed under CC-BY-4.0).

4.3 Flux and the physical interpretation of the simulation data

The third publication [88] continues on the analysis of the simulated polysilicon films. Here, we investigate and present models to interpret the results of an investigation relating to the flux (presented in the first publication) and its components: deposit rate and the surface area onto which the deposition is done. 36 simulations were done with the different parameter values and a physically meaningful model is derived with surface diffusion physics, which can provide further understanding of the polysilicon growth. It also serves as a practical guide to more controllably produce desired polysilicon structures (Fig. 23) and guide the selection of growth parameters in simulations, particularly in terms of the resulting crystallinity degree (ratio of atoms in crystalline structure to total number of atoms) of the polylayer.

The resulting structure depends largely on how well atoms can diffuse on the surface to energetically favorable sites. Given too dense flux, other atoms disturb the diffusion. With probability analysis of the adsorption events, a model with two fittable parameters (Δt_0, A_0) is developed to estimate the relation of the surface area A, the interval between deposited atoms Δt and the crystallinity degree r_{pc}. The simulation data is to fit the two parameters. The physical meaning of the two fitted parameters is explained, which provides further understanding of our simulated polysilicon growth and provides a simple way to choose suitable parameters for obtaining desired polysilicon in simulations.

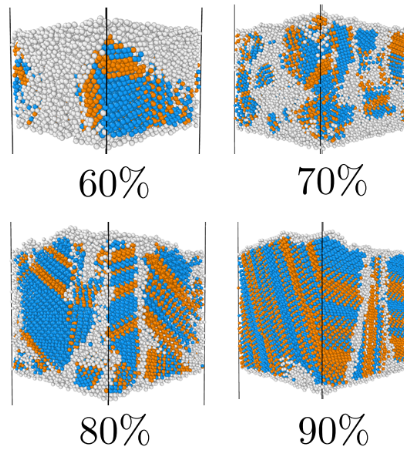


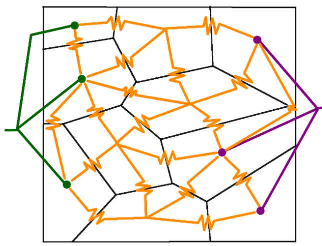
Figure 23. The crystallinity degree of the simulated polysilicon can be controlled by the deposition parameters. Our model provides a way to select suitable values to produce desired polysilicon. Figure from Publication III [88] (licensed under CC-BY-4.0.).

4.4 Resistivity model extension

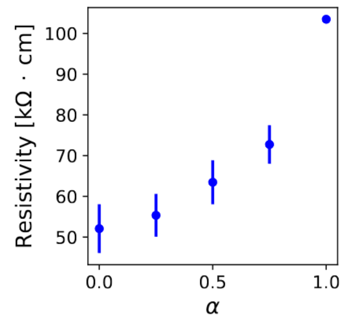
We have analyzed grain size distributions both from our simulations and from the real world polysilicon films. The question then became how does the grain size distribution affect the resistivity of polysilicon. In the fourth publication, an extension to existing resistivity models is introduced to incorporate the grain size distribution.

Using a controlled Voronoi tesselation, we form diagrams with size distributions corresponding to our grain size distribution data. We then form resistor networks with these diagrams, whose resistances for the grain-to-grain connections can be calculated from the existing one-dimensional resistivity models. The resulting resistor network (Fig. 24a) is simulated with the circuit simulator SPICE, which gives us the 2D grain size distribution dependent resistivity.

The effect of grain size distribution on resistivity is investigated with the presented Voronoi-SPICE using different test size distributions (resistivity as a function of the width of the grain size distribution log-normal peak, Fig. 24b) and at different doping concentrations to highlight the increasing impact of the grain boundary barrier as more charges get trapped there at higher doping concentrations. We also investigate the effect with our experimental and simulated grain size distributions.



(a). A generated Voronoi diagram is used to represent the grain structure. A resistor network is used to estimate the effect of the grain size distribution on polysilicon resistivity.



(b). Resistivity as a function of the width of the grain size distribution (controlled with the Voronoi regularity parameter α). Wide distributions (low α) can feature less than half of the resistivity of the polysilicon with uniform grain size ($\alpha = 1$).

Figure 24. Figures from Publication IV [89].

5 Conclusions

This dissertation has collected our work on how to mitigate the increasing losses encountered with the high frequencies of RF devices. A phenomenon called parasitic surface conduction, where the fixed oxide charges in the oxide next to the silicon interface causes free carriers to collect near to the interface, is at the core of the investigations. Leaking electric fields then causes ohmic losses in the silicon substrate.

We have established a multiscale simulation setup, which has been illustrated in Fig. 6 as a flowchart and in the graphical conclusion (Fig. 25). Starting from the atomic-scale simulations we have investigated the growth of polysilicon layers, how different parameters affect the growth and provided models, investigations, and explanations on how a certain type of polysilicon layer is formed. We also have focused on the resulting structures and particularly grain boundaries, which provide trapping states for the otherwise free parasitic charges. Our analysis of the simulations has provided us with the densities of these miscoordinated structures. Trapping states are given by the connection between the structural defects and miscoordinations and the resulting electronic states they produce. We have done preliminary investigations on these. We supplement these with existing grain boundary trap state models from literature.

For a configuration (trapping state density, fixed oxide charge magnitude, doping concentration, polylayer thickness, grain size distribution, etc.), we investigate how the parasitic charge is distributed in the substrate using a specifically developed iterative Poisson solver. Based on the distribution of the charge (together with basic substrate properties) and theoretical resistivity model of (poly)silicon, we can calculate the resistivity profile of the substrate under the influence of the fixed oxide charge. The resistivity profile provides an input to our device simulations, which then gives us the losses of the given configuration. This has allowed us to test different parameters and how well they mitigate the losses.

My personal focus was at first the molecular dynamics simulations of growth. These provided us with plenty of data to analyze the growth of polysilicon and the resulting structures. Publications I-III are largely based on this simulation data. After these, a large part of my work has been the modeling of the electrical properties of the substrate under the influence of the fixed oxide charge. From there, the notable highlights are the development and testing of the resistivity modeling program together with the extension of the resistivity model to incorporate grain size distri-

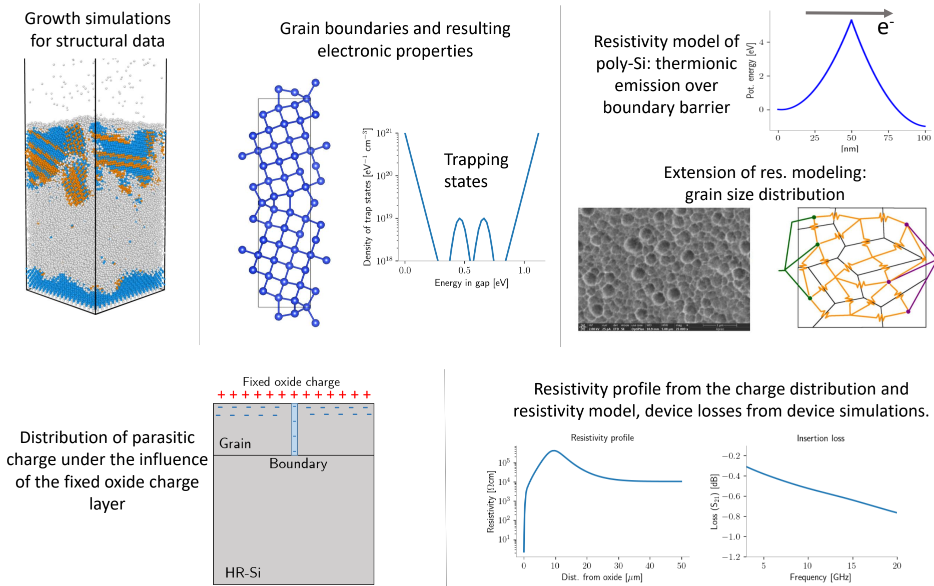


Figure 25. The subprojects of the multiscale simulation setup presented graphically. Fig. 6 shows how the subprojects work individually and how they link in to each other.

bution (publication IV), which give us the resistivity profile of the substrate under the influence of the fixed oxide charge. While not my primary focus, I also had the chance to look into the ab initio calculations and the device simulations.

Overall, each subproject has been quite well tested and we successfully can derive estimation of loss behavior starting from the atomic scale. The work was quite extensive in its scope, since we have investigated the problem all the way from the atomic to the actual device scale. Therefore, there were quite a lot of considerations that unfortunately were left out of the scope of this work. Section 3.5.5 has discussed some future improvements and further considerations specifically for the tail end of the simulation chain. As a more overall discussion of further studies, I would like to note a few.

The connection between different structural defects and their resulting electronic properties ended up as an incomplete investigation and we relied mostly on trapping state configurations examples found in literature as well as wide range of hypothetical test values. While different parts of the work have been compared with literature results and experimental data, we however need more work on the final parts of simulation chain. The device simulations that used the resistivity profiles of different configurations received some good verification with test cases from literature (Rack et al. [17] featured spreading resistance profiles and loss for few configurations) but we lacked the suitable experimental data to make a link between the experimental and the simulation for our polysilicon samples. Finally, the main achievement of

the work was in establishing the framework and the first iteration of the simulation chain. Practical investigations using the entire chain of methods were fairly limited. This work however provided many tools and skills for myself and the research group to continue on the problem.

List of References

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