Optimization of $Gd_{0.2}Ca_{0.8}MnO_3$-based capacitive memristors

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B.Sc. Anni Antola
Examiners:
Prof. Petriina Paturi
Dr. Hannu Huhtinen
Dr. Ilari Angervo

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Department of Physics and Astronomy

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After the time of miniaturizing transistors used in integrated circuits comes to an end, another computational method is likely to answer the ever-growing need for more computational power. One of the possible options for evolving past the traditional von Neumann architecture is neuromorphic, human brain-inspired, computing, based on the memory and data transfer properties of synapses and neurons. These two main components of the human brain can be artificially fabricated with different methods and materials. Memristors, short for memory resistors, have been proven to work both as synapses and neurons, making them an ideal component.

In this thesis I studied and optimized the fabrication process of $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) thin film capacitive memristive devices. The fabrication methods tested in this thesis were pulsed laser deposition, photolithography with etching, and electron beam deposition. Five iterations of samples with varying combinations of the fabrication methods for the three layered capacitive structure were studied. The characterization of the fabricated samples was done mainly with electrical transport measurements using ArC ONE (Memristor characterisation platform), with additional surface and material quality checks done with atomic force microscopy, scanning electron microscopy, and energy-dispersive spectroscopy.

The measurement results showed some memristive properties, for example, accessible high resistance and low resistance states, for the final fabricated device. As the difference in resistance value between these two states was found to be much smaller than what has been measured for a planar GCMO memristor, some optimization is still left to do on the fabrication process of the capacitive structure. Also, the device-to-device variation was high.

Manganite oxide memristors have been widely studied in relation to the possibility of working as a synapse or a neuron. For example, for PCMO, both planar and capacitive memristors have been researched. As no measurement results for GCMO-based memristors with capacitive structures have been published previously, it was crucial to find out whether capacitive GCMO possesses the same properties as its planar counterpart. A new, capacitive structure could advance the usability of GCMO as a component for future neuromorphic applications, and deepen the knowledge of the memristive properties of the material.

Keywords: GCMO, memristor, resistive switching, neuromorphic, thin film, capacitive

Contents

Introduction

Moore's Law, i.e., doubling of the number of integrated circuit (IC) transistors biyearly, was an observation of Gordon Moore in 1965 [1]. The so-called law was proven to be quite accurate up until the 2000s when the advancements and progress started to slow down below the predicted pace. The achievable improvements of complementary metal-oxide-semiconductor field-effect transistors (CMOS) are coming to an end due to the scaling limitations of the technology. Even the now disbanded ITRS (International Technology Roadmap for Semiconductors) predicted that transistor scaling will come to an end in the 2020s, stating also: "Moore's Law is dead, long live Moore's Law" [2]. The possible advancements after Moore's law are not tied to the development of smaller transistors anymore, as the future is somewhat unknown territory filled with promising developmental branches, e.g., ICs done with 3D technology of stacked transistors (3D Power Scaling) [2].

According to ITRS, memory technologies have been and will be the driving force behind Moore's Law [2]. One promising direction for future development is manganite-based memristive materials used as a basis for memory devices. Memristors, short for memory resistors, are usually metal-oxide-metal junctions possessing the property of resistive switching, rapid and significant resistance changes due to applied voltage pulses. Memristive devices are able to retain the achieved resistance, i.e., the changed energy region of the interface of the oxide and the active metal. Memristors were first discussed in the 70s by L. Chua [3], but the research was limited to the theoretical existence of the component. The resurfacing of memristor research came in 2008 by the works of Yang *et al.* [4] and Strukov *et al.* [5], when physical devices were found to have memristive properties.

Memristors are found to behave like artificial synapses or neurons, making them the ideal component to create neural, brain-like, networks. At the moment, many different memristive materials, mainly transition metal oxides, are of interest, one

of them being $Gd_{1-x}Ca_xMnO_3$ [6]. Memristors can have different device geometries, for example planar (in-plane) or capacitive [7–9]. The topic of the thesis is to study and optimize the fabrication process of $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) -based capacitive memristors by characterizing the properties of the memristors made with varying combinations of fabrication methods. This will lay the foundation for further research.

1 Background

1.1 Neuromorphic computing and engineering

The need for more computational power is ever-growing, especially in the age of artificial intelligence and machine learning. Neuromorphic computing tries to solve the computational limits we are facing today and will face in the future with von Neumann computer architecture. A von Neumann computer is composed of a central processing unit (CPU) housing a processing unit and a control unit and an external memory unit [10]. This structure, with a shared bus for transferring data between the CPU and the memory unit, causes a narrow bottleneck for the data. The computational power is limited, as the data has to be fetched from the memory to the CPU and returned back after usage. The bottleneck will reach a so-called memory wall, an exponentially growing gap in the rate of improvement of the processing and memory speeds [11].

Increasingly in recent years, the developmental focus has shifted in multiple different directions, one of which is neuromorphic engineering, to answer the ever-growing need for high efficiency computing that requires minimal power consumption. Neuromorphic engineering tries to bring to life the needed hardware of neuromorphic computing. As the name suggests, neuromorphic engineering and computing close in on the problem at hand by mimicking the behavior and structures

present in the human brain, which has superior computing power and less power consumption compared to von Neumann architecture. [12, 13]

Brain-like structures need to have at least the two repeating fundamental units: neurons and synapses. Neurons are responsible for the processing of the informational signal, as synapses cover the transmission of the signals between the neurons. The neurons can be said to be the processing unit, and synapses the memory, both key computational components neatly combined. For a neuromorphic computer to work, it needs to have some basic properties, e.g., neural behavior replicating a biological neuron and synaptic spiking time dependent plasticity (STDP). [12, 13]

The initial combination of the metal-oxide-semiconductor (CMOS) technology with artificial neural circuits was a developmental success, a starting point for further evolution. The first completely fabricated neuromorphic circuit was made with metal-oxide-semiconductor field-effect transistors (MOSFETs). After that, there have been a variety of materials and novel devices used for fabricating the components needed for neural circuits. These novel neuromorphic devices are mostly based on memory cells or devices, for example memristors. Memristors have shown promising properties to function as a part or neural circuits, e.g., they have low power consumption and high endurance, and their memory properties are non-volatile. This is an improvement compared to CMOS-based neural circuits, which require multiple transistors to replicate a single neuron and a constant supply of power to retain the memory. [12–16]

1.2 Capacitive structure and materials

1.2.1 Capacitive structure

Neuromorphic engineering and computing are highly linked to materials science, as we want to travel from fully simulated devices and circuits to physical hardware made out of optimized materials. Memristors can be based on different geometries

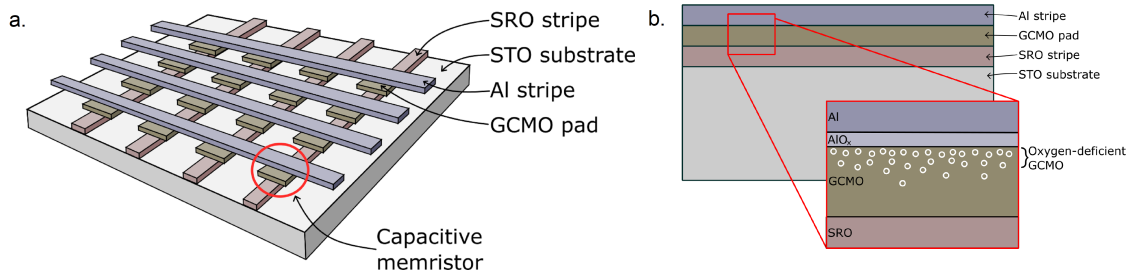

Figure 1. a. Illustration of a capacitive memristor grid structure with STO as the substrate, SRO and aluminum stripes as the electrodes, and GCMO pads as the memristive material. b. Schematic of the layer structure, with oxygen vacancies illustrated in the GCMO layer at the interface with the oxide layer in the aluminum. The thicknesses of the layers and widths of the patterns are not to scale.

for the primary structure. For example planar memristors are extensively studied in relation to their promising behavior as a base for a neuromorphic device [7, 17]. Another possible configuration for a memristor is a capacitive one, in some cases as a part of a memristive crossbar array [14, 18, 19]. More in-depth comparisons between the memristive properties of different materials and memristor geometries are left to Chapter 1.3.2.

In this thesis, we wanted to find out whether capacitive GCMO possesses the same memristive properties as it does with a planar configuration, and if so, can the fabrication process be optimized. The material properties of GCMO are discussed in more detail in Chapter 1.2.2.

Fig. 1 shows a schematic for the chosen geometry and layering of the materials for the memristor. A grid of 4×4 memristors (crossbar array) was chosen to give us more data to work with when characterizing the devices of the fabricated samples. The selected substrate was $SrTiO_3$ (STO), as it had been previously used successfully as a base for planar GCMO-based memristors due to having the same perovskite crystal structure [7]. $SrRuO_3$ (SRO) was utilized as the bottom electrode of the capacitive structure, because it has an epitaxial growth on top of the STO substrate [20], providing a good growth medium for the GCMO layer. SRO is a semiconductor

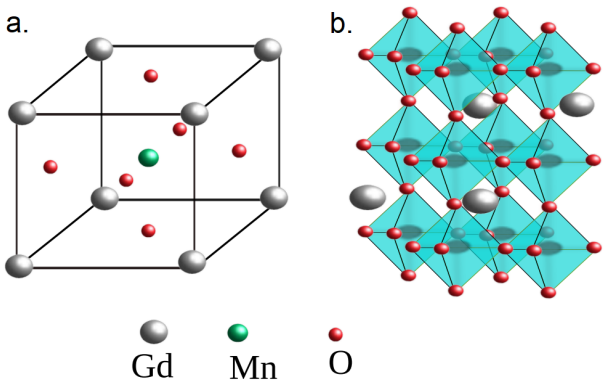

Figure 2. a. The ideal cubic structure for a GCMO, with atomic positions for Gd (or Ca), Mn and O. b. The oxygen octahedra enclosing the manganese centers within the perovskite structure. [23]

with a highly conductive, metallic-like, nature, and the characteristic resistance of a SRO thin film is known to be around 300 $\mu\Omega$cm [21]. For a thinner stripe of SRO the resistance is a bit higher due to a narrower path for the current. To ensure that the interface of SRO and GCMO is non-rectifying, both materials are of the same type of semiconductor (n-type). Aluminum (Al) was used for the top reactive electrode, as it creates an active interface with GCMO. The resistance of an Al thin film is also around 10^{-6} Ωcm [22]. An electrical connection through the GCMO layer occurs between the electrodes, as the voltage is applied through Al wires bonded to the SRO and Al stripes.

1.2.2 $Gd_{(1-x)}Ca_xMnO_3$

Gadolinium calcium manganite oxide, $Gd_{(1-x)}Ca_xMnO_3$ ($0 \leq x \leq 1$), with a concentration of $x = 0.8$ was chosen as the memristive material between the SRO and Al layers (Fig. 1b), because according to the research of Lähteenlahti *et al.* this concentration is amongst the most promising ones [7]. $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) is a mixed valence manganite oxide with a perovskite structure. GCMO, with the generalized structural formula of $R_{(1-x)}A_xMnO_3$, has a *Pbnm* symmetry unit cell, with corner-linked oxygen ion octahedral structures containing manganese ion centers and

Gd and Ca interlaced between the octahedra (Fig. 2). In the structure class, R is a lanthanoid cation, A is an alkaline earth cation, manganese is a cation, and oxygens are anions interacting with all cations [7, 23]. One unique aspect of transition metal oxides, a partly filled d shell, exists also in GCMO, causing fascinating spin and charge properties and orbital ordering [6].

The unit cell has a possibility of distorted oxygen octahedra typical to manganite lattices. This distortion, i.e., the ideal cubic structure changing either to orthorhombic or tetragonal, is caused by the small radius of the A or R cation (Gd or Ca) in comparison to the Mn cation. The tilting and deforming phenomenon is known as a Jahn-Teller effect, and it causes some interesting properties for the material, for example charge ordering [24]. Charge ordering signifies the phase transition, in which the charges are localized, resulting in, for example, a checkerboard-like ordered lattice and a high resistivity [25]. The amount of oxygen octahedra distortion is inversely proportional to the electron bandwidth, which in turn causes the temperature of magnetic ordering to decrease and the temperature of charge order to increase. The magnetic ordering of the Mn-ion in GCMO is antiferromagnetic most prominently at $x = 0.8$. At this concentration a magnetic cluster glass phase has also been found for Mn-ions, and as a whole, the bulk GCMO is mainly insulating [23].

For oxide materials, there are multiple different conduction models for describing the electrical current flow: Ohmic, space-charge limited, Poole-Frenkel, and Schottky conduction. For Ohmic conduction, the resistance of the material stays constant as the current flow is directly proportional to the applied voltage (linear conduction). If the space-charge of the material limits the current, like in many semiconductors, the type of conductivity is space-charge limited. The current flow is caused by the injection of electrons at an Ohmic contact, as electrons will move from the metal to the conduction band of the insulator forming a local space-charge

due to the accumulated charge. For space-charge limited conduction, quadratically proportional current to the applied voltage is typical. If the material in question is an insulator, Poole-Frenkel model is observed, as the Poole-Frenkel effect, i.e., the trap-assisted electron transport energy reduced due to being in an electric field, limits the current. Schottky-type conductivity is typical for interfaces between metals and semiconductors, as the current is limited by the Schottky effect, i.e., the barrier affecting current flow between a semiconductor and the metallic material. [26]

1.3 Resistive switching

1.3.1 Types of resistive switching

Resistive switching as a phenomenon is tightly tied to memristive thin films. The simplest explanation for resistive switching is that applying an electric field to the device terminals changes the resistance of the material non-volatilely, i.e., repeated modifications to the device conductivity are possible. An electric field can also be used to read the resistive state of the device non-destructively, if a small enough field amplitude and a suitable polarity are utilized. The phenomenon should not be confused with an electrical breakdown of an insulator: the insulator is incapable of recovering from the change in the conductance, when the insulator breaks down due to too high applied amplitude of voltage. [27]

Characteristic for resistive switching are the high resistance states (HRS) and low resistance states (LRS), caused by the higher and lower conductivity of the GCMO layer. The conductivity changes due to two main causes, resistive switching based on an electrochemical metallization (local phase change from insulating to metallic) and a valence change. Electrochemical metallization is more common for capacitive memristors than for those with a planar structure. When an electric field is applied, the amount of oxygen is reduced from the oxide material, resulting in a local metallization and a conducting filament between the electrodes. The HRS and

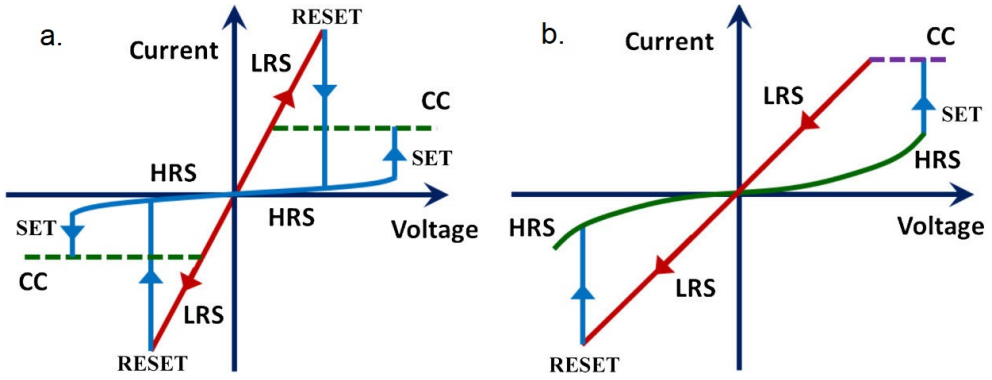

Figure 3. Characteristic IV curves with differentiated high and low resistance states (HRS and LRS) for a. Unipolar devices b. Bipolar devices. [29]

the LRS are accessed when the applied electric field is used to form, dissolve, and re-form the filament through the weakest percolation path between the electrodes. [27, 28]

In planar GCMO-based memristors, the switching mechanism is based on a valence change, i.e., the change in conductance comes from the migration of oxygen vacancies (or ions, depending on the semiconductor type) at the interface of the oxide and the reactive electrode. In a GCMO thin film with an Al-electrode, an AlO_x layer forms between the pure Al and GCMO and causes a depletion of oxygen from the GCMO near the interface. With an electric field, the conductance of the interface changes due to the oxygen ions moving back and forth between the oxygen-deficient GCMO and AlO_x. In Fig. 1b we can note the oxygen vacancies in the GCMO layer close to the AlO_x layer. The HRS corresponds to less conductive vacancies within the material, modulating the Schottky-like barrier properties at the interface. As no previous studies have been done on capacitive GCMO-based memristors, we cannot be completely certain on the exact mechanism behind the resistive switching, thus the assumption of a same, or similar, mechanism is the safest. It should also be considered that both presented switching mechanisms can occur simultaneously. [7, 27, 28]

The phenomenon can be divided into two categories, uni- and bipolar switching, based on whether the polarity of the electric field affects the device polarity or not. The characteristic IV-curves for both are presented in Fig. 3. Set and reset voltages, V_{set} and V_{reset}, are the voltages needed to switch between the HRS and the LRS. Unipolar switching occurs often with electrochemical metallization, and for it, V_{set} and V_{reset} have the same polarity (independent of field polarity), V_{set} being larger in amplitude. For switching the device from the LRS to the HRS, firstly the electric field is set to zero after which V_{reset} is applied. For switching back to the LRS, the electric field must be set to zero before V_{set} is applied. Bipolar switching happens with valence change-based switching, and it is more promising out of the two for neural applications due to better endurance and smaller power consumption. In bipolar devices, the resistance depends on the electric field amplitude and polarity. The HRS and the LRS are accessed by V_{set} and V_{reset}, which are of different polarities, usually V_{reset} being smaller in amplitude. Both uni- and bipolar switching can be achieved with an electric field applied using current instead of voltage pulses. [27, 28]

One key factor to look for when determining whether the device is uni- or bipolar is the changing of the device behavior in relation to the active interface area. Unipolar switching behavior should remain unchanged, as the filament growth does not depend on the area by much, but for bipolar switching, the valence change is highly dependent on the interface area. The type of switching can be permanently affected by a too-high applied electric field, changing the device from bipolar to unipolar. [27, 28]

1.3.2 Switching in memristive devices of different geometries

The two main variations for the device geometry are planar and capacitive. The basics of the capacitive structure, and the specifics of our version, have been discussed in Chapter 1.2.1. Planar structure is simply a thin film of memristive material,

for example a manganite, deposited on a suitable substrate, and electrical contacts from some non-active metal electrode and from the chosen active metal electrode deposited on the film. All of the components are located in one plane, i.e., the memristor is "two-dimensional". The interesting interface is once again between the active metal and the memristive thin film. [7]

Many different materials have been used for the fabrication of memristive devices, e.g., manganite oxides $Gd_{1-x}Ca_xMnO_3$, $Pr_{1-x}Ca_xMnO_3$, and $La_{1-x}Ca_xMnO_3$, all having the same general structural formula presented previously for GCMO. For example with $Pr_{1-x}Ca_xMnO_3$ (PCMO), both planar and capacitive memristors have been studied: Lähteenlahti *et al.* [17] examined PCMO (x = 0.4) with a planar structure, and Li *et al.* [18] studied resistive switching in PCMO (x = 0.3) capacitive structures. In both structures, Al was utilized as the active metal electrode. The usability and overall quality of the devices of those geometries were quite similar. Both exhibited bipolarity, even though both polarities have been noted for PCMO previously [30]. The behavior and resistive switching of the compared PCMO-based devices were similar: non-volatile and controllable, and both had accessible HRS and the LRS. The HRS and the LRS values were a bit higher for the capacitive configuration, but the value of the LRS compared to the HRS was about the same for both device configurations, the LRS being 0.1 % to 1 % of the value of the HRS. The difference between the states was at least a couple of orders of magnitude.

For GCMO, resistive switching has been previously studied only for planar geometry. For planar GCMO (x = 0.8) -based memristors, the switching was bipolar, according to Lähteenlahti *et al.* [7]. The difference between the LRS and the HRS was measured to be a couple of orders of magnitude, similarly as for PCMO. Reflecting the results of PCMO, the resistive switching should be bipolar also for capacitive GCMO-based memristors, at least if the samples are somewhat similarly fabricated and prepared. An example of an IV measurement done on a planar

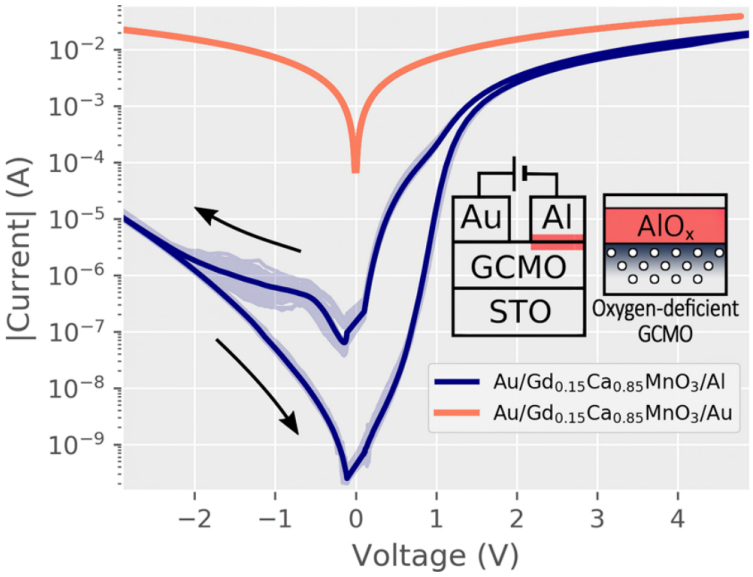

Figure 4. Characteristic IV curve of a planar GCMO (x = 0.85) -based memristor and the included schematic of the device layer structure [7].

GCMO (x = 0.85) -based memristor is shown in Fig. 4. The shape of the IV curve is highly asymmetric, and there is notable hysteresis especially around the zero voltage point.

The quality of memristive properties can be analyzed by using different variables. To determine whether a contact possesses the wanted memristive properties at all, and whether the quality of these properties is good enough, we selected three main criteria: the asymmetry of the measured IV curve, the general resistance level of the contact, and the ratio of the LRS and the HRS. The asymmetry, i.e., the different paths of the IV curve in the positive and negative voltage sides (including hysteresis of the curve), is a key indicator on the type of the polarity of the device. If the IV curve is highly asymmetrical, we can be quite certain that the device has the sought after bipolar tendencies, but in the case of more symmetrical IV curves, the division between uni- and bipolar is not as easy to make. The general resistance level of the contact must be high enough to reduce the risk of a sneak path forming. A sneak path, as the name suggests, is a meandering, lowest resistance path between two

points for the current to flow through. Especially for crossbar array configurations, these current detours are unwanted, as the path through the memristive device is left unused in the process [7]. The ratio of the LRS and the HRS is the last key factor in determining the memristive quality, as it sets the usable resistance range of the device. These chosen parameters will be kept in mind while conducting the measurements on the devices.

2 Fabrication methods

There are multiple different ways to fabricate a full thin film or a thin film pattern. Our goal is to optimize the fabrication of capacitive memory devices with three thin film layers. The fabrication methods explored within this thesis are pulsed laser deposition (PLD), electron beam evaporation (E-beam), photolithography and etching, and ultrasonic wire bonding. The following chapters will present the basics of each of the used methods.

2.1 Pulsed laser deposition (PLD)

Pulsed laser deposition (PLD) is a widely used physical vapor deposition technique for the fabrication of thin films. The general configuration of the method includes a high energy pulsed laser beam directed through a focusing lens to a vacuum chamber where it makes contact with the target. The laser vaporizes material from the target creating a plasma plume that hits the heated up substrate providing the substrate with a flux of material for continuous crystalline growth. If the deposition conditions are ideal for the deposited material, a crystallized epitaxial growth as a thin film is achieved on top of the substrate. Usually the process takes place in a vacuum, where an oxygen circulation is used when depositing oxides to make sure no oxygen is extracted from the deposited material via heating. By varying the energy density

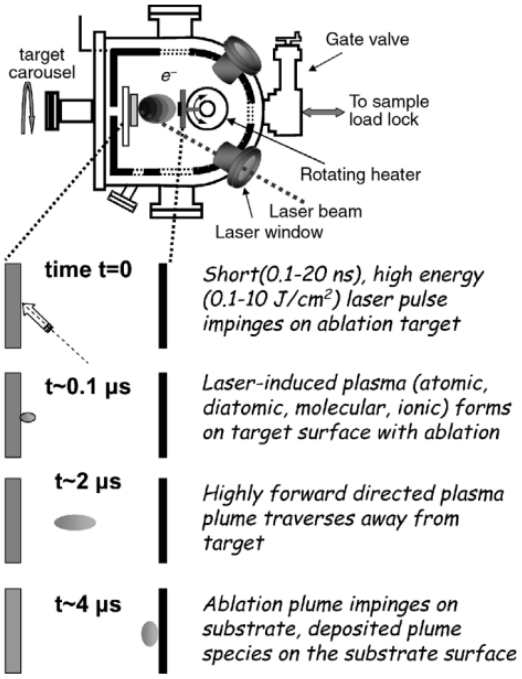

Figure 5. PLD schematic with the general components of the device and an included time scale and explanations for the plasma plume movement [31].

and the pulse frequency of the laser, the temperature of the substrate (deposition temperature), and the oxygen pressure one is able to optimize the process to cater to the growth of different materials. The resulting thickness of the thin films is controlled mainly by the number of laser pulses. The schematics and time scale for the PLD deposition process is presented in Fig. 5. Some of the most useful features for our use is the stoichiometric transfer of the target material to the thin film, the easily tunable thickness of the resulting thin film by varying the amount of pulses and the other previously optimized parameters needed for the PLD process for the optimal growth of GCMO and SRO thin films. [31]

2.2 Electron beam evaporation (E-beam)

Electron beam evaporation (E-beam) is a way to deposit material onto a substrate via evaporation of the material by heating it with an electron beam. One possible

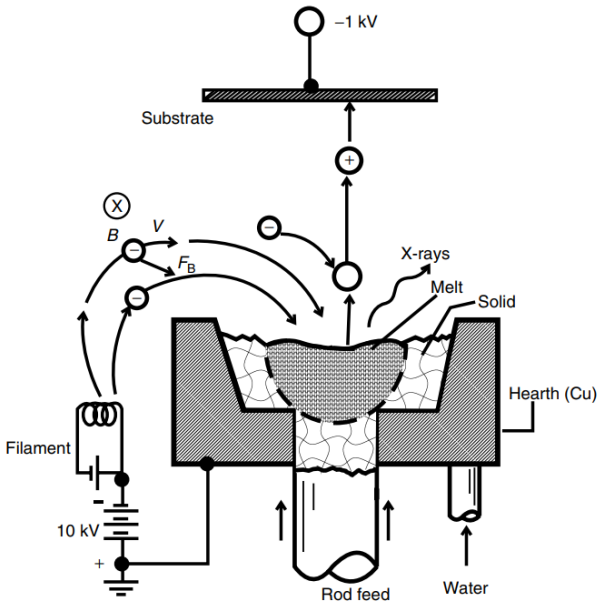

Figure 6. Illustration of the E-beam configuration with the general components and electrical circuits of the device and an illustrated path for the electrons moving from the filament to the crucible, and the path of the material vapor moving to the substrate [32].

configuration of the E-beam is presented in Fig. 6. An intense beam of high energy electrons is generated in the filament cathode using a high voltage of 10 kV. The beam is directed towards the surface of the evaporation material at the crucible acting as an anode. The kinetic energy of the electrons striking the surface is converted to other forms of energy via electrons interacting with the atoms of the material. Some of the energy ends up as thermal energy of the evaporation material. The melted or sublimated material creates a vapor which then makes contact with the substrate placed on its path. The parameters of the deposition process, e.g., the deposition rate and resulting thickness of the thin film, are easily adjustable. The process takes place in a high vacuum, as the lower pressure provides a longer electron mean free path and less contamination by particles from air. To control the path of the electrons, an electric or a magnetic field can be utilized. [32]

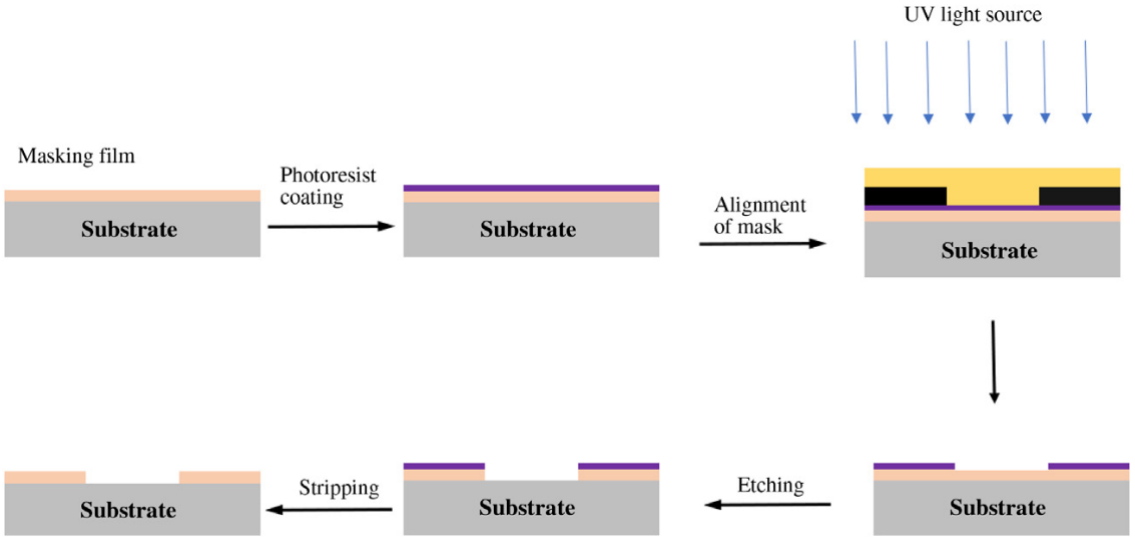

Figure 7. A schematic of the photolithography and etching process with the needed steps to achieve a patterned thin film [33].

2.3 Photolithography and etching

Photolithography and etching are used when delicate patterns of the material are needed instead of a full thin film. Photolithography and etching go usually hand in hand, as etching is carried out within an ongoing photolithography process. Fig. 7 illustrates the sequence of the process including both photolithography and etching. Almost any kind of pattern can be optically transferred on the surface of a substrate, but in this case the pattern is to be etched out of a fabricated thin film of some other material. Firstly, the full thin film is fabricated on top of the substrate, e.g., by PLD or E-beam, to the thickness of the pattern wanted at the final stage. The surface is then coated with a thin, smooth film of a positive or a negative photoresist via spinning a droplet of the resist at a high rotation speed (spin coating). When the resist is exposed to electromagnetic (UV) radiation, the molecular structure changes, changing also its solubility. When a shadow mask is placed on top of the sample, the radiation is blocked from reaching the resist beneath it leaving parts of the resist unchanged by the light. Depending on whether the resist was positive- or

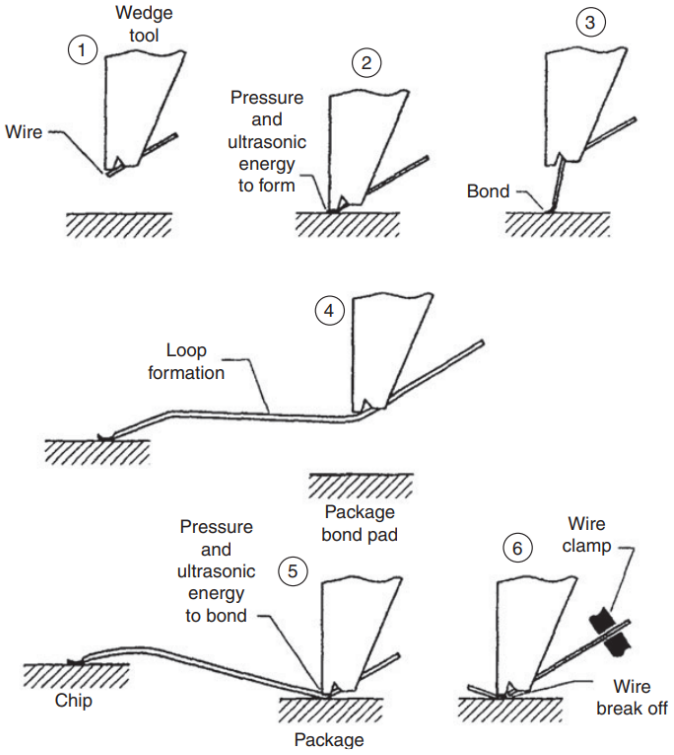

Figure 8. A schematic of the ultrasonic wire bonding process with the needed steps to achieve a bonded electrical contact between two points [34].

negative-type, the UV-treated or untreated areas of the resist are removed by some chemical, e.g., with a NaOH solution, whilst developing the rest of the resist. Now the resist covers only the chosen pattern of the surface, thus providing an area for the etchant to work on. When the pattern is etched out of the thin film, the leftover resist can be stripped off the surface leaving us with a substrate with a cleanly carved out pattern of the original thin film material. In theory, the wet chemical etching should result in sharper and more accurate edges of the patterns and finer patterns overall than those fabricated using PLD or E-beam with shadow masks. [33]

2.4 Ultrasonic wire bonder

Ultrasonic wire bonding is the last step in the fabricating and connecting of the sample to the mount for the electrical measurements. It is not an actual fabrication method for thin films, per se, but it is still a crucial part of the preparation of the sample for the experiments. The principle of the wedge-bonding technique follows the steps presented in Fig. 8. The operation of the machine can be manual, thus the placements of the bonds can be chosen freely. The wire, in our case Al wire with the thickness of 33 μm, is placed between the wedge tool and the surface of the sample and pressed with ultrasonic energy provided simultaneously to form the first bond. The tool is lifted and moved, forming a loop out of the wire originating from the initial bond. The second bond is made in a similar fashion with pressure and ultrasonic energy, after which the rest of the wire is broken off by clamping and pulling it back. As the wire is bonded from both of its ends, it will create an electrical connection. [34]

3 Characterization methods

To determine the quality of the fabricated samples we need different characterization methods to determine the quality of different properties of the samples. The following chapters will discuss the used methods: memristor characterization platform ArC ONE, scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), and atomic force microscopy (AFM). As the focus of studying a memristor is in the electrical transport measurements, ArC ONE is the main characterization method utilized for the measurements and the rest are complementary methods.

Figure 9. ArC ONE user interface and the functional panels: Device History, Manual Operations, Toolbar, Data Plot, Advanced Modules, and Crossbar Panel [35].

3.1 Memristor characterization platform, ArC ONE

All information in this chapter is taken from the ArC ONE Memristor Characterization Platform User Manual [35]. ArC ONE is made specifically for testing and characterizing the electrical transport properties of memory devices. ArC ONE is a commercial product of ArC Instruments, but the methods implemented within the measuring program replicate the general measurements done on memristive devices, e.g., IV and RV curves, manual pulsing of voltages, and reading of the resistive state. The fabricated sample can be connected to word- and bitline header banks on the ArC ONE hardware instrumentation board to access specific devices at specific addresses.

ArC ONE provides multiple different modes and scripts for testing and characterizing memory devices. All of the functions are used through the user interface's functional panels shown in Fig. 9. The basic operations, i.e., positive and negative voltage pulse and resistive state read (TIA4P: Kelvin sensing at a programmable

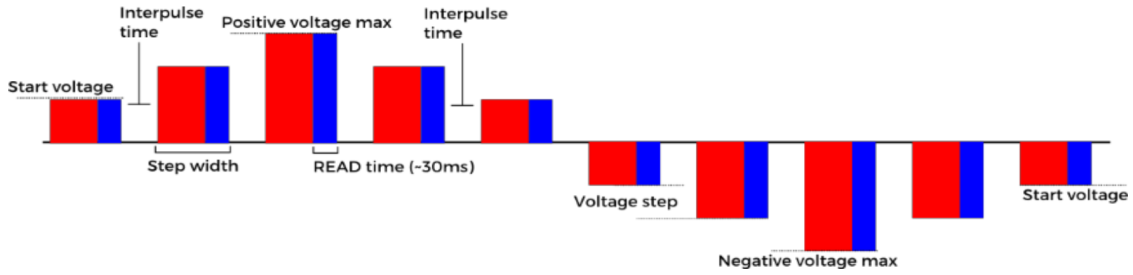

Figure 10. The pulsing algorithm of CurveTracer with some of the adjustable parameters [35].

voltage) functionalities, can be operated manually from Manual Operations. The voltage value 0.5 V was chosen as the main read voltage. The Advanced Modules panel houses, for example, the following Advanced Pulsing Modules: CurveTracer, Retention, SwitchSeeker, MultiStateSeeker, and SuperMode (freely combine and loop any modules and functions). The modules can be applied to a specific crosspoint corresponding to a device (word- and bitline) chosen from the Crossbar Panel, a range of devices, or all of the devices.

CurveTracer is the standard mode for IV measurements. Fig. 10 shows the pulsing algorithm of CurveTracer and the parameters associated with it. The adjustable parameters of CurveTracer and the values or ranges used for the measurements are collected in Table I. The current is measured towards the end of each write pulse, thus providing us with the IV curves. The IV measurements can be also done on a live version of CurveTracer, where one is able to change the parameters of the measurement during the measuring process. Measuring the IV curves is an important starting point for characterizing the memristors, as the shape of the curve can be used to predict the resistive switching possibilities of the device. In addition to the standard IV curves, one can see RV and logarithmic IV curves constructed from the original measurement data after the measurement is done.

Retention is used to determine how the resistive state of a device changes over a period of time. The adjustable parameters of Retention are the time interval

Table I. The adjustable parameters of CurveTracer and the approximate values or ranges used for the measurements.

Parameter	**Value/range**	**Unit**
Positive voltage max	1 to 12	V
Negative voltage max	-1 to -12	V
Voltage step	0.05	V
Start voltage	0.05	V
Step width	2	ms
Cycles	1 to 10	-
Interpulse	10	ms
Positive current cut-off	0	μA
Negative current cut-off	0	μA
Halt and return	Not chosen	Checkbox
Bias type	Staircase	Dropdown menu
IV span	Start towards V+	Dropdown menu

Table II. The adjustable parameters of Retention and the approximate values or ranges used for the measurements.

Parameter	**Value/range**	**Unit**
Read every:	1	Dropdown menu, min
Read for:	5	Dropdown menu, h

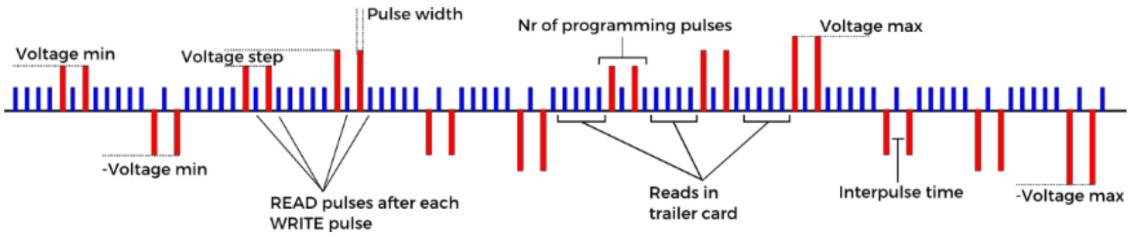

Figure 11. The pulsing algorithm of SwitchSeeker with some of the adjustable parameters [35].

and full duration of time to read the resistive state (Table II) which are located in the Retention Operations panel, and the reading method and reading voltage set in the Manual Operations panel. When used with SuperMode, Retention can be implemented subsequently to positive and negative voltage pulse sequences to follow the behavior at different resistance states of the device. As the goal for an optimally working memristor is to retain the reached resistance state without any upkeep of applied voltages, the result of the Retention is a useful tool for determining device quality.

SwitchSeeker assumes a bipolar device and then tries to determine the pulse parameters of repeatable resistive switching by applying voltage pulses of both polarities with increasing width and amplitude. Fig. 11 shows the pulsing algorithm of SwitchSeeker and the parameters associated with it. The adjustable parameters of SwitchSeeker and the values or ranges used for the measurements are collected in Table III. The main use for SwitchSeeker is the determination of voltages at which the resistive switching occurs, but it can also act as an indicator of missing resistive switching behavior. In our case the module was most useful at predicting whether the device was capable of responding to any voltage pulses at all, as the method would not continue on to the second state if no resistive switching behavior is found.

MultiStateSeeker can be used to check the device's ability to reach and retain different resistance states, i.e., assess multiple bit storage capabilities. The script has three phases: Phase I - Polarity interface, Phase II - Pulsed stability calibration, and

Table III. The adjustable parameters of SwitchSeeker and the approximate values or ranges used for the measurements.

Parameter	**Value/range**	**Unit**
Reads in trailer card	5	-
Programming pulses	10	-
Pulse duration	2	ms
Voltage min	0.5	V
Voltage step	0.05	V
Voltage max	1 to 12	V
Max switching cycles	5	V
Tolerance band	10	%
Interpulse time	1	ms
Resistance threshold	1 000 000	Ω
Seeker algorithm	Fast	Dropdown menu
Stage II polarity	Not chosen	Dropdown menu, if checkbox Skip Stage I selected
Read after pulse	Not chosen	Checkbox

Table IV. The adjustable parameters of MultiStateSeeker and the approximate values or ranges used for the measurements.

Phase	**Parameter**	**Value/range**	**Unit**
Phase I: Polarity interface	Reads	5	-
	Prog. pulses	10	-
	Pulse width	2	ms
	Voltage min	0.5	V
	Voltage step	0.1	V
	Voltage max	12	V
	Interpulse	1	ms
	Tolerance band	10	%
	Read after pulse	Not chosen	Checkbox
Phase II: Pulsed stability calibration	Pulse voltage	8 to 12	V
	Pulse width	2	ms
	State mode	As calculated	Dropdown menu
	Stability test	Linear fit	Dropdown menu
	Max time	10	s
	Tolerance band	10	%
Phase III: State assessment	Mode	Voltage sweep	Dropdown menu
	Reads	20	-
	Max prog. pulses	10	-
	Pulse width	2	ms
	Voltage bias	Not chosen	V, if not assessed before
	Voltage min	0.5	V
	Voltage step	0.05	V
	Voltage max	12	V
	Interpulse	1	ms
	Retention time	1	ms
	Std. deviations	3σ	Dropdown menu
	Monotonicity	Move to next step	Dropdown menu
	Reset counter after step	Chosen	Checbox

Phase III - State assessment. The first phase acts in a way similar to SwitchSeeker: It tries to determine the polarity of the device by applying increasing amplitude voltage pulses of varying polarities with some tolerance band for the change in resistance. When the polarity is found, the module continues to the next phase, which is designed to stabilize the device into a resistive state chosen by the polarity interference. If the resistive state is found to be stable, the module proceeds to the last phase where the accessible resistive states are assessed. In short, after determining the polarity of the device, the resistive state is driven to the HRS or the LRS with subsequent voltage pulses, after which all of the resistive states to the LRS (if starting from the HRS) or to the HRS (if starting from the LRS) are searched for. In theory, the method should return at least the HRS and the LRS (binary digit memory) reachable by manual voltage pulses, but in the best case there should be multiple resistive states between them (multibit memory). The adjustable parameters of MultiStateSeeker and the values or ranges used for the measurements are collected in Table IV.

3.2 Scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS)

Scanning electron microscopy (SEM) is a nondestructive surface imaging technique suited for characterizing a multitude of different materials ranging from biological to minerals and alloys. The main instrument components of SEM are an electron source, a lens system, a scan unit, and a detection unit. Electrons are generated at the electron source using high voltages (30–40 kV). The electron beam is accelerated, focused, and directed by the lens system consisting of electromagnetic and electrostatic lenses and different apertures. The scan unit is responsible for the raster pattern scan over the specimen surface. As the electron beam strikes the surface, the electrons interact with the sample surface atoms in different ways

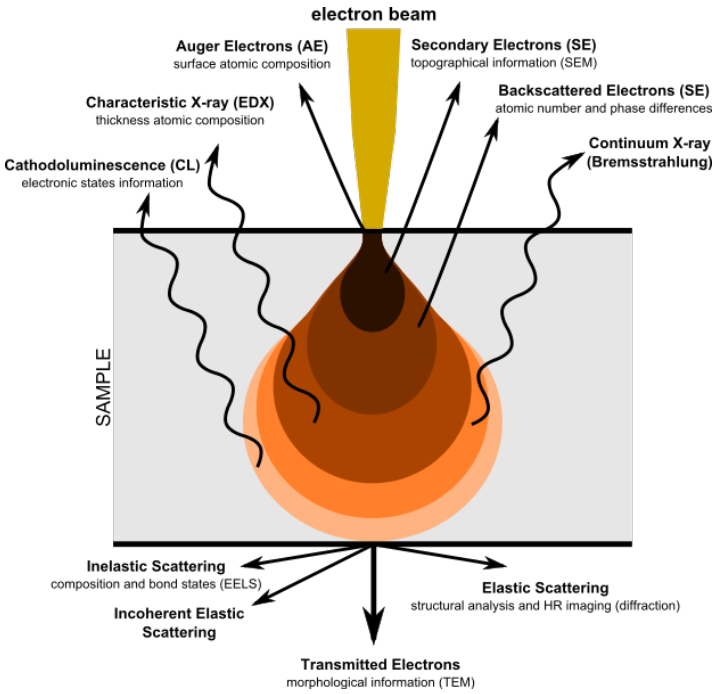

Figure 12. Electron-matter interaction volume (pear shape) with related and resulting phenomena and signals [36].

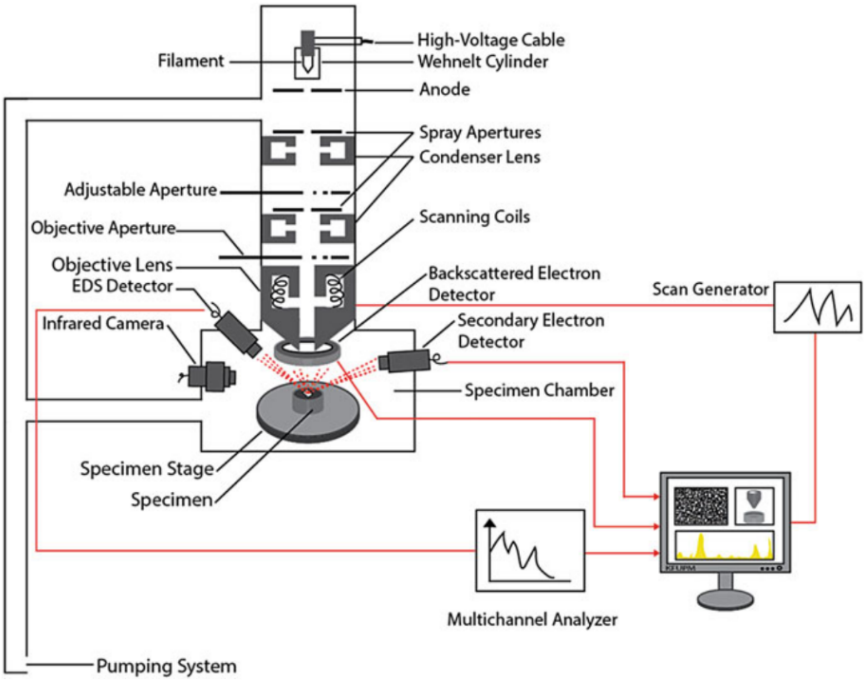

Figure 13. Schematic illustration of the typical SEM components [37].

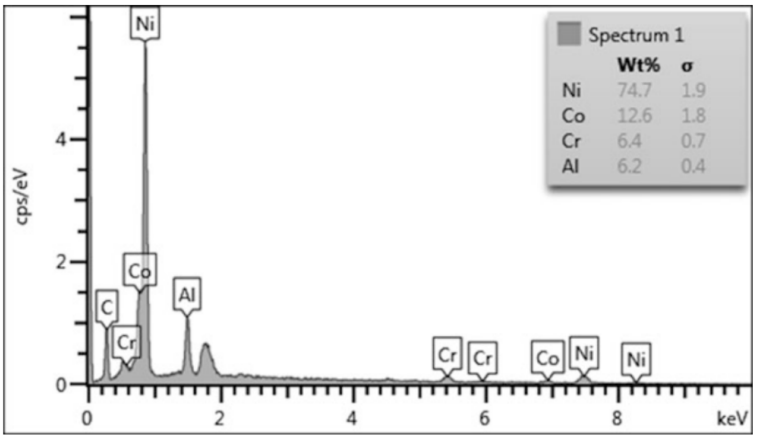

Figure 14. EDS spectrum, i.e., the intensity (counts per second) as a function of the energy of the emitted X-ray photons (keV), with an added elemental concentration quantification [37].

producing detectable electrons and photons (X-rays). An illustration of the electron-matter interaction volume is presented in Fig. 12. After making contact with the specimen, the scattered electrons, e.g., backscattered electrons, are collected in different detectors depending on the origin and scattering method of the electrons. The information from the detectors is then displayed on a computer monitor to be examined. The schematic illustration of the configuration of the SEM can be found in Fig. 13. In our case, the utilized machine for SEM measurements was Apreo S from Thermo Fisher Scientific and the detectors were the Everhart-Thornley detector (ETD) placed next to the sample close to the sample surface at a slight angle (around 30°) for measuring secondary electrons and the in-lens Trinity detector T1 placed within the column for measuring backscattered electrons. T1 provides us with the composite sample contrast when operated in composite mode and the ETD highlights the topographical information of the surface. [37, 38]

Energy-dispersive X-ray spectroscopy (EDS) is an additional instrumentation for SEM meant for elemental identification of the sample and for obtaining characteristic X-ray peaks and the X-ray maps of the material. Characteristic peaks come from the characteristic excitations (K, L, and M lines) of electrons within the material as

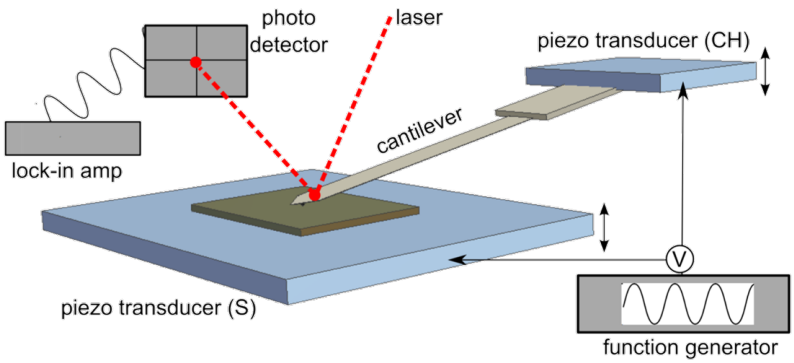

Figure 15. Schematic illustration of the typical AFM components [39].

a high energy 15–20 keV electron beam is used. The EDS detector measures these characteristic X-rays and compares them automatically to the database of materials. An example of an EDS spectrum is shown in Fig. 14. For us, the EDS measurement was used as verification that the elemental composition of the sample was what was expected. [37]

3.3 Atomic force microscopy (AFM)

Atomic force microscopy (AFM) is another imaging method for studying the surface structures and details of a vast range of materials. AFM is based on repulsive and attractive Van der Waals interactions between the surface of the sample and the probe tip of the cantilever. The measurements can be done using different modes, e.g., contact mode, tapping mode, and non-contact mode. While scanning, the changes in these forces due to the surface contours and topography will vertically deflect the cantilever. The topographic surface information is collected via a photodetector using a laser pointed at the top of the cantilever. An illustration of the measurement configuration can be seen in Fig. 15. For our samples, the method was used to examine the edges of the material patterns fabricated with different methods. The used machine for AFM measurements was the Bruker Innova Atomic Force Microscope and the chosen operating mode was contact mode. [40]

Table V. The fabricated samples, the used method of fabrication for each material layer and the parameter that was changed between iterations (pulses or thickness), and the corresponding chapters where the results are discussed.

Sample	**SRO**		**GCMO**		**Al**		**Chapter**
	Method	Parameter	Method	Parameter	Method	Parameter	
1	PLD	300 pulses	PLD	1500 pulses	E-beam	150 nm	4.2.1
2	PLD	500 pulses	PLD	2000 pulses	E-beam	200 nm	4.2.2
3	Etched	300 pulses	PLD	2000 pulses	E-beam	200 nm	4.3.1
4	Etched	100 pulses	PLD	2000 pulses	E-beam	200 nm	4.3.2
5	Etched	150 pulses	Etched	2000 pulses	E-beam	200 nm	4.4

4 Results and discussion

The fabrication methods described in Chapter 2 can be combined in multiple different ways, thus the optimization of the fabrication process is complicated. Multiple sample iterations were needed to study the effects of the different fabrication methods. All of the samples and their preparation is presented in Chapter 4.1. The combinations of methods can be divided into three categories according to the amount of photolithography used in the process. The second section, Chapter 4.2, will concentrate on the results gained from the samples fabricated with shadow masks and PLD, completely without photolithography and etching. The section after that, Chapter 4.3, will introduce photolithography for the fabrication of the SRO stripes, with the rest of the sample still being made with shadow masks and PLD. Finally, in the last section, Chapter 4.4, we will also switch the fabrication of the GCMO pads to etching in addition to the etched SRO. Al is fabricated using E-beam throughout this thesis, but the thickness is changed after the first sample.

Table VI. The fabrication methods and the related constant parameters.

Method	Parameter	Value
PLD	Energy density	$1.2\,\mathrm{J/cm^2}$
	Pulse frequency	5 Hz
	Temperature	700 °C
	Oxygen pressure	0.175 Torr
Etching	Chemical (SRO)	0.01 M $NaIO_4$
	Chemical (GCMO)	[HCl] = 0.122 M (≙ 0.37 wt%), [KI] = 5 M, [Ascorbic acid] = 0.1 M
	Photoresist	MEGAPOSIT™ SPR™ 220-3.0 positive photoresist
	UV light exposure time	70 s
	Development time	30 s
E-beam	Deposition rate	2 Å/s
	Pressure	1×10^{-7} mbar
	Voltage	10 kV

4.1 Fabricated samples

All of the samples were fabricated on top of STO (100) substrates, which had one polished side and were the size of $5 \times 5 \times 0.5\,\mathrm{mm^3}$. The SRO thin films were then deposited on top of the substrates with PLD, either with a shadow mask of 4 stripes or one with a full square opening. Usually, the thermal contact is ensured by gluing the substrate onto the holder with a silver paste, but in our case, it was only tightened with a shadow mask and two screws. No silver paste was used in the rest of the PLD usage either. During the PLD process, an oxygen circulation of 0.175 Torr was used to ensure that none of the oxygen of the sample surface is removed during the heating. The deposition was carried out when the temperature of the substrate was 700 °C, using a deposition energy density of $1.2\,\mathrm{J/cm^2}$ and a pulse frequency of 5 Hz. The same parameters were used for the making of the GCMO pads or thin films.

For etching of the two materials, two different etchants were needed: $NaIO_4$ for SRO and a combination of HCl, KI, and ascorbic acid for GCMO. Otherwise, the process remained the same for both with a positive photoresist spinned on the

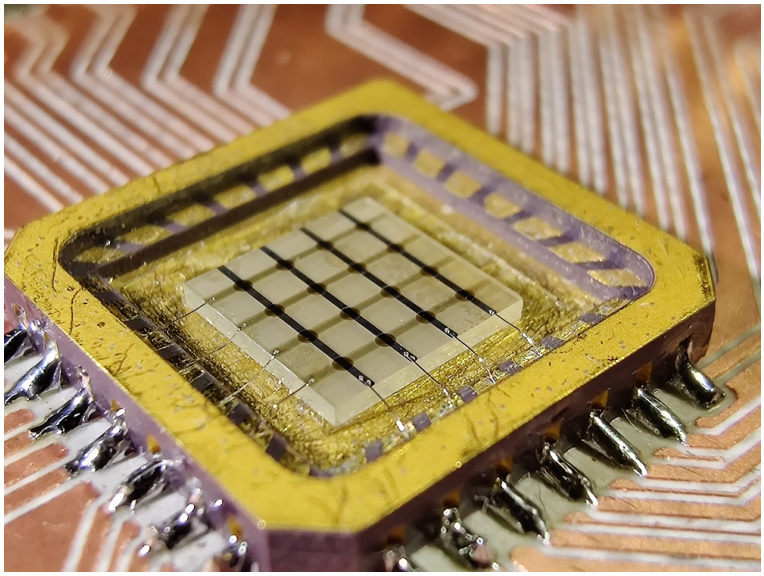

Figure 16. Sample 1, fabricated using PLD and shadow masks for the SRO stripes (300 pulses, fainter stripes) and the GCMO pads (1500 pulses) and E-beam for the Al stripes (150 nm, darker stripes). The Al wires were bonded ultrasonically to the SRO and Al stripes, one contact per stripe.

surface, a UV light exposure time of 70 seconds, a development time of 30 seconds in diluted NaOH, and the needed time in the etchant to reveal the patterns.

The final layer of Al stripes was done with E-beam and a shadow mask, with the pressure of the deposition chamber being around 1×10^{-7} mbar, a high voltage of 10 kV, and a deposition rate of 2 Å/s. The exact methods used and the parameters related to those are collected in Table V in relation to the samples marked 1–5. Also the chapters where the results of these samples are discussed are marked into the same table. Parameters that were kept unchanged for each fabrication method are collected in Table VI.

4.2 Samples with shadow masks

4.2.1 Sample fabricated using PLD

The fabrication process of Sample 1 was quite simple: The SRO lines and GCMO pads were fabricated with shadow masks and PLD, and the Al stripes were added

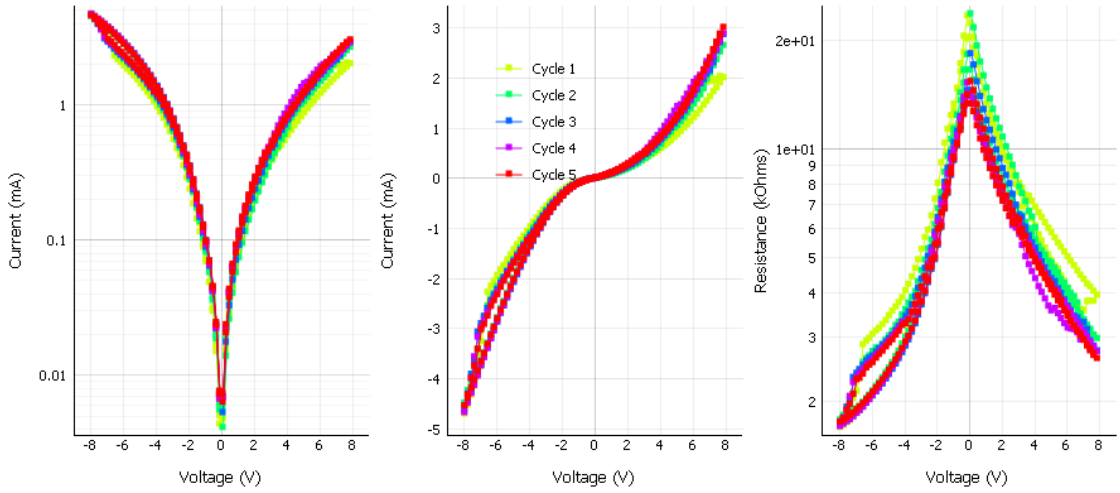

Figure 17. Example of a CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 1. Voltage limits −8.0 V and 8.0 V.

using a shadow mask and E-beam. The parameters of the fabrication process of the sample can be found in Tables V and VI of Chapter 4.1, and an image of the sample fabricated in the described way can be seen in Fig. 16. After the fabrication of the layers, Al wires were bonded to the four SRO, four Al stripes, and the mount to continue on to the measurements.

As Sample 1 was the first sample fabricated, we needed to determine some kind of a starting point for the optimization process. For that, we used the ArC ONE measuring device to study the memristive properties of the sample. Fig. 17 shows one of the best results obtained for the IV and RV curves amongst the 16 devices within the sample. The familiar shape of Schottky-type contacts, some asymmetry between positive and negative voltages, quite high overall resistance, and slight hysteresis on mainly the negative voltage side of the curve can be seen in the figure. This was a promising start for the process, as there was no guarantee that any reasonable results were obtainable without optimization. Even though the ArC ONE results were partially promising, some problems arose during the measurements. The main problem seemed to be the low resistance compared to the resistance of

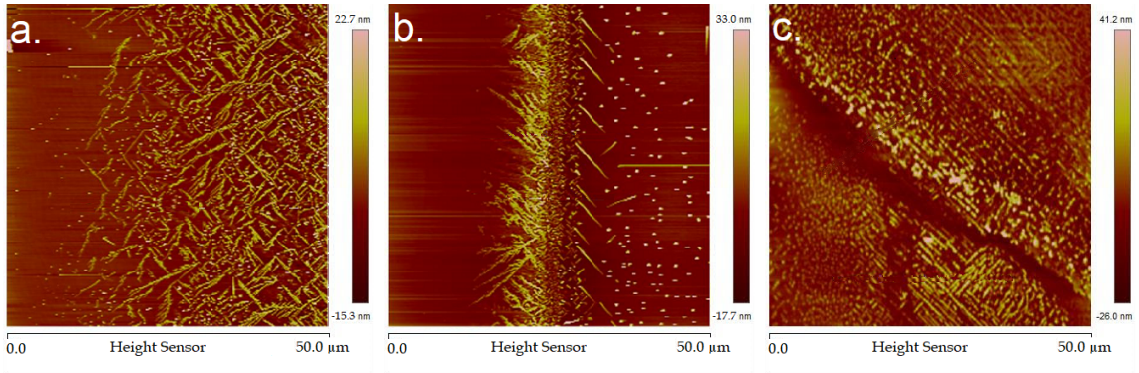

Figure 18. AFM measurements done on Sample 1 with the patterns fabricated with shadow masks and PLD with an additional test sample, full SRO thin film fabricated with shadow masks and PLD. SRO thickness in both samples is 300 pulses, GCMO thickness in Sample 1 is 1500 pulses. a. Edge of a full thin film of SRO. b. Edge of a thin film stripe of SRO, stripe on the left side of the image. c. Edge of GCMO pad overlapping with a SRO stripe. Lighter, more yellow parts of the images are the raised and textured areas.

a singular SRO stripe (measured to be around 1.5 kΩ for one stripe) of most of the devices, which could be interpreted as a breakdown of the device, or a short circuit through some other contacts. The devices of the sample seemed to affect the neighboring ones, mainly along the Al stripes. Also, the wanted hysteresis within the IV curves disappeared quite rapidly whilst measuring. This could be seen as devices weakly or not at all responding to applied voltages, i.e., there was no real resistive switching present in the devices.

To find out some possible causes of these problems we were battling with, AFM measurements were done. The results of the AFM measurements (Fig. 18) revealed a previously unknown side effect of the fabrication process done with shadow masks: The parts of the material near the edges of the shadow masks were highly textured, even so that the textured pattern of the SRO stripe showed through the GCMO layer put on top of it. The rough edges were not small either, as the texture could reach up to tens of microns towards the middle of the material and could be up to a hundred nanometers higher than the rest of the surface. As the height of these peaks were the same scale as the thickness of the layers, the possibility of the layers

beneath peeking through and disturbing the growth of the layers on top was high.

One supposed quick fix to these problems was to thicken all of the layers, as thicker layers could smooth out the irregularities of the surfaces below for the addition of the next material layer. Breakdowns and shortcuts should then be less common among the devices. The thicker layers were implemented in the next sample, Sample 2, which shall be discussed in the next chapter.

4.2.2 Thicker layers of SRO, GCMO, and Al

Sample 2 was fabricated in a similar fashion to the first one, using shadow masks and PLD for SRO and GCMO layers and a shadow mask and E-beam for the Al stripes. The difference between these samples was the thickness of the thin film layers of the used materials, as can be seen in Table V of Chapter 4.1. All of the layers were thickened, SRO from 300 pulses to 500 pulses, GCMO from 1500 pulses to 2000 pulses, and Al from 150 nm to 200 nm. The 4×4 devices were easy to find by bonding the Al wires to the Al stripes and SRO stripes, one contact per stripe. This time with the thickened Al the bonding seemed to stick better and not rip out as easily as with Sample 1, so the thicker layer of Al was used for the rest of the samples.

ArC ONE was used also for Sample 2 to compare the effect the thicker layers had on the behavior of the devices. Some of these contacts seemed to have the wanted shape of IV curves, but still the hysteresis was not stable: Even slight modifications to the used voltages could "break" the device, resulting in flattening of the hysteresis especially around the zero point as can be noticed in Fig. 19. In some cases this effect, usually a lost HRS, was reversible by applying carefully selected voltages, but in most cases the voltage limitations of the ArC ONE restricted the rescue of the device. This resulted in lost resistive switching property of the devices.

The weak hysteresis was not the only problem reminiscent of the first sample,

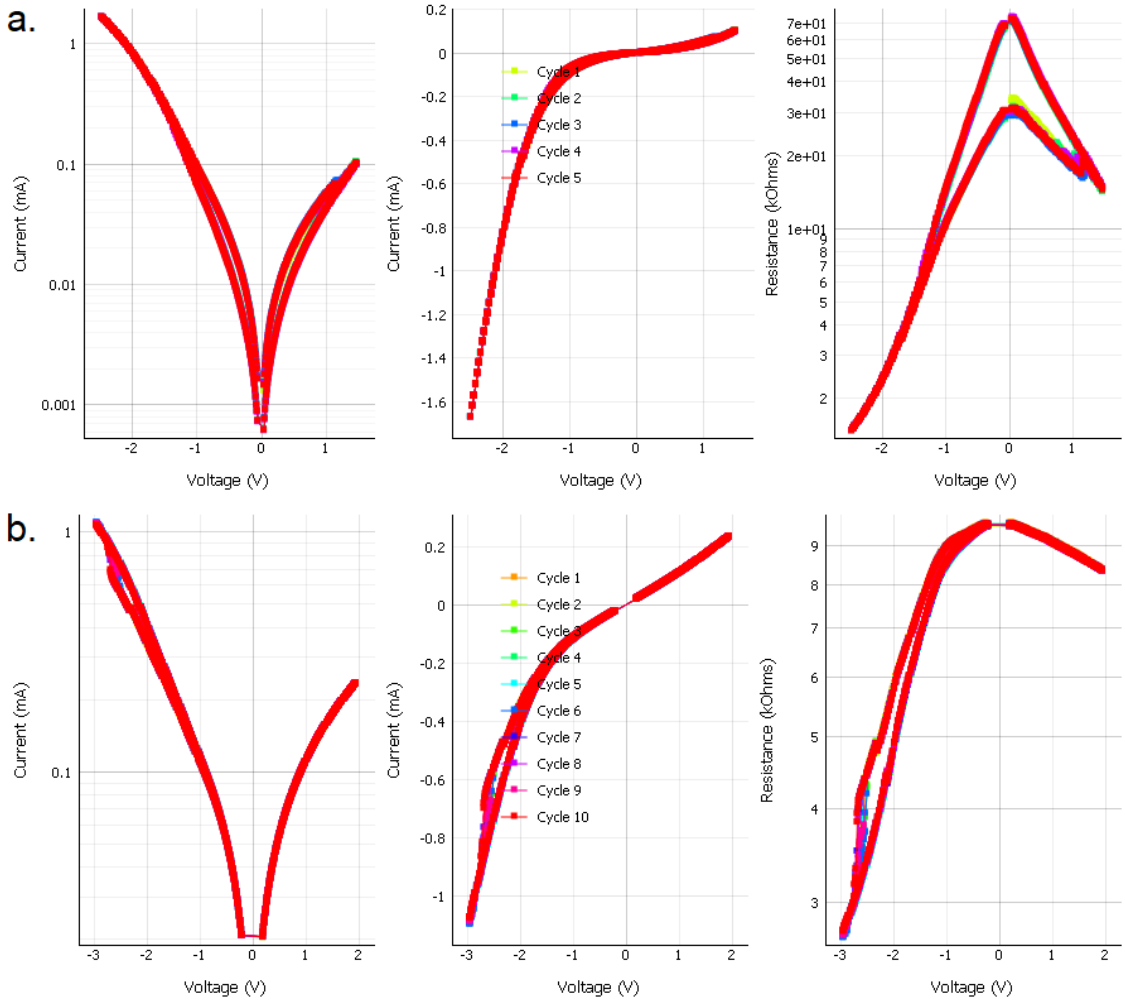

Figure 19. CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 2. a. Voltage limits −2.5 V and 1.5 V. b. Voltage limits −3.0 V and 2.0 V.

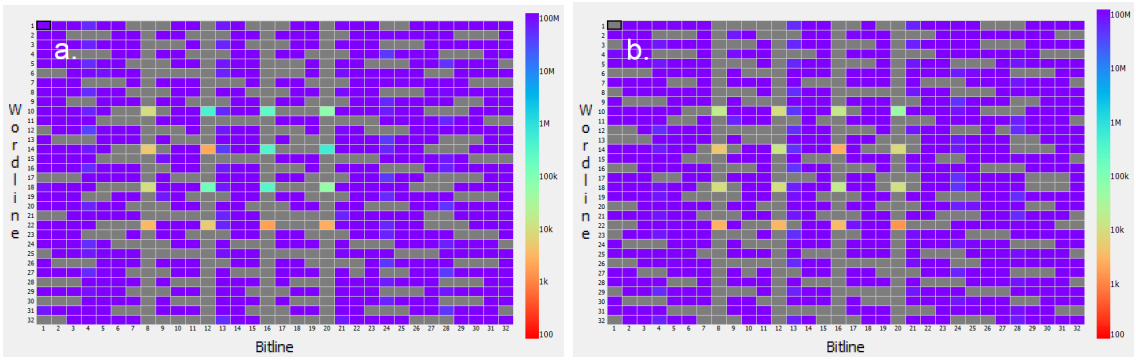

Figure 20. Image taken from the ArC ONE measuring program depicting the resistances of the devices present in Sample 2 read using 0.1 V. a. Read before a measuring session and b. Read after a measuring session. Brighter, lower resistance squares depict the found contacts with resistances ranging from 1 kΩ to 1 MΩ

as we also encountered the linked breakage of the devices. Fig. 20 depicts the resistances of the devices before and after a measuring session. As we can see, the previously high resistances had all dropped to lower resistances (towards more orange coloring), many to similar values from 1 kΩ to 10 kΩ. The resistance differences between the devices had diminished, even without applying any voltages to some of the devices. This was a huge problem, which needed to be corrected somehow.

The thickening of the layers did not fix many of the problems present in Sample 1, but the Al contacts seemed to connect better without ripping out as much. As we still had many of the problems of Sample 1, another way to optimize the behavior of the sample was needed. The most problematic layer seemed to be the rough and textured SRO stripes poking through the GCMO layer, so the SRO layer was the next one to go through more careful optimization. The fabrication of the SRO stripes was switched to photolithography and etching, which also introduced the varying width SRO stripes to the devices. The samples using etched SRO will be discussed in the next chapter.

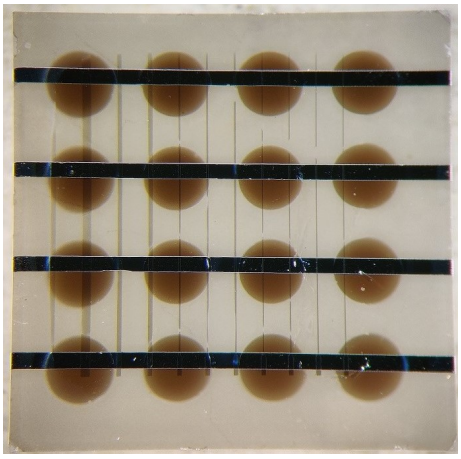

Figure 21. Sample 3, fabricated using photolithography for the SRO stripes (300 pulses, fainter, vertical stripes), shadow masks and PLD for the GCMO pads (2000 pulses), and E-beam for the Al stripes (200 nm, darker, horizontal stripes).

4.3 Samples with etched SRO

4.3.1 SRO fabricated using photolithography

In Sample 3, the fabrication of the SRO stripes was switched to photolithography, while the GCMO pads and Al stripes were made in the same way as the previous two samples, especially the thicknesses of those two layers were kept the same as they were in Sample 2. The SRO layer was switched back to a thinner one, as the thickening did not prove useful and was possibly an even worse option. The parameters of the fabrication process of Sample 3 can be found in Table V of Chapter 4.1, and an image of the sample fabricated in the described way can be seen in Fig. 21. If we closely inspect Fig. 21, we can see that some of the SRO stripes had been severed during the deposition of the GCMO pads with PLD. This resulted in the inability to bond and connect only once to the 4 stripes of Al and 4 stripes of SRO to access all of the 16 devices (GCMO pads). It should also be noted, that the positioning of the SRO stripes passing under the GCMO pads was difficult, as the shadow mask used to generate patterns out of the photoresist was placed in an approximately good position by hand. This means that one or more SRO stripes

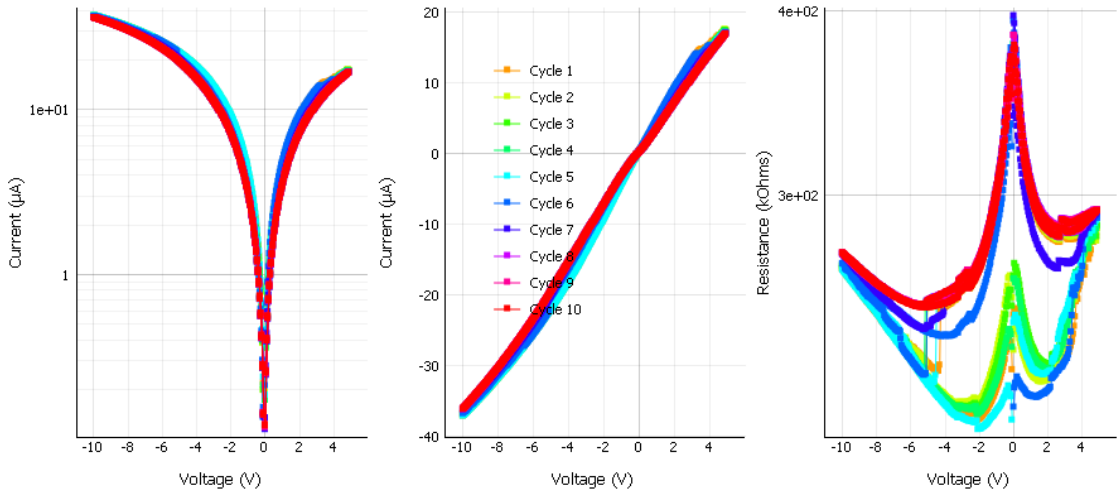

Figure 22. CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 3. Voltage limits −10.0 V and 5.0 V.

could be used as the other side of the capacitive contact per one GCMO pad. It should also be taken into account that the position of the Al stripes is not always in the middle of the GCMO pads, thus the important interface could lie at the rough edge of the material.

ArC ONE was the main categorization method used to test Sample 3. One example of the obtained, unstable, IV curve of one of the devices can be seen in Fig. 22. Even though some asymmetry in the curves and the highly sought after hysteresis around zero point is present in the figure generated from one of the devices, many of the other devices fabricated within the sample were unusable in a sense that they did not provide any hysteresis within the voltage limitations of ArC ONE. One other possible negative side effect of the switched fabrication method was the lost Schottky-like contact shape of the IV curve, as now the IV curve was more linear in most cases. A linear IV curve is in most cases a good indicator of Ohmic-like conduction. Also the consistency of the memristive behavior was still lacking: The SwitchSeeker reveals how the behavioral response of the device changed between four consecutive runs (Fig. 23), the last one looking the most promising. The contact

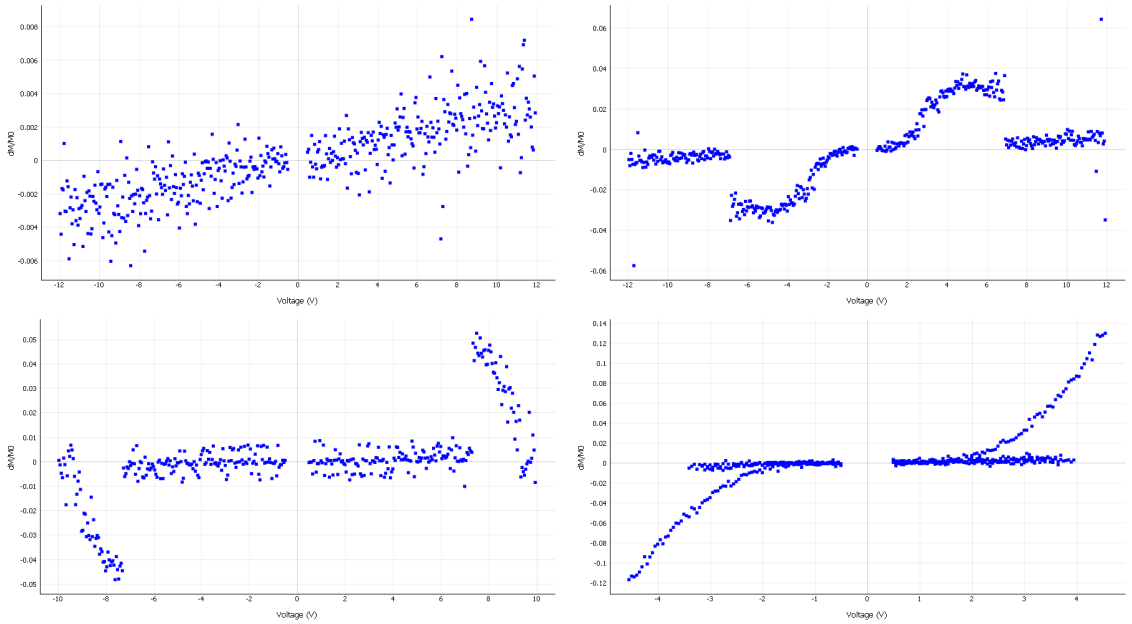

Figure 23. Four consecutive SwitchSeekers of Sample 3. Voltage limits were −12.0 V and 12.0 V, but not all runs reached those values.

area of the capacitor or the width of the used SRO line was not under inspection during these measurements, as there were still only few decently working devices to draw any conclusions out of the results for the preferred SRO line width.

Even though the results were better than those of the previous two samples, as there was no more linked breakage of the devices present in the sample, the photolithography process caused another set of problems to deal with. The uneven and severed SRO stripes made it difficult to say exactly how good the interfaces of the GCMO and Al could have been. We still had some doubts, that the thickness of the SRO layer was possibly a cause of some of the problems, as the 300 pulses worth of SRO was quite thick compared to the 2000 pulse GCMO layer. For the next sample we chose to make the SRO layer thinner, as according to [41], the current should be able to go through the thinner layer without difficulties.

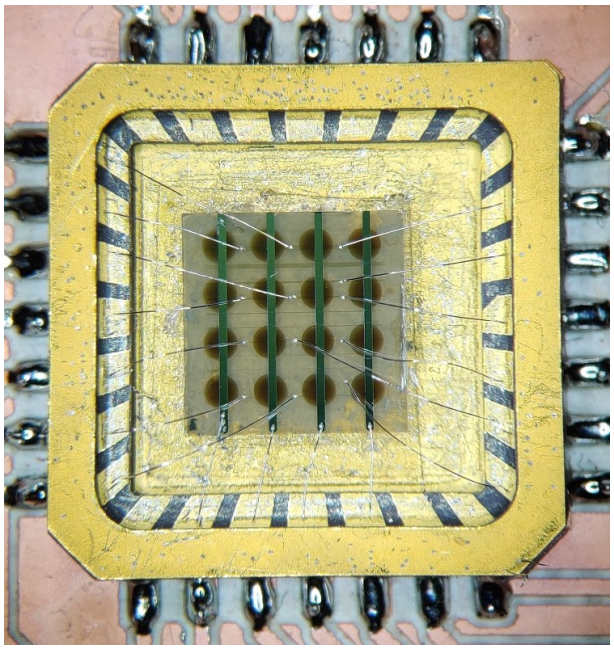

Figure 24. Sample 4, fabricated using photolithography for the SRO stripes (100 pulses, fainter, horizontal stripes), shadow masks and PLD for the GCMO pads (2000 pulses), and E-beam for the Al stripes (200 nm, darker, vertical stripes). The Al wires were bonded ultrasonically to the SRO and Al stripes, one contact per Al stripe, but multiple contacts to the SRO stripes.

4.3.2 Thinner SRO fabricated using photolithography

Etched SRO stripes were also used for Sample 4, but now the layer of deposited SRO was even thinner, instead of 300 pulses the layer was now 100 pulses. The parameters used for this sample can be found in Table V of Chapter 4.1, and an image of the sample already connected to the mount can be seen in Fig. 24. Similarly as for the last sample, multiple connections were needed for the SRO stripes to access the devices. Now there was no visual indication of severed SRO lines, but still only some of the contacts seemed to work.

Like for the previous ones, the memristive properties of Sample 4 were examined using ArC ONE. This time we saw multiple positively behaving devices across the different line widths of SRO (Fig. 25, a. 10 μm, b. 50 μm and c. 100 μm SRO line width). Some hysteresis was visible in all three presented devices, but as we can see, the quality of the hysteresis varied a lot. The IV curves were almost linear and symmetrical in most cases, the differences between the HRS and the LRS were small, and the found states were mostly unstable. The biggest problem was the unresponsiveness to voltage pulse sequences: When up to 12 V had been applied to the devices multiple times and read afterwards, the resistance state had not changed at all.

Even in the cases of seemingly promising IV and RV curves, Retention could prove the device to have unwanted behavior. For a device with 10 μm SRO stripes (Fig. 25a) the retention measurement revealed high instability after both applied positive and negative voltages (Fig. 26). Not all was lost, as some promising contacts also delivered somewhat promising retention measurements: For a device with 20 μm SRO stripes (Fig. 27), the device was able to retain some difference between the HRS and the LRS over the measurement time. This could be taken as a small victory, even though the difference between the states was small compared to the overall resistance.

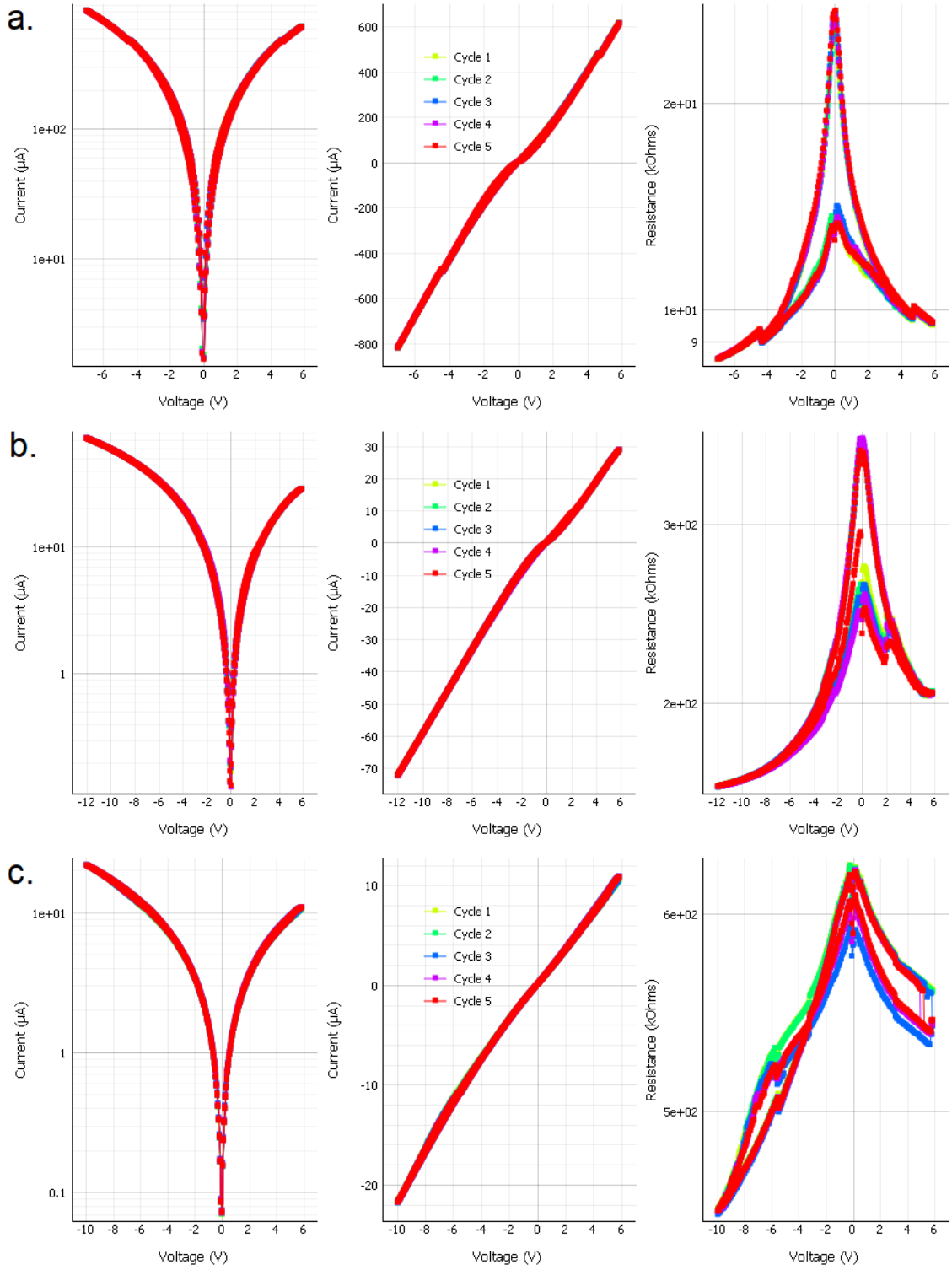

Figure 25. CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 4. a. SRO line width 10 μm, voltage limits -7.0 V and 6.0 V. b. SRO line width 50 μm, voltage limits -12.0 V and 6.0 V. c. SRO line width 100 μm, voltage limits -10.0 V and 6.0 V.

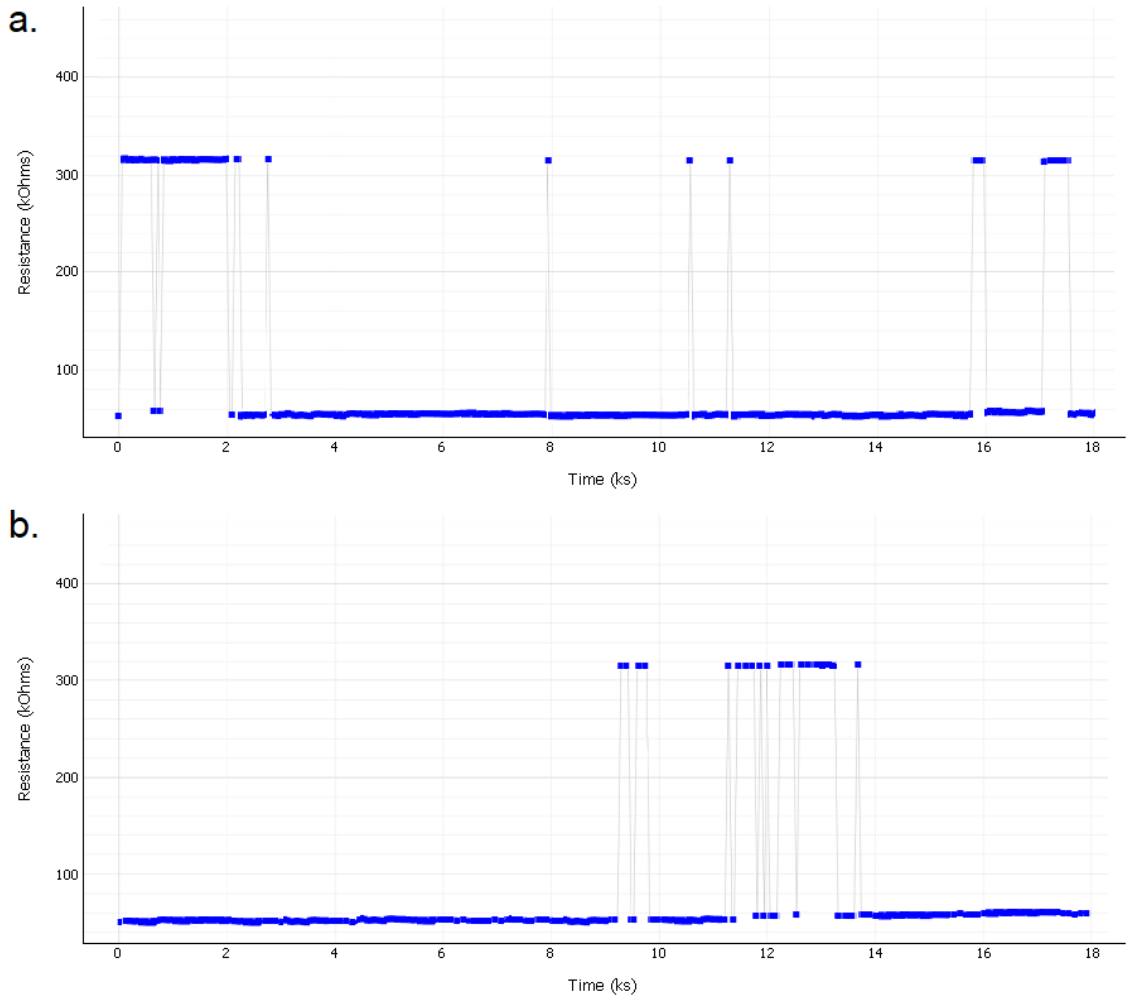

Figure 26. Sample 4, Retention measured for 5 hours after applied voltage pulses on a device with SRO line width 10 μm. a. 9.0 V applied voltage pulses. b. -8.0 V applied voltage pulses.

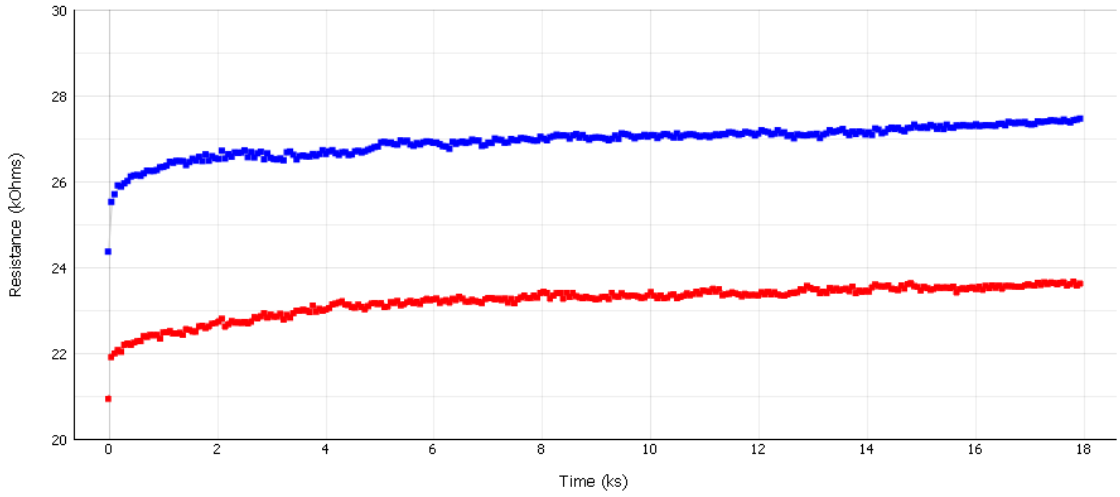

Figure 27. Sample 4, Retention measured for 5 hours after applied voltage pulses on a device with SRO line width 20 μm. Top (blue) curve measured after 12.0 V applied voltage pulses, bottom (red) curve measured after -12.0 V applied voltage pulses.

In addition to ArC ONE measurements, the sample was also examined using SEM and EDS. With SEM we were able to better study the edges of etched SRO and PLD fabricated GCMO (Fig. 28 a and b), as well as look at the full device (Fig. 28c). There was some unevenness present in the etched SRO edges, but the sizes of these leftover particles were much smaller than those coming from PLD, and there were no high ridges of material on the edge like there were before. The cross pattern on top of SRO was still visible, even on the cleaned surface of the STO substrate. The amount of particles and leftover material decreased as we moved away from the etched edge of the material. This could be interpreted as a too hastily ended etching process, as not all of the material had had time to be removed. The left side of Fig. 28b is covered in GCMO, but there was no clear edge of the material to be found. The thickness of the GCMO layer increased with a gradient towards the center of the pads when fabricated using shadow masks and PLD. The last figure also reveals there to be some missing or extra material in a shadow-like manner around the GCMO pad. With EDS we concluded that the elemental composition

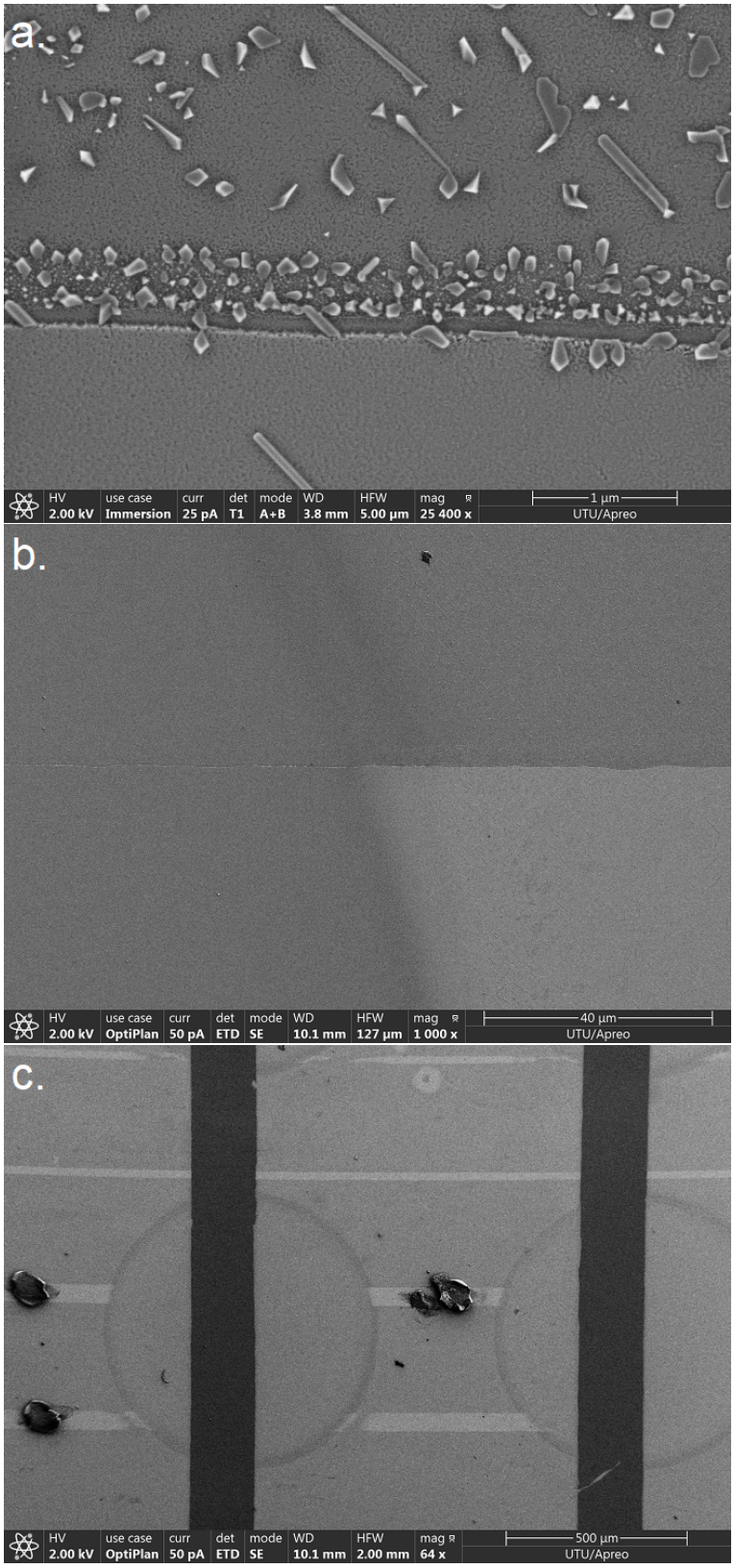

Figure 28. Sample 4, images from the SEM measurement. a. The edge of the etched SRO measured with T1 using 2.00 kV and 25 pA. b. The intersection of a SRO stripe and a GCMO pad measured with ETD using 2.00 kV and 50 pA c. The full device with some leftover Al connections bonded to the SRO stripes measured with ETD using 2.00 kV and 50 pA.

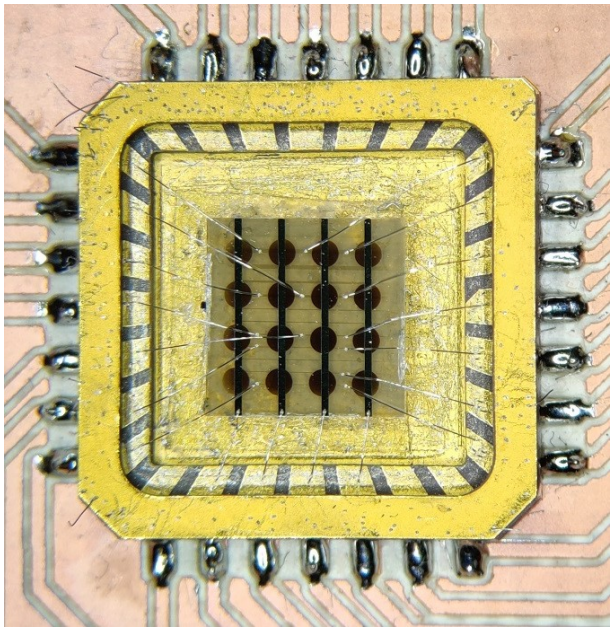

Figure 29. Sample 5, fabricated using photolithography for both the SRO stripes (150 pulses, fainter, horizontal stripes) and the GCMO pads (2000 pulses), and E-beam for the Al stripes (200 nm, darker, vertical stripes). The Al wires were bonded ultrasonically to the SRO and Al stripes, one contact per Al stripe, but multiple contacts to the SRO stripes.

of the sample was what was expected.

Inadequate SRO lines could again be the reason why only a part of the connected Al wires produced any output, but this time the fixing needed to concentrate on the fabrication of the GCMO pads. The unevenly deposited and grown GCMO could hinder the resistive properties the most, as the important interface was between GCMO and Al. For the next sample we chose to switch the fabrication of GCMO to photolithography, as it had resulted in some positive results for the fabrication of the SRO stripes.

4.4 Fully etched samples

The final sample utilized photolithography and etching for both the SRO stripes and GCMO pads, and E-beam for the Al stripes. The SRO layer was thickened up to 150 pulses from the previous 100 pulses, but the thicknesses of the GCMO and

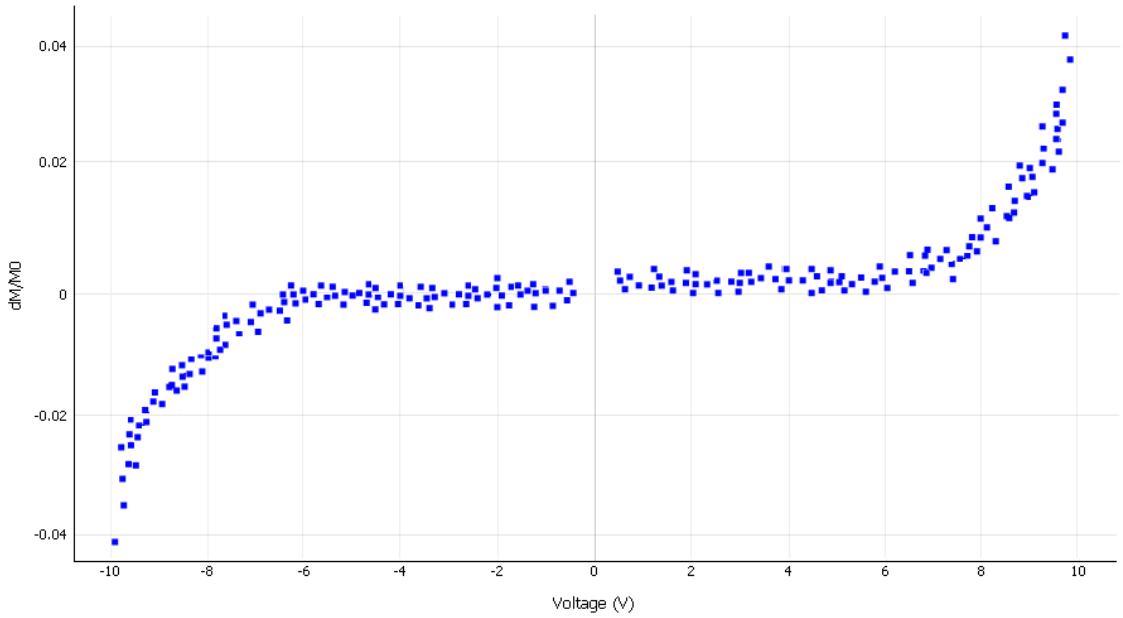

Figure 30. SwitchSeeker of Sample 5, SRO line width 20 μm, voltage limits -10.0 V and 10.0 V.

Al layers were kept the same as before. The parameters used for this sample can be found in Table V of Chapter 4.1, and an image of the sample already connected to the mount can be seen in Fig. 29. Similar to all of the samples utilizing etching for the SRO stripes, multiple connections were needed for the SRO stripes to access the devices. As compared to the previous sample, the thickening of the SRO layer did not help the connection problems to the SRO stripes.

The devices within the samples were tested with ArC ONE similarly to the other samples. The results were amazing in comparison to the results discussed previously, as we were able to detect the wanted memristive behavior in most of the devices. In general, the found HRS and LRS were generally further away from one another, the states were more stable, and the devices were more responsive to the applied voltages. The responsiveness to the voltage pulses was easily detectable also with SwitchSeeker measurements, e.g., from one of the devices with SRO line width 20 μm (Fig. 30). We still had the worrisome linearity of the IV curves (more Ohmic-like than Schottky-like contact), e.g., in Fig. 31, which had been present almost from

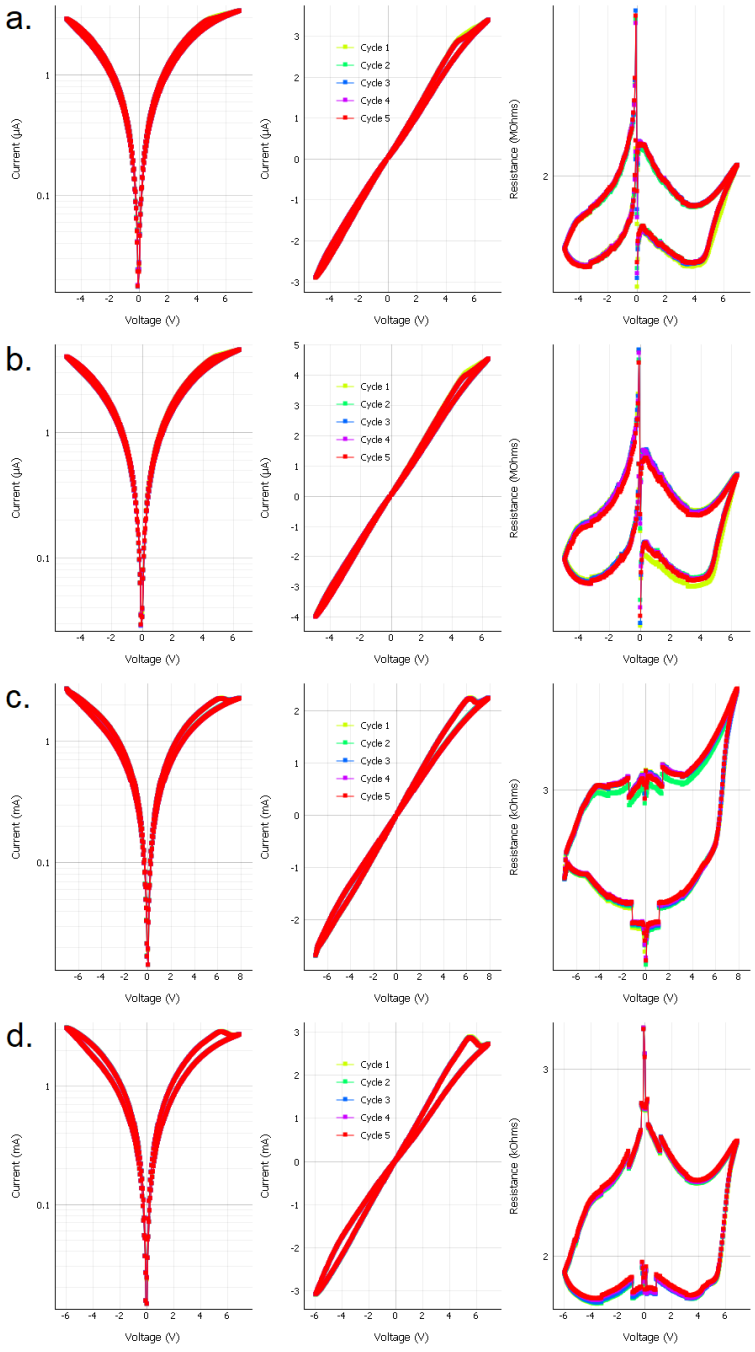

Figure 31. CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 5. a. SRO line width 10 μm, voltage limits -5.0 V and 7.0 V. b. SRO line width 20 μm, voltage limits -5.0 V and 6.5 V. c. SRO line width 50 μm, voltage limits -7.0 V and 8.0 V. d. SRO line width 100 μm, voltage limits -6.0 V and 7.0 V.

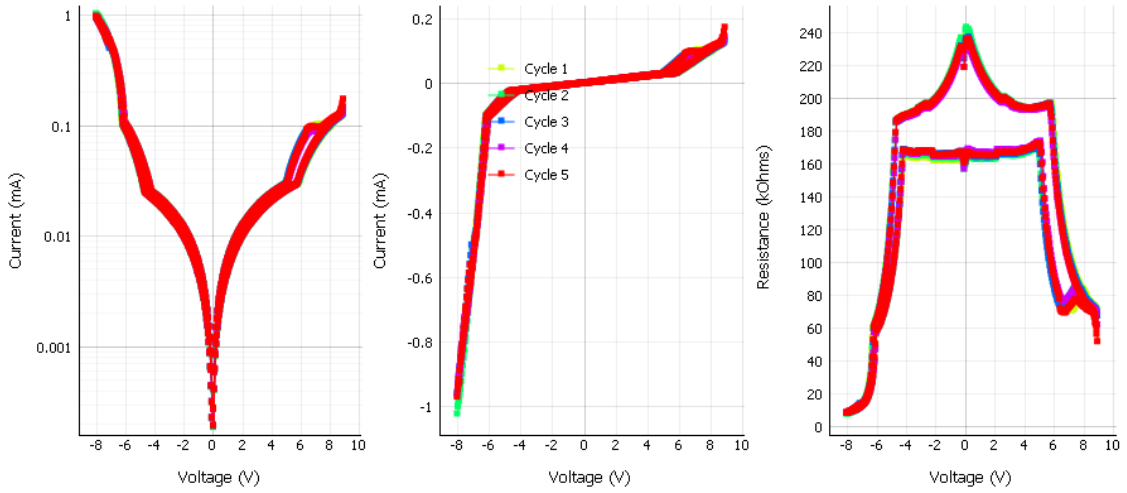

Figure 32. CurveTracer, i.e., an IV measurement with logarithmic IV and RV curves generated from it, of Sample 5, SRO line width 100 μm and voltage limits -8.0 V and 9.0 V.

the start of the optimization process. The cause of this happening is the type of the contact changing a bit as the interface layer is affected by the chosen fabrication methods. If the SRO stripe is of poor quality, the GCMO can not grow properly on top of it, causing the type of the contact to be more Ohmic in nature. The poorly grown GCMO might contain pinholes, providing an unwanted path for the current directly from one electrode to another.

The retention of the states was impressive for one of the contacts of SRO line width of 100 μm: Over the 5 hour period after applying positive or negative voltage pulses, the reached resistance states remained almost perfectly. The IV and RV curves of the studied device are presented in Fig. 32, and the results from Retention in Fig. 33. As we can see from the figures, the states of 160 kΩ and 120 kΩ did not change significantly over the measurement period.

As the HRS and the LRS were more stable and further away from each other, we were able to utilize the MultiStateSeeker. As seen from Fig. 34, a remarkable number of separate states were accessible on the device on two separate measurements. Interestingly, the upper end of the found states was a lot higher than the HRS

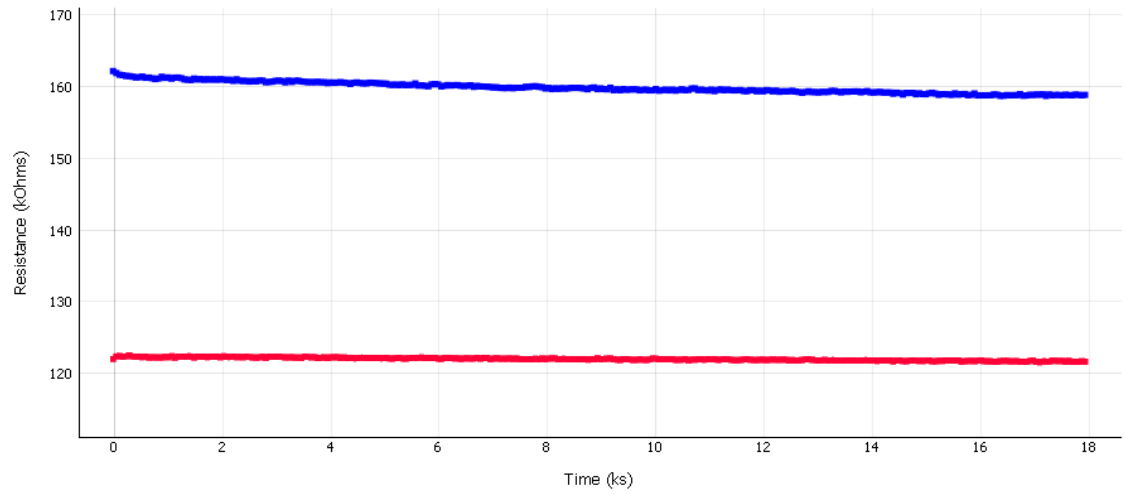

Figure 33. Sample 5, Retention measured for 5 hours after applied voltage pulses on a device with SRO line width 100 μm, device CurveTracer shown in Fig. 32). Top (blue) curve measured after 12.0 V applied voltage pulses, bottom (red) curve measured after -11.5 V applied voltage pulses.

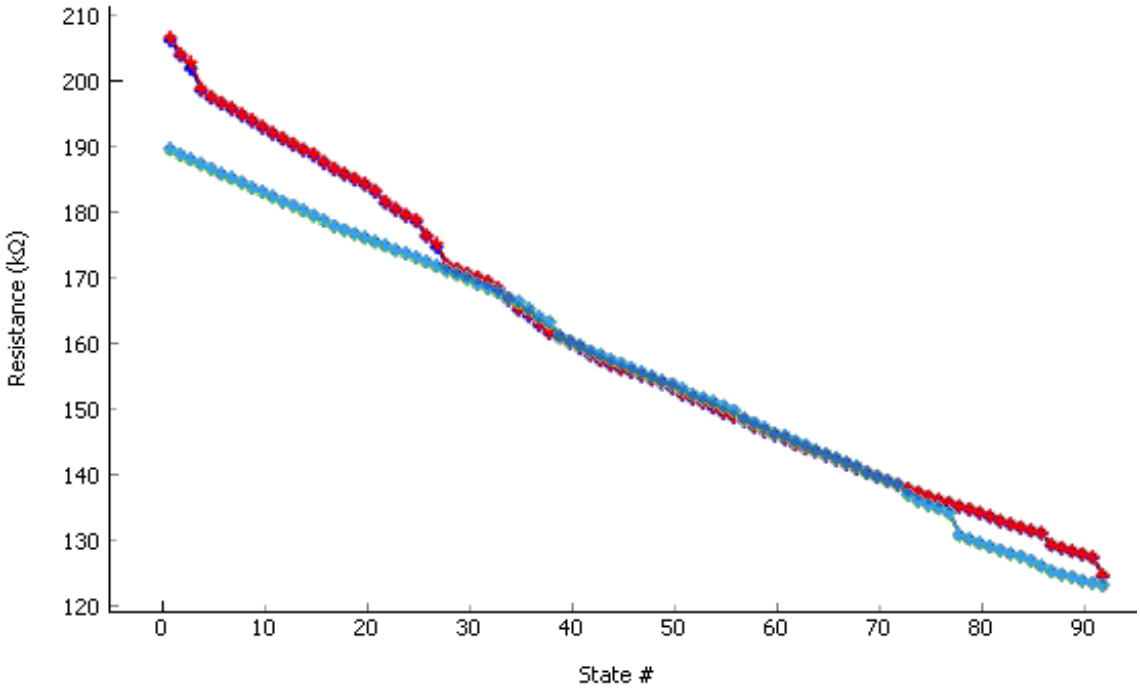

Figure 34. Sample 5, MultiStateSeeker measurement executed two separate times, the red curve being the first of the two, on a device with SRO line width 100 μm, device CurveTracer shown in Fig. 32.

Table VII. The resistances in Ω of the devices of Sample 5, categorized by the bit- and wordlines.

Bit-/wordline	**W10**	**W14**	**W18**	**W22**
B1 (100 μm)	1.568×10^4	1.560×10^3	1.762×10^3	2.222×10^5
B4 (10 μm)	1.869×10^6	2.124×10^5	2.720×10^4	1.236×10^5
B5 (100 μm)	8.460×10^2	1.776×10^3	1.791×10^4	7.992×10^5
B8 (10 μm)	1.354×10^6	1.357×10^6	8.358×10^4	4.386×10^5
B9 (50 μm)	1.784×10^3	4.512×10^3	4.643×10^4	1.913×10^6
B12 (20 μm)	7.812×10^5	4.506×10^4	1.002×10^4	2.176×10^7
B13 (20 μm)	9.830×10^3	3.215×10^5	6.031×10^6	6.705×10^7
B16 (20 μm)	1.153×10^6	1.012×10^6	2.223×10^4	1.126×10^5
B20 (50 μm)	7.864×10^5	3.369×10^5	2.575×10^3	9.942×10^4
B24 (50 μm)	2.782×10^4	2.499×10^3	1.886×10^3	8.291×10^5
B28 (100 μm)	5.325×10^5	1.881×10^5	2.383×10^3	1.606×10^4

reached in retention measurement. The limit seemed to slightly drop for the second MultiStateSeeker measurement, from 120 kΩ to 190 kΩ, even though the number of found states remained approximately the same, a bit over 90 states. Some shifting of the reachable resistances is expected from the devices, as they are used and tested more.

As more of the contacts worked somewhat well, we were able to see a connection between the area of the capacitive device and the resistance of the device, a smaller area causing in general a higher resistance. The correlation was visible even though there was huge variation of the values and quite a small sample of unique devices. The fabricated sample should contain 16 separate devices (GCMO pads), but as there were multiple connections bonded to the SRO stripes, the same GCMO pads were accessed from different sides or from the same side with two SRO stripes passing under the same GCMO pad. This caused there to be more data points to collect

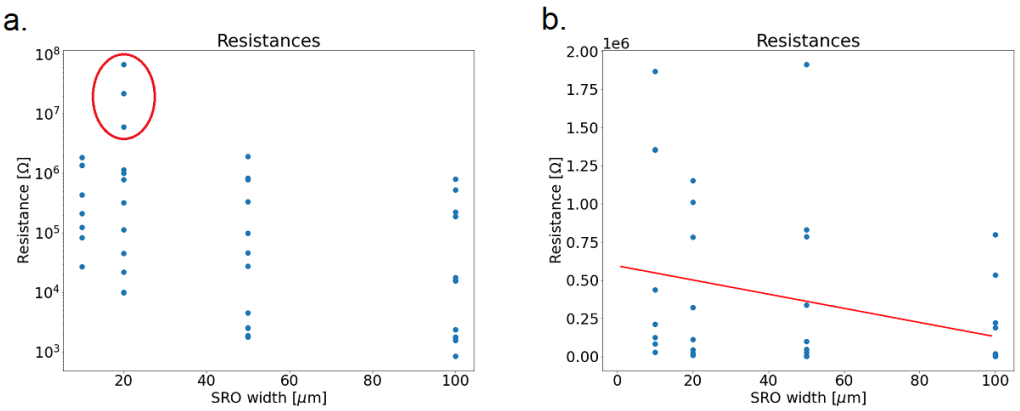

Figure 35. General resistances of Sample 5 devices in relation to SRO line width 10 μm, 20 μm, 50 μm, and 100 μm. a. All of the data points b. Three largest outlying values (circled in red in a.) removed from the SRO line width 20 μm, linear fit of the rest of the data points.

the resistances from, but at the same time it caused unreliability in the correlation calculations. The general resistance values of the devices, not specifically being the HRS or the LRS, were collected in Table VII. Fig. 35 shows the resistances of specific size SRO stripes against each other with three outliers from 20 μm SRO circled in red and the same values with the outliers removed and a linear fit. Looking at the trends of the resistances we can notice a somewhat linear dependence in the resistance values in relation to the SRO width and contact area. Comparing these resistances to the previously achieved resistances of working memristors, e.g., for a planar GCMO-memristor a general resistance from $10^6\,\Omega$ to $10^7\,\Omega$ [7], we see that the resistances of smaller contact area devices come closer to the same values.

Because the resistance values discussed in the last paragraph were not clearly at the HRS or the LRS, some additional measuring was done to find out the ratio of the states, the value of the LRS compared to the HRS. The general percentage of the LRS compared to the HRS was around 70 % for all of the SRO widths, meaning that most of the time the LRS was basically the same order of magnitude as the HRS. This does not reflect the results of the planar GCMO-based memristors, for which the LRS was only about 1 % of the HRS [7].

As the results for Sample 5 were still not perfect due to the high variance of resistances of devices of the same contact area, some optimization of the fabrication process could be done in the future. One layer we did not optimize much during the process of this thesis was the Al layer. As the interface of GCMO and Al is the place of interest, i.e., resistive switching happens there, we should try to optimize the fabrication of Al as well. One way to improve the quality of the interface is to heat up the sample before the deposition of Al, as heating would burn off the reminiscent materials of the photolithography process on top of the GCMO layer. Another improvement could be switching the fabrication of the Al layer to lift-off, where a similar photoresist layer would be applied as a guide to the Al stripes, thus eliminating the need for the shadow mask when depositing Al with E-beam. As we saw with PLD, shadow masks are not the best option when trying to fabricate small patterns on the sample due to the edges disturbing the deposition. This, or the possibility of the mask partly ripping out the material when removed, could also be the cause of imperfect samples when using E-beam.

5 Summary and conclusions

The fabrication process of a capacitive GCMO-based memristor was optimized in this thesis. The fabrication methods examined and experimented with during the process were PLD, E-beam, photolithography and etching, and different combinations of these. Many previously unknown side effects of the specific methods were discovered throughout the measurements, for example the roughness of the pattern edges produced by the PLD shadow mask. Different difficulties were also faced with photolithography and etching, but in general they proved to be the better option when wanting to pattern small details out of the thin films.

There is a clear path in the results of the optimization process: Initially, the first sample showed some promising properties when tested, but no clear and usable

Table VIII. The chosen memristive quality parameters of Sample 5 and a planar GCMO counterpart [7].

Quality parameter	**planar GCMO**	**capacitive GCMO**
IV asymmetry (Difference/higher limit)	Example limits: $\frac{7.0\,\mathrm{V}-(-4.0\,\mathrm{V})}{7.0\,\mathrm{V}} = 1.6$	Example limits: $\frac{10.0\,\mathrm{V}-(-8.0\,\mathrm{V})}{10.0\,\mathrm{V}} = 1.8$
General resistance	$10^6\,\Omega$ to $10^7\,\Omega$	$10^4\,\Omega$ to $10^6\,\Omega$
LRS/HRS	0.1 % to 1 %	70 % to 80 %

resistive switching could be found. The controlling of the resistance states of the devices was nearly impossible, as the applied voltages could also affect the neighboring devices unintentionally. With etched SRO we were able to get rid of the linked breaking of the devices. The switching of SRO fabrication method to etching provided us with capacitive devices of different contact areas and some resistive switching, but no real correlation between the resistances and the areas of the contacts could be seen in the results due to the high instability of the resistance states. This was possible in the last phase, switching the fabrication of GCMO also to photolithography. With the last sample we were able to detect some resistive switching in most of the fabricated devices, and the devices were more easily controlled with voltage pulses.

The final sample, Sample 5, achieved quite good results for the chosen memristive quality parameters: the asymmetry of the IV curve, the general resistance level, and the ratio of the LRS and the HRS. These results are collected in Table VIII. To note, the asymmetry was calculated by dividing the difference of the voltage limits with the higher amplitude limit. Value of 2.0 for the IV asymmetry denotes a completely symmetrical curve, anything less increasing asymmetry. To determine whether a good result for the properties was achieved, the same qualities of the planar counterpart, GCMO (x = 0.8) -based memristor from Lähteenlahti *et al.* [7] were added in the same table. For our sample, the example voltage limits were

chosen from the 100 μm width SRO device, of which the IV curve is presented in Fig. 32. For the planar GCMO-based memristor, the values were collected from Fig. 3 of the article [7]. As we can see, all criteria were achieved at least partly, but not fully. Especially the result of higher symmetry of our IV curves could mean that unwanted conduction mechanisms take place or even dominate in our fabricated devices. Unless this can be fixed, there might not be a way to increase the difference between the LRS and the HRS.

Comparing these results with the previous measurements done with planar and capacitive PCMO-based memristors [17, 18], we can see that the results have room for improvement, but that they are, as a whole, promising. From the PCMO comparisons, we suspected the capacitive GCMO to work in a similar way as the planar GCMO works, as that was the case for similarly fabricated PCMO-based memristors. Planar GCMO has bipolar tendencies, and the LRS is usually around 1 % of the value of the HRS. For our samples, some weak asymmetry, thus possible bipolarity, can be seen from the measured IV curves. The difference from the LRS to the HRS was unfortunately a lot smaller than what was hoped for, the LRS being around 70 % of the HRS. Some unwanted linearity of the IV curves also persisted up to the final results, pointing to the conclusion that some Ohmic-like conduction happens in the material. This Ohmic-like behavior of the contact could be due to pinholes in the GCMO layer, providing a direct contact of the electrodes, from the SRO layer to the Al layer. As mentioned previously, the pinholes could be the result of a poorly grown GCMO on top of an uneven SRO layer.

As with any process, there is some room for further optimization. The SRO and GCMO layers were fabricated with PLD, but another alternative for the fabrication of full thin films would be chemical spin coating, in which the fluid coating materials are spread over the flat surface by spinning the substrate. As briefly discussed before, the fabrication of the Al stripes could be improved by switching it to the

lift-off method. Another option is once again photolithography, as etching of Al is possible, for example, with ferric chloride ($FeCl_3$) [42], but $FeCl_3$ also acts as an etchant for GCMO. A better etchant for our case could then be hydrofluoric acid (HF), as it etches Al but not GCMO or SRO. Etched Al could even result in a better Al-GCMO interface, as the surface of GCMO can be heat treated before the deposition of a full layer of Al. With lift-off, the heat treating is impossible due to the photoresist burning off before it is needed in the deposition process. Furthermore, etching could provide us with as thin stripes as is possible to fabricate with lift-off. Also the contact area of the device should be switched to a square one, i.e., equal line widths of SRO and Al, as the highly uneven widths could limit the behavior of the device. The SRO and GCMO layers could also be fabricated sequentially, etching both layers afterwards, as the chosen etchants for those materials do not affect the other. Some insulating material is then needed to cover the empty areas of the surface to limit short circuiting before adding the Al stripes, e.g., with lift-off or another chosen method. As the most used substrate material in the industry is silicon (Si) and not STO, the fabrication of the capacitive structures should be also tested on Si wafers. The wafers are usually also larger in size, so that should be taken into account when making the thin films.

When the fabrication methods of the thin film layers are optimized and a working capacitive GCMO-based memristor is achieved, the fine tuning of the fabrication method parameters can be done. This includes for example the thicknesses of the layers and the widths and areas of the stripes and contacts. After that, the full crossbar array memristor can be studied and measured to provide us with a starting point for brain-inspired neuromorphic computing.

As memristive devices, especially GCMO-based ones, have properties resembling the behavior of both synapses and neurons, they can be used as the hardware implementation of a neuromorphic computer. Larger scale crossbar arrays can be used

for matrix calculations, in-memory parallel computations, suitable for example for deep learning and spiking neural networks. [43–45]

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