An ECG Processor for the Detection of Eight Cardiac Arrhythmias with Minimum False Alarms

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***Abstract*— An Electrocardiography (ECG) based processor for eight Cardiac arrhythmias (CA) detection with smart priority logic is presented to minimize the false alarms. The processor utilizes a Multi-Level Linear Support Vector Machine (ML-LSVM) classifiers with one-vs-all approach to distinguish the different CAs. The classification is solely based on 5 features including R-wave, S-wave, T-wave, R-R interval and Q-S interval. The processor employs a priority logic to prioritize the detected conditions if more than one condition are detected. The system is implemented using CMOS 180nm with an area of 0.18mm^2 and validated using 83 patient's recordings from Physionet Arrhythmia Database and Creighton University Database. The proposed processor consumes 0.91uW with an average classification accuracy of 98.5% while reducing the false alarms by 99%, which is 30% superior performance compared to conventional systems.**

Keywords*— *Electrocardiography (ECG), Ventricular arrhythmias, Atrial Arrhythmias, Multi-Level support-vector-machine (ML-SVM), False alarms, wearable sensor.

I. Introduction

Cardiovascular Diseases (CVDs) are chronic heart conditions and considered as the most fatal among all the chronic disorders with ~17.9 million people died; only in 2016 [1]. Cardiac arrhythmia (CA) is responsible for almost 80% of sudden cardiac arrests and is the most recurrent among all of the CVDs. It is caused when the heart beats irregularly, too rapidly and too steadily [2], [3]. CA's can be categorized into five arrhythmias, 1) Sinus node arrhythmias, 2) Atrial arrhythmias (AA's), 3) Junctional arrhythmias, 4) Ventricular arrhythmias (VA's), and 5) Atrioventricular blocks. Nevertheless, the most common and critical among CAs are AA and VA, respectively [4].

AA's also known as Supraventricular Tachycardia (SVT) originates in upper chambers of the heart (Atria) and cause abnormally fast heartbeats. Typically, patients have symptoms from SVT, but occasionally they may have no symptoms [4]. A common symptom during SVT is palpitations or a sensation that the heart is beating rapidly, fluttering, or racing. SVTs are one of the most frequent causes of emergency department and physician office visits. Although most cases of SVT are not considered dangerous or life-threatening, frequent episodes can weaken the cardiac muscle over time, and should, therefore, be addressed with medical intervention to prevent further complications. AA can be classified into 1) Atrial tachycardia (AT), 2) Atrial Flutter (AFL), and 3) Atrial fibrillation (AFIB). On the other hand, VA's originates in lower chambers (Ventricles) of the heart leading to abnormal rapid heartbeats [6] and less cardiac output, which prevents oxygen-rich blood from circulating to the brain and body and may cause cardiac arrest [4]-[6]. The types of VA include 1) Premature ventricular contractions (PVCs), 2) Ventricular fibrillation (VFIB), 3) Ventricular tachycardia (VT), and 4) Ventricular Flutter (VF). An idioventricular rhythm (IDIO) is very similar to VT except the heart rate is less than 60 bpm.

The general medical practice for CVDs detection relies on interviewing the patients and through the analysis of the heart's electrical activity (Electrocardiograms (ECG)). Since the occurrence of most of these CA is intermittent, there is no guarantee that CA can be diagnosed during the ECG recording at the hospital. Therefore, a wearable and long-term ECG monitoring device is indispensable with the ability to detect CA.

Wearable sensing solutions such as multiple-leads Holter monitors are opted vastly [7], however, the operating time is limited for few days (< 3 days) and lacks on sensor processing. Implantable Cardiac Monitors (ICM) emerged as a solution for continuous heart-monitoring but the invasive nature is the major bottleneck for their usage [8]. Real-time continuous monitoring devices based on cognitive clocking can decrease the power consumption but they lack the CAs detection [9]. Machine Learning has played a vital role in classifying complex datasets with the help of support vector machine (SVM) [10]. Ref. [11] presents a PVC detection system using a Wave-Based Bayesian Framework with an average accuracy of 99.1% but fails to identify other types of CAs. For CAs classification, multiple features have been proposed in the literature ranging from spectral, temporal and complexity measure of the ECG signal [12]. Similarly, machine learning techniques like convolutional neural networks (CNN) and SVM have been recently implemented to classify CA conditions [10], [12]. While these algorithms exhibit high classification accuracy for arrhythmias like PVC and VT, they usually come at the expense of exponentially high computational power and hardware infrastructure. Moreover, CNN and non-linear SVM requires both complex arithmetic operations and high on-chip memory to store the learned parameters for classification, which increase the area-and-power requirements significantly [13].

This paper proposes the first wearable CA detection processor to detect 8 types of arrhythmias with highest classification accuracy and minimum false alarm. The proposed CA detection utilizes one vs all (O-vs-A) multi-SVM classifier, and patient-adaptive false alarm reduction logic (PAFARL) to enhance the classification accuracy to 98.5%. The anomalous ECG data will be stored on chip (SRAM) for future analysis by the concerned physician.

II. Proposed ECG Classification Algorithm

The overall block diagram of the single-lead ECG system on Chip (SoC) for the early detection of CAs is shown in Fig. 1. The ECG signal will be acquired using the analog front end; digitized using SAR ADC and finally, it will be processed to detect the CAs. The contribution of this work is mainly the CA detection processor, which is the first classifier to distinguish 8 CAs implemented on-chip. It is based on an optimized feature set and machine learning classifier as described below.

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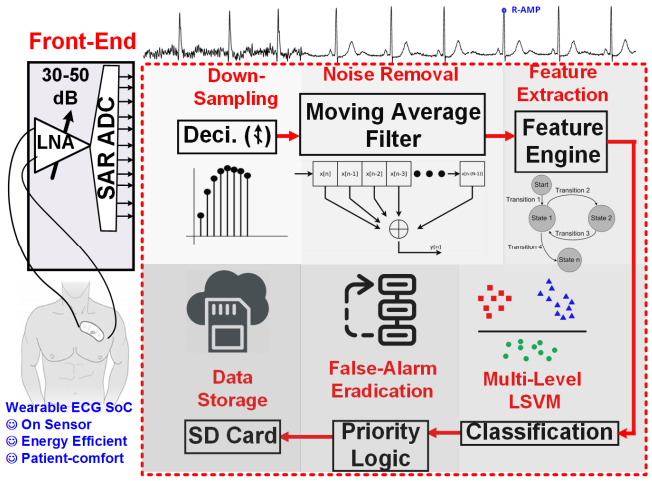

Fig. 1: Proposed wearable ECG SoC for the AA and VA prediction.

A. Proposed Feature Extraction

The minimum essential feature set consists of 5 features: R-wave amplitude (R_{AMP}), S-wave amplitude (S_{AMP}), T-wave amplitude (T_{AMP}), R-R interval (RR_{INT}), and Q-S interval (QS_{INT}). Since all of these features are based on the amplitude of the ECG signal, which can vary from patient-to-patient, the proposed feature extraction is designed to be robust and adaptive using a simple threshold logic. It utilizes the slope variation method for wave detection in a certain window of the ECG signal. Fig. 2 describes the state flow diagram of the proposed feature extraction algorithm. Initially, for calculating the R_{WAVE}, the threshold (RTH) is computed in the 'state 0' by averaging out 2-sec absolute data. Then, the incoming data (ID) is compared against the RTH to evaluate the R_{WAVE} that is the dominant component of the QRS complex. The RTH can differ from patient to patient; therefore, a self-adaptive structure is adapted to make it more rigorous against amplitude and beat-frequency variations. After the R_{WAVE} is detected, it moves to 'state 1', which identifies the deflection of the QRS complex. If the QRS complex is negative as compared to the T_{AMP}, it directly transfers to the 'state 3' to detect the 3rd feature i.e. T_{AMP} by bypassing 'state 2'. If the QRS complex is positive, then it goes to detect S_{AMP} in the 'state 2' with the help of slope change method. The algorithm reaches to 'state 4' after at least one T_{AMP} is detected. In ECG tracings Q_{AMP} is the negative wave which comes after T_{AMP} but before R_{AMP}. Q_{AMP} is also identified with the help of slope change method, it detects the most negative amplitude between previous T_{AMP} and next R_{AMP}. The proposed Q_{WAVE} detection makes it more accurate compared to [2], by choosing a specific window considering QRS complex deflection. Multiple counters are operating on parallel to count the detected R_{AMP}, Q_{AMP}, and S_{AMP}, peaks and the system goes into 'state 5' when the sum of counters reach a count value of 2. RR_{INT} and QS_{INT} are computed in this state, and once all five features are detected, the system will go to sleep state and wait for next QRS to arrive.

B. Machine Learning based Prediction Processor

In the proposed algorithm, linear SVM is preferred over CNN and nonlinear SVM to achieve area-and-power efficient implementation, as linear SVM does not require the support vectors or enormous parameters to be uploaded on-sensor for processing at run time.

The extracted features are passed through a multi-classification binary LSVM algorithm to distinguish multiple arrhythmia conditions (AFL, AFIB, PVC, VT, VFL, VFIB, VF, and IDIO) using an O-vs-A multi SVM system. SVMs are inherently binary in nature but can be utilized to separate multiple boundary problems. The two common adopted techniques are O-vs-A and one vs one (O-vs-O). Fig. 3 shows the trade-off between O-vs-A and O-vs-O for on-chip implementation, and classification accuracy and training. O-vs-A is preferable compared to O-vs-O approach since it 1) allows multiple CAs to exist in parallel, 2) supports on-chip implementation in term of hardware utilization and 3) utilizes off-sensor training. Furthermore, O-vs-O approach requires more computations and larger memory on-chip. To produce a final decision of the multi-level SVM classifiers, the proposed PAFARL decides between VA/AA based on the severity of the detected conditions in order to reduce false alarms. The training process is done offline with the help of MATLAB to reduce computational power.

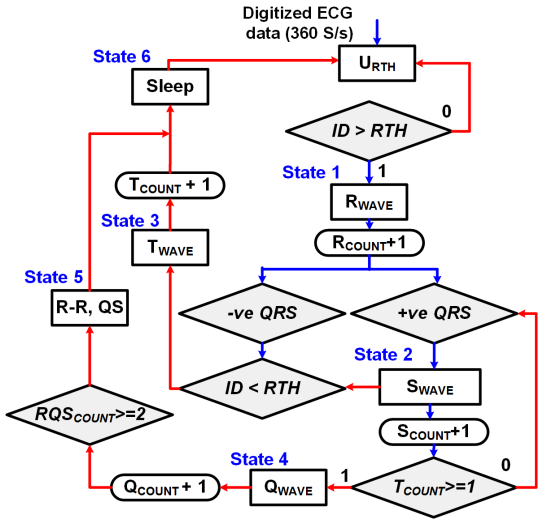

Fig. 2: Proposed single EEG channel feature extraction block.

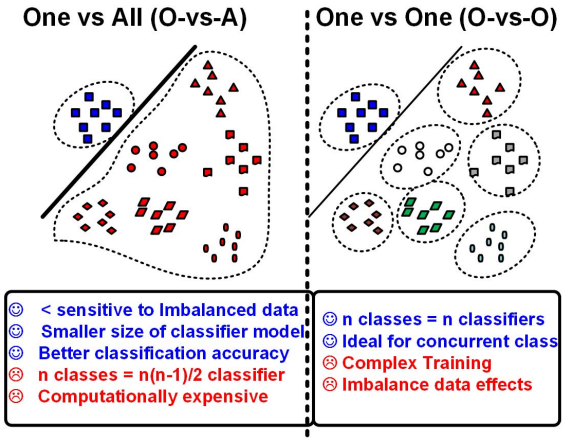

Fig. 3: Comparison between O-vs-A and O-vs-O classification methods.

C. Patient Adaptive False Alarm Reduction Logic

Multiple parallel decisions from the multi-classification block are fed into priority logic block. The main purpose of this block is to give importance to an arrhythmia, which is more critical at a specific time in order to treat it on early

stages. Since VAs are more critical compared to AAs, the co-existence of any VAs and AAs will alarm for VA only. Fig. 4 demonstrates examples of the operation of the proposed priority logic in reducing the false alarm for a hypothetical ECG trace. The detection of AFL condition after the occurrence of AFIB is insignificant and can be considered as a false alarm since AFIB is a more advanced condition of AFL [4]. Another scenario is shown in Fig. 4 with IDIO and VFL being detected at the same time. In this case, the PAFARL will assign priority to the serious one, which is VFL. Another case of AA's is shown, where AFL and AFIB are occurring parallel, in this situation, the PAFARL logic will prioritize AFIB.

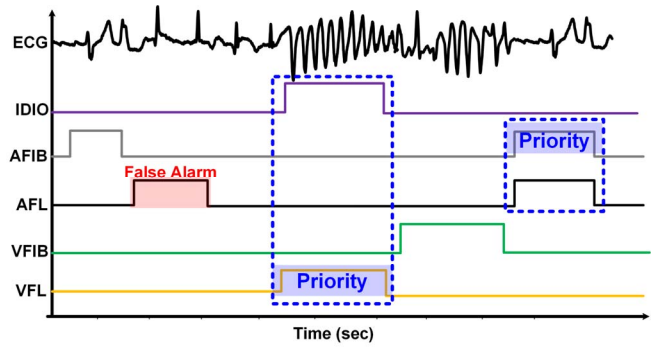

Fig. 4: Examples of the operation of the PAFARL block.

III. Proposed ECG Classification Processor

The ECG data with a sampling frequency of 360 S/s from an 11-bits ADC, is processed for filtering and noise removing, feature extraction and classification. The Feature extraction engine implementation is modified version of ref [5] and working flow is shown in Fig. 2. The engine is exclusively based on comparators and simple ALU blocks. The proposed system divides the incoming ECG signal into 2-sec windows having 720 samples. The 2-sec window is further divided into smaller sub-windows i.e. Q, S, and T-windows. Each of these sub-windows can store 64 samples. The local maxima is identified once the incoming signal reaches a maximum amplitude in the selected sub-window by comparing each sample with the succeeding and preceding samples to monitor the changes in the slope. For local minima, a similar procedure of finding local maxima is applied but it searches for the minimum amplitude in the selected sub-window. Both local maxima and local minima are computed using the same block to reduce the hardware resources. The counters for R, S, T, Q waves are incremented by 1 every time these waves are detected. The RR_{INT} and QRS_{INT} are computed when the counters of R, S, T, Q reaches to 2 or more. Therefore, the proposed implementation technique is more efficient compared to the conventional methods [2],[5] of calculating these intervals since its scrutinizing in sub-windows instead of time stamps before and after R_{AMP}.

The implementation of multi-class linear SVM and priority logic block are represented in Fig. 5. Eight weight vector (5 dimensions) and biases are computed and stored offline based on data from ECG Physionet databases [14], [15]. The binary training for each of VA's and AA's are applied offline separately. The biases and weights are exported and passed to a classification block in parallel along with the five features extracted from the feature extraction engine.

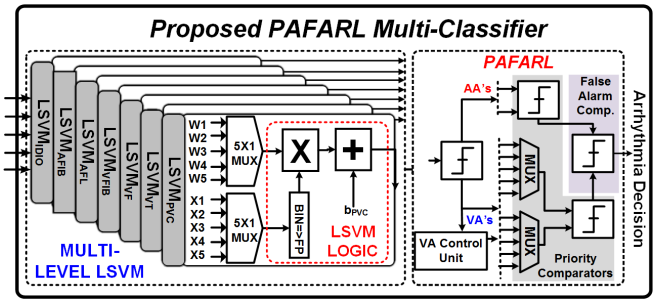

Fig. 5: The block diagram of the Multi-Level SVM Classifier processor.

All of the Multi-level LSVM results are calculated in parallel are defined by (1) [16]. To optimize the patient-specific decision boundary between specific arrhythmia and non-arrhythmia, the eight copies of LSVM classifiers are utilized, one for each arrhythmia condition.

$$W^T . K(x) + \beta = \begin{pmatrix} > 0 & \text{Arrhythmia} \\ < 0 & \text{No Arrhythmia} \end{pmatrix} \quad (1)$$

where in (1), W (the normal vector to the hyper-plane) and β (determines the offset of hyper-plane, i.e.$\beta/\|W\|$) is the patient-specific parameters and $K(x)$ is the incoming feature vector extracted from the incoming ECG data. The feature vector '$K(x)$' and normal vector 'W' are 5-dimensional vectors in the implementation, separated by a 4 dimension hyperplane for classification. The multiple decisions produced concurrently from the classification block are fed into the priority logic block. The reliability of our system depends on this block since it can give false alarms and at the same time, it can detect correctly. For that, it is designed in a way that it can reevaluate detection results based on a defined priority criterion which help in reducing the false alarm in real time. For example, if AA and VA come at the same time then it prioritizes them and give the priority to the critical one. Priorities are given as in (2), showing VFIB get the highest priority [4].

$$AFL < AFIB < PVC < VT < IDIO < VF < VFIB \quad (2)$$

IV. Measurement Results and Discussion

The proposed CA detection processor is implemented using CMOS 180nm process with an active area of 0.18mm^2 as shown in Fig. 6. The overall power consumption for 8 CA classification processor is 0.91uW @ 1 KHz. The performance validation is based on two different databases from Physionet, (MIT-BIH Arrhythmia Database [14] and Creighton University Ventricular Tachyarrhythmia Database [15]). The MIT-BIH Arrhythmia Database consists of 48 records and each of them is of approximately 30 minutes. While the Creighton University database has 35 records and each of them is of approx. 8 minutes.

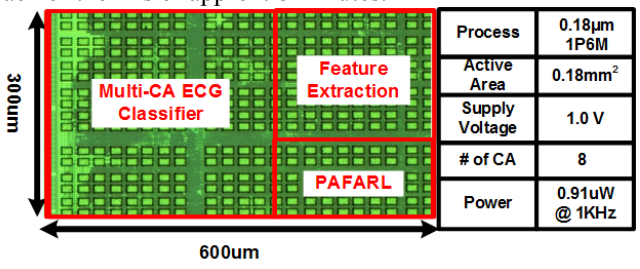

Fig. 6: Die photo and performance summary.

The measurement of the processor performance is shown in Fig. 7, where the abnormal VFIB and AFIB patterns are correctly identified by our implemented processor.

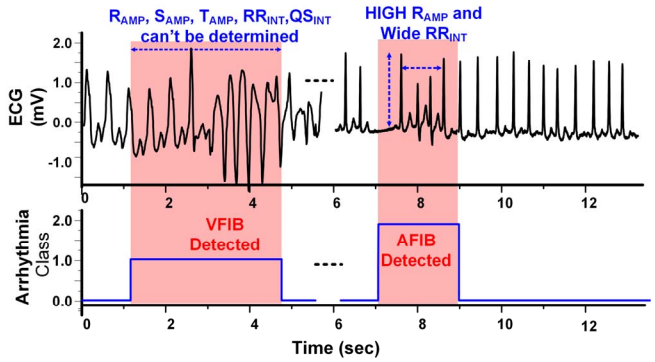

Fig. 7: Measurement results of the proposed CA detection processor.

The proposed processor yields an overall average accuracy of 98.5% with false alarm reduction of up to 99% compared to the state of the art works [17], [18]. It enhances the reduction of false alarms by 30% compared to work in [12]. Fig. 8 shows the detailed analysis of confusion matrix of each individual CA condition. The comparison with state of the art works along with implemented work is depicted in TABLE I. This work is the first ECG processor implemented on chip to detect eight (8) CA with significant high classification accuracy.

AFIB	Predicted 0	Predicted 1
Actual 0	97.86%	2.14%
Actual 1	6.74%	93.26%

AFL	Predicted 0	Predicted 1
Actual 0	99.77%	0.23%
Actual 1	0	100

VF	Predicted 0	Predicted 1
Actual 0	100%	0%
Actual 1	1.79%	98.21%

VT	Predicted 0	Predicted 1
Actual 0	99.43%	0.57%
Actual 1	0.98%	99.02%

IDIO	Predicted 0	Predicted 1
Actual 0	100%	0
Actual 1	2.9%	97.1%

VFIB	Predicted 0	Predicted 1
Actual 0	98.7%	1.3%
Actual 1	1%	99%

AT	Predicted 0	Predicted 1
Actual 0	100%	0
Actual 1	0	100%

PVC	Predicted 0	Predicted 1
Actual 0	99.3%	0.7%
Actual 1	0.9%	99.1%

Fig. 8: Confusion matrix of all binary LSVM classifiers.

V. Conclusion

An area and power-efficient processor for CAs detection with a priority logic to reduce the false alarms is presented. The proposed processor utilizes 5 features and multi-level LSVM classifier to distinguish 8 types of CAs. It is implemented using 180nm CMOS and provides an average accuracy of 98.5% for 83 patients. IT also reduces the false alarms up to 99% with a power consumption of 0.91uW.

Acknowledgment

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Table 1: Comparison with the state-of-at processors for CA classification.

	Q. Li, TBME'14 [10]	S. Fallet, CinC'15 [12]	D. Jeon, ISSSC'14 [8]	S. Abu., ASSCC'18 [5]	This Work
Technology	X	X	65nm Implantable	65nm Simulations	180nm
# Arrhythmia's Detected	2	N/A	Real-time Detection	2	8
Classifier	SVM	-	Threshold	Threshold	Multi-Level SVM
Accuracy	96.3%	X	-	98.66% Se, 99.75% Sp	98.5%
False Alarm Reduction	X	76.11	X	X	99%
Power	X	X	45nW	115.5nW	5.36uW
Database	CUDB, AHA, MIT-BIH	PhysioNet Challenge	Recruited	MIT-BIH	MIT-BIH, Creighton Uni.

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