Oxidation-Induced Changes in the ALD-Al_2O_3/InAs(100) Interface and Control of the Changes for Device Processing

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ABSTRACT

InAs crystals are emerging materials for various devices like radio-frequency transistors and infrared sensors. Control of oxidation-induced changes is essential for decreasing amounts of the harmful InAs surface (or interface) defects because it is hard to avoid the energetically favored oxidation of InAs surface parts in device processing. We have characterized atomic-layer-deposition (ALD) grown Al_2O_3/InAs interfaces, pre-oxidized

differently, with synchrotron hard x-ray photoelectron spectroscopy (HAXPES), low-energy electron diffraction, scanning tunneling microscopy, and time-of-flight elastic recoil detection analysis. The chemical environment and core-level shifts are clarified for well-embedded InAs interfaces (12 nm Al_2O_3) to avoid, in particular, effects of a significant potential change at the vacuum-solid interface. High-resolution As 3d spectra reveal that the Al_2O_3/InAs interface, which was sputter-cleaned before ALD, includes +1.0 eV shift, whereas As 3d of the pre-oxidized (3×1)-O interface exhibits a shift of -0.51 eV. The measurements also indicate that an As_2O_3 type structure is not crucial in controlling defect densities. Regarding In 4d measurements, the sputtered InAs interface includes only a +0.29 eV shift, while the In 4d shift around -0.3 eV is found to be inherent for the crystalline oxidized interfaces. Thus, the negative shifts, which have been usually associated with dangling bonds, are not necessarily an indication of such point defects as previously expected. In contrast, the negative shifts can arise from bonding with O atoms. Therefore, specific care should be directed in determining the bulk-component positions in photoelectron studies. Finally, we present an approach to transfer the InAs oxidation results to a device process of high electron mobility transistors (HEMT) using an As-rich III-V surface and In deposition. The approach is found to decrease a gate leakage current of HEMT without losing the gate controllability.

INTRODUCTION

Oxide/III-V-semiconductor interfaces play a key role in several electronic devices like transistors, photodetectors, solar cells, and light-emitting diodes (LED).[1-8] Unfortunately, these interfaces are naturally very defect-rich as compared to bulk-crystal parts beneath the surfaces and, thus, tend to degrade the device performance. Despite of the extensive work in the field, various etching and passivation methods have been inefficient in reducing the III-V interface defect density to industrial standards set by today's silicon technology.[9-15] This is a

drawback to be overcome, as with III-V's intrinsic properties, it is possible to manufacture devices having remarkably low power consumption and high operation frequencies. III-V surface oxidation is thermodynamically a very favored reaction and it can happen uncontrollably if the surface is exposed to any oxygen-containing environment, even for a short period of time (e.g., less than one second). Such oxidation-induced changes usually cause a high density of point defects at the oxidized semiconductor side, which in turn cause electronic defect levels in the semiconductor band gap region.[16-18]

Minimizing the interface defect state density (D_{it}) at the oxide/III-V interface region is thus an instrument to develop III-V devices further.[19-24] Oxidation-induced defects have been usually associated with vacancies, dimers, and/or substitutional non-isoelectronic atoms (i.e., atoms with different amounts of valence electrons). Furthermore, charge carriers are easily trapped in such defects, causing changes in the operation voltage and making the device operation unstable as the degree of trapping fluctuates. The trapped charges can also scatter charge carriers and thereby lower the carrier mobility. Moreover, the interface defect states lead to undesirable non-radiative recombination of charge carriers resulting in energy losses and degraded operation performance.[25-27] Defects are often the starting point for further electrical failure and oxide breakdown in general. In the aim of reducing D_{it}, it is important to investigate and modify the interface chemistry on an atomic scale.

Many studies have targeted at the D_{it} reduction since the 1970's.[28] For example, D_{it} of 10^{12} $cm^{-2}eV^{-1}$ was obtained, if the interface was kept free of arsenic oxides by the cleaning-effect that occurs during atomic-layer-deposition (ALD) growth of Al_2O_3.[29] However, sources of defect levels can remain if thermally stable In_2O_3 and Ga_2O_3 oxide phases stay at the interface.[27,30] Recently, D_{it} of the same order was obtained also by Babadi *et al*. with hydrofluoric acid (HF) etching and alternating cycles of nitrogen plasma and trimethyl aluminum (TMA) before depositing HfO_2 or ZrO_2 dielectric films on InAs(100).[31]

Trinh *et al.* also succeeded in reducing the D_{it} level to 10^{12} $cm^{-2}eV^{-1}$ range in HfO_2/InAs/InGaAs stacks by using HF (49%) and $(NH_4)_2S$ (7%) solution together with post-deposition annealing at 500 ºC in forming gas.[32] In this case, the presence of In_2O_3 was detected still at the interface. A similar reduction in D_{it} was observed at Al_2O_3/InGaAs interface by using $(NH_4)_2S$ treatment before ALD-Al_2O_3 growth together with post-deposition annealing in forming gas (10% H_2).[33] Because D_{it} well below 10^{12} $cm^{-2}eV^{-1}$ is preferred for industrial demands, as obtained for SiO_2/Si,[1,2] further progress in the D_{it} reduction is still needed.

An acceptable level of D_{it} depends on the semiconductor application. For example, field-effect transistors set one of the most stringent levels, as low as 10^9 $cm^{-2}eV^{-1}$ for proper operation, as can be deduced from SiO_2/Si transistors.[1,2,5] Considering still the hurdles in the D_{it} reduction for the III-V interfaces, one key obstacle might be related to the heating tolerance of III-V crystals, which is clearly lower than that of Si. High-quality insulator/Si interfaces have been often heated up to 1000 ºC in atmospheric pressures,[1,5,9-15] which can lead to even an epitaxial SiO_2/Si interface.[12] Indeed after commonly used chemical treatments (e.g., wet etching), a semiconductor surface is usually amorphous rather than crystalline, but the high-temperature post heating can restore the crystal structure at the semiconductor surfaces as well. The difference in the heating tolerance is also reflected in the heating-induced oxide removal between the Si and III-V systems: SiO_2 can be removed from Si at 800-900 ºC in vacuum, while most III-V crystals start to decompose (below 700 ºC) before all their native-oxide phases can be removed in vacuum. This might be one reason why native oxides of III-V's have been so poor as compared to SiO_2, and therefore, the common target has been indeed to avoid the oxidation of III-V surfaces during device processing. This is again easier said than done because the III-V oxidation is an energetically driven process, which occurs anyway at some stage of processing.

We have investigated an alternative technique to control oxide/III-V interface quality.[27,34] In contrast to the common target of avoiding (or minimizing) the oxidation of semiconductor surfaces, we have performed intentional pre-oxidations of semiconductor surfaces in a controlled manner prior to growing the insulator film. Through this method, a clean III-V surface is pre-oxidized in an ultra-high vacuum (UHV) chamber using the parameters that result in a crystalline oxidized layer and limits the effects of subsequent, random oxidation routes in air or during the ALD growth. Specific III-V semiconductor temperature (*T*), oxygen pressure (*p*), and oxidation time (*t*) combinations can be used in an UHV-environment to produce long-range ordered O-containing surface layers with different crystalline symmetries on several III-V(100) surfaces.[34] Other crystalline oxide surface reconstructions have been found also for ternary InGaAs and AlGaN.[30,35] Among the various experimentally determined surface structures, InAs(100)(3×1)-O, InAs(100)*c*(4×2)-O, GaAs(100)-In-*c*(4×2)-O, InGaAs(100)(3×1)-O, InGaAs(100)(3×2)-O, and AlGaN(0001)(1×1)-O have already been proven to decrease D_{it} markedly at oxide/III-V interfaces.[27,30,35-39] For example, D_{it} of 10^{11} $cm^{-2}eV^{-1}$ was obtained in a metal-oxide-semiconductor capacitor if InAs(100)(3×1)-O was used before low temperature ALD-HfO_2 growth.[36] In addition, the photoluminescence intensity of an Al_2O_3/GaAs(100) interface doubled, a direct indication of decreased interface-defect density, when an In deposition and *c*(4×2)-O treatment was carried out.[38] Later, use of this approach provided also a clear increase in quantum efficiency of an infrared photodetector.[27] The (3×1)-O and (3×2)-O crystalline oxide interface layers at a HfO_2/$In0_{.53}Ga_{0.47}As$ heterointerface showed, in turn, a significant passivation effect and D_{it} reduction at metal-oxide-semiconductor capacitors.[30] Moreover, an unstrained InAs fin-field-effect transistor was successfully manufactured by using the (3×1)-O interface layer as an interphase before ZrO_2 dielectric growth, and electron transport properties were reported to match planar InAs technology.[39]

InAs(100)(3×1)-O is so far the most studied crystalline oxidized III-V surface. In this work, we also focus on InAs(100)(3×1)-O, in comparison with other InAs surfaces, because a complete understanding of the InAs(100)(3×1)-O properties might lead to new approaches to develop oxidized III-V surfaces. The first theoretical models were proposed for this surface in Refs. (34 and 40), which explain well the 3× periodicity seen by STM for the topmost surface. However, there is a growing number of indications that InAs(100)(3×1)-O includes a considerably larger O concentration than the first models suggest. It is possible that O atoms are incorporated into several atomic layers below the topmost (3×1)-reconstructed surface part. Such an extended crystalline oxidized layer would explain why the (3×1) periodicity disappears, but the crystalline (1×1) remains still when the ALD growth is started,[41] and why the improvement in device performance remains after the ALD growth.[27,36,37] The extended crystalline oxide layer of InAs would be also consistent with previous high-resolution photoemission measurements from the surface.[42] Thus, the crystalline oxidized III-V layers are probably thicker than the topmost atomic layer.

To advance the knowledge of InAs(100)(3×1)-O further, it is relevant to study the practical insulator/InAs junctions including a well-embedded InAs(100)(3×1)-O interface layer. However, a general problem is probing such buried interface properties on an atomic scale. One useful method has been the photoelectron spectroscopy (PES),[43-51] which provides chemically sensitive changes in the bonding environment at the interface as compared to a well-known reference (usually the bulk emission component from the host semiconductor crystal beneath the surface). This has been presented also for InAs interfaces using high-resolution synchrotron sources.[47-51] Still, a critical issue that needs to be considered in PES measurements and analyses is that it is in fact difficult to determine the bulk-peak position carefully among several possible interface components. To overcome this problem, we have used a state-of-the-art light source to increase the probing depth of the measurements and to

characterize well-embedded interfaces. We have particularly employed hard x-ray photoelectron spectroscopy (HAXPES) to get access to the interface well beneath (12 nm) the vacuum-solid interface, latter of which includes a significant potential change as compared to a potential change at solid-solid interfaces. Although the presented high-resolution HAXPES results are at the heart of this manuscript, the other methods combined here provide crucial complementary information.

EXPERIMENTAL SECTION

10 mm × 6 mm sized samples were cut from commercially available InAs(100) p-type wafer with Zn doping (2×10^{18} cm^{-3}). They were cleaned in an UHV chamber (Omicron) with 4 cycles of Ar-ion sputtering (6×10^{-8} mbar, 1 kV, 10 mA, 300-350 ºC, 40 min) and subsequent indirect annealing at 350-400 ºC. Temperatures were monitored by an infrared pyrometer. The resulting chemistry of the cleaned InAs surfaces was retained as the samples were transferred in UHV conditions to perform low-energy electron diffraction (LEED), scanning tunneling microscopy (STM), and x-ray photoelectron spectroscopy (XPS) pre-characterizations. The cleaned surfaces were free of oxides, as deduced from STM images (please see Fig. S1 in Supporting Information) and supported by a clear (4×2) LEED (Fig. S2) as well as by an absence of O 1s intensity in XPS (not shown). Thermal oxidations were carried out in the same UHV chamber by leaking O_2 gas (6.0 purity) into the chamber via a leak valve. The following oxidation-parameter combinations were used: T = 380 ºC; p = 3-4×10^{-6} mbar; t = 10 min, and T = 360 ºC; p = 7-8×10^{-6} mbar; t = 15 min for the crystalline *c*(4×2)-O and (3×1)-O surfaces, respectively. These surfaces were also characterized *in situ* with XPS, LEED, and STM. The samples were then transferred into an ALD-chamber (via a vacuum transfer line, 3×10^{-6} mbar) immediately to grow a 12 nm Al_2O_3 film. In addition, one reference sample with InAs native oxides was characterized in UHV environment and

transferred to the ALD chamber for similar ALD growth. The base pressure of the ALD chamber was below 1.5×10^{-1} mbar. TMA (Sigma-Aldrich: code 663301-25G) and deionized H_2O precursors were kept at room temperature, and the working pressure of the reactor during the precursor pulses (1 s) was 6.0×10^{-1} mbar. N_2 (5.0 purity) gas was used as a purging agent (10 s purges). Several groups report optimal Al_2O_3 film growths close to 300 ºC, when best stoichiometry and minimal impurity films are required.[52-54] However, the optimized growth in our home-made ALD system, according to material purity and stoichiometry characterizations, is reached at 180 (±20) ºC. A similar temperature of 200 (±20) ºC was reported to be used in Ref. (55). In fact, very low-temperature ALD growth (e.g., 120º C) has been reported to decrease border trap density.[22] An important circumstance to notice is that we started the ALD-Al_2O_3 growth with a H_2O pulse instead of a TMA pulse, in an attempt to minimize TMA reacting directly with the prepared crystalline oxide surfaces. A film thickness of 12-13 nm with a refractive index of 1.4-1.5 was determined through ellipsometry. This thickness was chosen on the basis HAXPES setup (described below) in order to change the probing thickness in the InAs side as much as possible, allowing also only the InAs interface part.

Separate Al_2O_3/InAs(100)(3×1)-O samples were grown for time of flight elastic recoil detection analysis (ToF-ERDA) characterization at the University of Jyväskylä (Finland). The ALD-Al_2O_3 films were grown thicker (30 nm) to quantify the elemental composition in the bulk film more reliably. ToF-ERDA is a method in which the sample is bombarded with high energy ions and in the consequent elastic processes individual sample atoms are recoiled towards the detector. Both time-of-flight and energy are measured for each recoiling atom (ion) and thus the mass and the original depth of the sample atom can be calculated. With ToF-ERDA all sample elements, including hydrogen, can be quantified with no reference samples needed. ToF-ERDA excels when measuring light elements (such as H,

C, N, O) in heavy substrates, but has no difficulties when quantifying heavy element films on light substrates either.[56] Elemental composition of the ALD-Al_2O_3 thin films were measured by 6.8 MeV $^{35}Cl^{3+}$ ion beam with 7 degree tilt from the beam direction.[57] Analysis was done using Potku ToF-ERDA analysis software.[58]

For the 12 nm Al_2O_3/InAs(100) structures, HAXPES measurements were carried out at HIKE endstation[44] located at BESSY II KMC-1 beamline at Helmholtz-Zentrum Berlin.[59] Samples were transferred via air and measured *ex situ* with photon energies 2020 eV, 4020 eV, 4520 eV, and 6060 eV in case of the Al 2p, As 3d, and In 4d energy regions. For the measurement of the In 3d and O 1s energy regions, photon energies of 2444 eV, 4444 eV, 4944 eV, and 7332 eV were used to attain approximately the same inelastic mean free path (IMFP) values for the photoelectrons of all core levels. IMFP varied approximately from 4 nm to 8 nm for the used photon energy range. The pass energy of the electron analyzer was 200 eV for all core-levels. The instrumental energy resolution was better than 0.35 eV. Binding energy (BE) calibration for each photoelectron spectrum was done by measuring the Au 4f energy region of a clean gold foil in electrical contact with the samples, and setting the BE of the Au $4f_{7/2}$ peak to 84.0 eV. Curve fit analysis of the measured spectra was performed using Origin software with a separate peak-fitting module. After Shirley-background removal, Voigt-function peaks were used with fixed Lorentzian line width but varying Gaussian line width to account for changes in experimental resolution. The presented fittings were justified in the following way: A minimum number of peaks that satisfy the physical restrictions (set by the samples material and measurement set-up) was introduced in the deconvolution. These restrictions include core-hole lifetime of different species (Lorentzian width), sample homogeneity and temperature, x-ray resolution, and total analyzer resolution with the chosen parameters (Gaussian width). The photoelectron signal originating from the InAs substrate (bulk) separates from the interface induced emission peaks by so-called core-

level shifts (CLS) in the electron binding energy. Hence, CLS reflect the change of the electrostatic potential due to charge redistribution (both electrons and ions) at the well-buried interface layers compared to the charge environment present in the bulk. Several different peak combinations were modeled, and the most reasonable fit is shown in the results.

In purpose to implement the family of crystalline oxidized III-V semiconductor surfaces to applications, separate high electron-mobility transistor (HEMT) structures were grown by molecular beam epitaxy (MBE) with a protective 50 nm As cap. The following heterostructure was grown by MBE on GaAs(100) from bottom to top: n-type $Al_{0.2}Ga_{0.8}As$ spacer (10 nm, 1.5×10^{18} cm^{-3}), undoped $Al_{0.2}Ga_{0.8}As$ spacer (2 nm), $In_{0.15}Ga_{0.85}As$ channel (14 nm), undoped $In_{0.49}Ga_{0.51}P$ (2 nm) + delta doping (2.5×10^{12} cm^{-2}), n-type $In_{0.49}Ga_{0.51}P$ (14 nm, 1.5×10^{17} cm^{-3}), and n-type GaAs (5 nm, 5×10^{18} cm^{-3}). The amorphous As cap was removed in UHV by annealing the samples at 400 ºC for 15 min, to produce As-rich GaAs(100) with the (2×4) reconstruction verified by LEED. This was followed by *in situ* In deposition, crystalline oxidation,[27,34] and ALD-Al_2O_3 growth (7 nm) starting with a H_2O pulse. The sample pieces were then processed into HEMT components by standard optical lithography procedure. Al_2O_3 film was wet etched with ammonium hydroxide based etchant (NH_4OH:H_2O, 1:10, 10 min) to form 0.1 × 0.2 mm^2 mesa areas. Then mesa isolation was done by dry etching with an inductively coupled plasma reactive ion etching system using Cl_2/N_2 plasma. A 100 nm SiO_2 insulating layer was deposited on the mesa sidewalls by plasma enhanced chemical vapor deposition at 150 ºC and removed from the mesa surface with a lift-off procedure. Source and drain openings to Al_2O_3 layer were then wet etched (NH_4OH:H_2O, 1:10, 10 min) on top of the mesa. Then, 1 μm wide trenches were etched with phosphorous acid / hydrogen peroxide based etchant (H_3PO_4:H_2O_2:H_2O, 1:1:10, 30 s) throughout the topmost GaAs layer parallel to the gate to avoid charge carrier transfer within this layer. Source and drain Ni/Au/Ge/Au (5/5/30/90 nm) metal stacks were deposited by e-

beam and using a lift-off process, following contact rapid thermal annealing at 370 ºC for 60 s. Finally, 4 μm wide gate Ti/Pt/Au (50/50/100 nm) e-beam metallization was carried out also by a lift-off process.

RESULTS AND DISCUSSION

HAXPES analysis of the differently prepared Al_2O_3/InAs(100) junctions reveal many interesting features. First, the binding energy (BE) of the component associated with the bulk InAs crystal was determined from the As 3d spectra measured with the highest x-ray photon energy (6060 eV). The As $3d_{5/2}$ bulk peak is located at BE of 41 eV in all the samples and labeled B in Fig. 1. Careful determination of the bulk BE value serves as an exact reference for analyzing the interface-related components (or core-level shifts). Among the used photon energies, 6060 eV photons give the largest IMFP value of about 8 nm for the As 3d photoelectrons, and hence the signal from the substrate can be detected well. BE values between 40.6-41.0 eV are reported for As $3d_{5/2}$ bulk InAs in literature.[47-51,56] The same reasoning was used for all core-levels to determine the bulk peak positions (6060 eV photons for Al 2p, As 3d, In 4d; 7332 eV photons for In 3d, O 1s). Concerning the photoelectron spectra recorded with more interface sensitive photon energies (2020-4555 eV), the bulk peak for the As $3d_{5/2}$ doublet is located between 40.98-41.05 eV in every As 3d spectrum in this work.

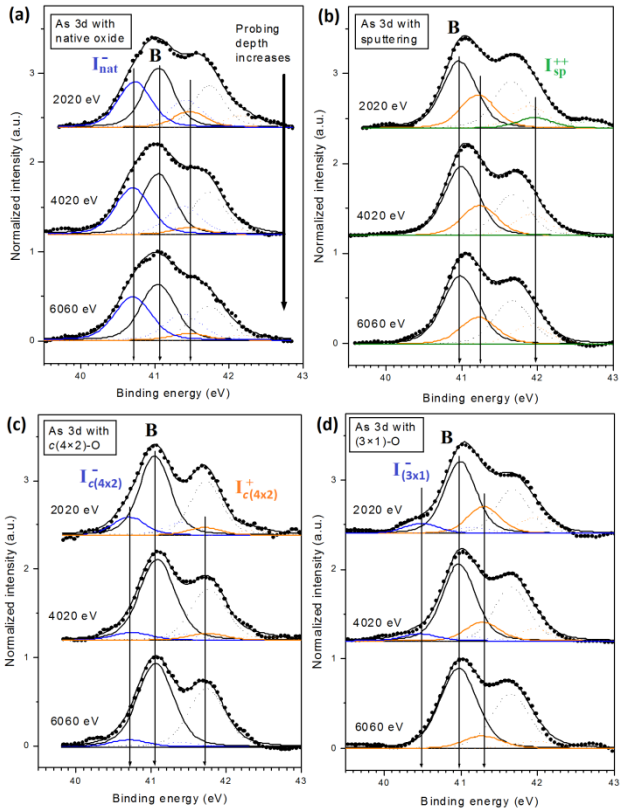

Figure 1. *As 3d core-level spectra from (a) native oxide Al_2O_3/InAs(100), (b) sputter-cleaned Al_2O_3/InAs(100), (c) pre-oxidized crystalline Al_2O_3/InAs(100)c(4×2)-O, and (d) pre-oxidized crystalline Al_2O_3/InAs(100)(3×1)-O interfaces. Negative CLS (Γ) and bulk signal (B) are marked in blue and black, respectively, together with their spin-orbit-splitting (SOS) pairs (dotted lines). Positive CLS (I^+ and I^{++}) are marked in orange and green together with their SOS pairs (dotted lines).*

In general, the As 3d spectra measured from the different Al_2O_3/InAs(100) interfaces (Fig. 1) are narrow (total width of main As 3d features less than 3 eV), as compared to the corresponding synchrotron based PES spectra we measured earlier from the crystalline oxidized surfaces without the Al_2O_3 dielectric layer (total width of main As 3d

features about 5 eV).[34,42] There are several possible reasons for this. Obviously, the vacuum-solid interface effects such as dangling bonds and surface re-bonded configurations are missing (or significantly decreased) at the solid-solid interface of Al_2O_3/InAs(100). Second, a significant potential change, appearing at the vacuum-crystal interface, is clearly decreased at the well-embedded Al_2O_3/InAs. Third, ALD precursors (e.g., TMA) are known to provoke a self-cleaning effect that removes at least some oxides from III-V surfaces during the starting cycles of ALD growth. Indeed, an absence of contributions from high oxidation states of As (e.g., As_2O_3 or As_2O_5, which are known to cause clearly separated emission components with at least +3.0 eV shift compared to the bulk component), can be readily explained with the ALD self-cleaning.[2] Earlier results[41] clearly support this explanation because As_2O_3 tends to be unstable against ALD-Al_2O_3 on InAs. Controversial results also exist that As_2O_3 is not removed from the InAs native oxide surface by TMA until the resulting Al_2O_3/InAs stack is heated up to 600 ºC.[47] This difference can be explained by a very thin Al_2O_3 film (1 nm) that allows oxygen diffusion from the surface toward the interface (or/and vice versa As diffusion toward the surface), and hence, interface re-oxidation after the ALD growth. Furthermore, while five deposition cycles of HfO_2 at 100 ºC still preserved As_2O_3 at the HfO_2/InAs(100)(3×1)-O interface, the ALD growth of 5 cycles at 150 ºC already removed most of the highly oxidized As bonds due to the clean-up effect.[60] Because the ALD growth temperature in our experiments was even higher (180 ºC) and because the Al-containing precursor can be expected to be more reactive than the Hf-containing one, the self-cleaning of As-oxides from all the different samples is the most likely reason for the absence (or significant decrease) of +3.0 eV As 3d shifts in our experiments (Fig. S3), despite that ALD was started here with the H_2O pulse. The presence of As_2O_3 in the form of nanowires on top of InAs(100)(3×1)-O (Fig. S1), as well as their removal during the ALD, is consistent with the self-cleaning concept and with energetically favored Al-O bond formation over As-O. It

was earlier noticed that substrate oxidation temperatures lower than 270 ºC resulted in an absence of As_2O_3 at InAs(100)(3×1)-O surface.[60] These temperatures are probably too low for oxidation-induced nanowire formation via As diffusion toward the topmost surface. Interestingly, temperatures over 330 ºC were reported to cause As_2O_3 immediate decomposition.[60] In our studies, however, As_2O_3 is present at the InAs(100)-(3×1)-O surface even if the pre-oxidation temperature is 400 ºC. A reasonable explanation for this apparent contradiction is that the decomposition of As_2O_3 happens only if the post-annealing treatment of pre-oxidized surfaces is used as in Ref. (60).

Furthermore, clear differences can be resolved in the spectra of the differently treated samples. The native-oxide Al_2O_3/InAs(100) interface contains an As environment reflected by signal at a lower BE value compared to the bulk value, i.e., a negative shift of -0.34 eV, which is labeled as I^{-}_{nat} in Fig. 1(a). The intensity of this component is clearly less sensitive to the photon energy than the negative shifts of the *c*(4×2)-O and (3×1)-O interfaces, although the *c*(4×2)-O interface has a nearly similar As 3d CLS value of -0.35 eV ($I^{-}_{c(4\times2)}$ in Fig. 1(c)). This implies that the bonding environment of I^{-}_{nat} is dispersed for several atomic layers and thus for a thicker interface layer than the interface related bonding environments in the other samples. According to the results, the native oxide interface is therefore thicker compared to the sputtered and crystalline oxide interfaces. This observation is reasonable, because the native oxide layer can be expected to be thicker than the pre-oxidized layers, and the ALD cleaning effect cannot remove the whole native oxide.

The sputtered InAs reference interface includes +1.0 eV shift (I^{++}_{sp} in Fig. 1(b)), which is commonly associated with As antisite (As-As-As) or low oxidation state of As.[41,50] This +1.0 eV component has the largest intensity in the spectrum with the largest interface sensitivity, indicating that it derives from the interface layers. BE shift of nearly +1 eV has also been associated with As-As dimers, for example at Al_2O_3/GaAs interfaces.[53] A clear

positive BE shift is observed in the As 3d spectrum of the *c*(4×2)-O interface as well: +0.77 eV shift labelled as $I^{+}_{c(4\times2)}$ in Fig. 1(c). A possibility of As-Al bonding present at Al_2O_3/InAs interfaces has been pointed out in earlier studies.[50,52] In this study, the positive BE shifts of about +0.4 eV seen in Fig. 1 can be an indication of an As-Al chemical environment, while the +0.77 eV shift is considered here as the sign of crystalline oxidation.

In contrast, a large negative As 3d BE shift of -0.51 eV is resolved at the (3×1)-O interface ($I^{-}_{(3\times1)}$ in Fig. 1(d)), which we here present to be a fingerprint feature of the (3×1)-O interface. In many cases, negative As shifts are associated with local defects, in particular, broken As bonds (i.e., dangling bonds). However, the (3×1)-O interface layer has been found to decrease the amount of interface defect states,[30,36,60] also when ALD-Al_2O_3 is used.[27,38] Therefore, we provide here an alternative explanation for the negative shift: Instead of on-site electron transfer or redistribution around the corresponding interface As atoms, the negative shift might originate from an increased negative Coulombic potential induced by a crystal neighborhood including, in particular, very electronegative O atoms. Indeed, such a long-range Coulombic effect (Madelung potential) has been found to play a key role in many semiconductor surfaces.[61]

Similarly to the As 3d spectra, the In 4d spectra (Fig. 2) are also narrow, but the different interface environments can be still resolved between the four samples. The In 4d contribution derived from the bulk was determined carefully from the In 4d photoelectron spectra measured with the highest x-ray photon energy (6060 eV). The bulk-reference peak is found at BE of 17.5 eV in all the samples (labelled with B in Fig. 2). This result serves again as a good reference for InAs oxidation PES studies. The BE value of 17.5 eV is also reported for In 4d of bulk InAs in literature.[47,48]

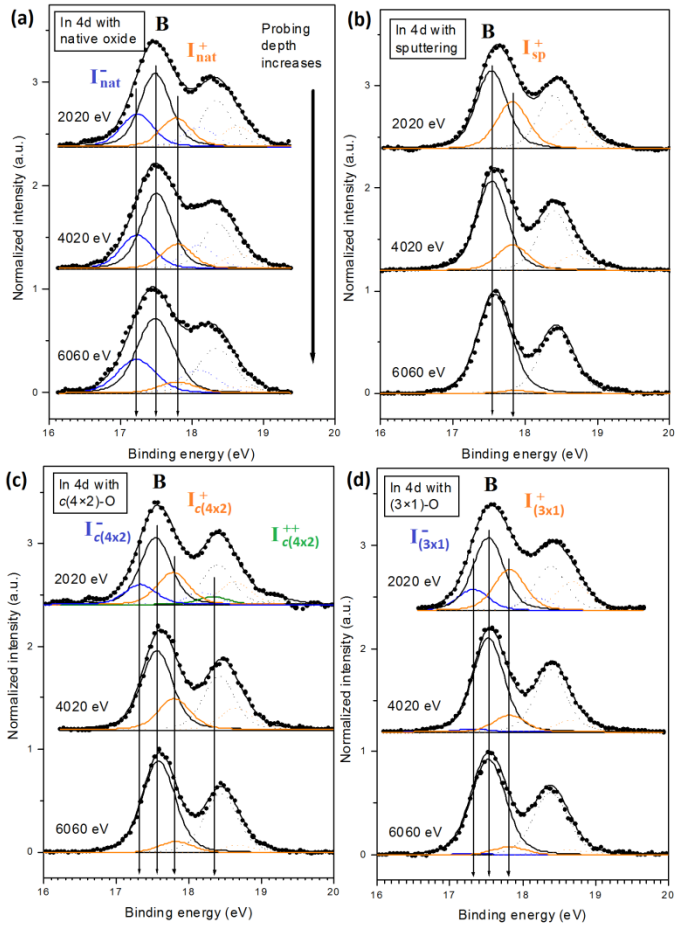

Figure 2. *In 4d core-level spectra from (a) native oxide Al_2O_3/InAs(100), (b) sputter-cleaned Al_2O_3/InAs(100), (c) pre-oxidized crystalline Al_2O_3/InAs(100)c(4×2)-O, and (d) pre-oxidized crystalline Al_2O_3/InAs(100)(3×1)-O interfaces. Negative CLS (I) and bulk signal (B) are marked in blue and black, respectively, together with their SOS pairs (dotted lines). Positive CLS (I^{+} and I^{++}) are marked in orange and green, respectively, together with their SOS pairs (dotted lines).*

There are several previous findings indicating that the low oxidation state of indium (In_2O) is an important building block of the crystalline oxides.[27,36,38,41,60] It can form beneath the topmost InAs atomic layer as small oxygen atoms diffuse towards the bulk and

release As atoms. Released As atoms, in turn, diffuse towards the surface. This phenomenon is energetically much more favorable than, for example, As-O bonding or strain inducing short O-O dimer bonds on the surface.[34,40] In_2O has been usually shown to cause +0.5 eV shift at the vacuum-InAs(100) surfaces, but in Fig. 2 it can be seen that the Al_2O_3/crystalline oxide interfaces do not exactly exhibit this fingerprint +0.5 eV component. However, in the present measurements the oxidized InAs interfaces lie clearly below the topmost Al_2O_3 (12 nm) film, deep inside a solid, which can cause variation in the potential as discussed above. Indeed, +0.25 eV and +0.29 eV shifts are seen at the Al_2O_3/InAs(100)*c*(4×2)-O and -(3×1)-O interfaces ($I^{+}_{c(4\times2)}$ in Fig. 2(c) and $I^{+}_{(3\times1)}$ in Fig. 2(d), respectively). These signals can be associated with In_2O-type environment. For the Al_2O_3/InAs(100)*c*(4×2)-O interface, also a second positive component +0.80 eV is observed: $I^{++}_{c(4\times2)}$ in Fig. 2(c). These two positive BE shifts in the In 4d spectra of the InAs(100)*c*(4×2)-O interface indicate two clearly different oxidation-induced environments for In atoms: +0.80 and +0.25 eV which might be traditionally associated with In_2O_3-type and In_2O-type bonding environments, respectively.[38,42]

Next, we discuss an important question regarding the crystalline oxidized structures: whether a negative In 4d shift is also an inherent property of the controlled oxidized InAs layer, or whether it just arises from local defects. The pure InAs(100)(3×1)-O surface has been observed to have two bonding environments with negative shifts: -0.47 eV and -0.23 eV.[42] The former environment was attributed to filled In dangling bonds, which were also observed at the crystalline oxidized InSb.[18] Such In dangling bonds can be expected to disappear (or significantly decrease) at the Al_2O_3/InAs(100)(3×1)-O interface. However, these negative shifts can originate also from the sputter cleaning that leaves InAs surface In rich (even In clusters), and hence the negative In 4d shift can be due to metallic In-In-In type environment as suggested previously.[60] In this study, the negative CLS are present

only at the interfaces that were oxidized before the ALD grown Al_2O_3 layer (I^-_{nat}, $I^-_{c(4\times2)}$, and $I^-_{(3\times1)}$ in Fig. 2(a), 2(c), and 2(d)). The sputtered interface shows in fact the most narrow In 4d photoelectron spectra and only +0.29 eV CLS (I^+_{sp} in Fig. 2(b)). Furthermore, STM characterization does not reveal any significant In clustering (Fig. S1) on the clean or crystalline oxidized surfaces before the ALD-Al_2O_3 growth. If all the different chemical enviroments observed at the studied Al_2O_3/InAs(100) interfaces are taken into account, our results indicate that the oxidized crystalline InAs interface layers own inherent negative BE shifts, as compared to the InAs bulk crystal. This can be associated with the Coulombic potential change induced by oxygen ions in the crystal neighborhood. In other words, the Madelung potential induced by other crystal ions also affects the BE shifts, in addition to changes in the valence-electron distribution around the atomic site considered (so called on-site charge). This is an interesting finding because only positive BE shifts are usually found for oxidized III-V interfaces, and because the crystalline oxidized interfaces with the negative BE shifts tend to decrease the defect densities. A negative CLS is seen here also for the native oxide interface, but this I^-_{nat} component behaves clearly differently from $I^-_{c(4\times2)}$ and $I^-_{(3\times1)}$, similarly to the case of I^-_{nat} detected in the As 3d spectra: The native oxide interface is thicker than the crystalline oxidized interfaces. $I^-_{c(4\times2)}$ is similar at the Al_2O_3/InAs(100) interface compared to the negative shift seen earlier at the InAs(100)*c*(4×2)-O surface (-0.22 eV).[38]

To confirm that the above results do not originate from interface effects caused by defects in the Al_2O_3 films and by different internal band bending, we have studied the junctions by ToF-ERDA method (Fig. 3) and by valence-band HAXPES measurements (Fig. S4). First of all, very similar valence-band offsets, approximately 4.5 eV, are found for all the junctions without any significant variation in the internal electric field at the interfaces. Furthermore, ToF-ERDA data in Fig. 3 show that the ALD grown Al_2O_3 films are homogenous and contain low concentration of impurities. It is worth noting that although the

ToF-ERDA data suggest minimal contributions from extrinsic point defects (impurities), it does not however exclude intrinsic point defects (e.g., vacancies). Typical observed elemental concentrations for the Al_2O_3 films are (59.0 ± 2.5) at-% of O, (40.4 ± 2.5) at-% of Al, (0.6 ± 0.2) at-% of H and (< 0.06) at-% of C. Long tails in Fig. 3 histogram in the right and in the graph on the left are caused by multiple scattering (i.e., not by impurites in the InAs substrate or in the Al_2O_3 film). Furthermore, measured HAXPES spectra of the Al 1s and O 1s energy regions unveil almost identical Al_2O_3 properties for the four samples. The peaks of the Al 1s and O 1s spectra are located at BE values of 1563.0 (±0.1) eV and 532.9 (±0.1) eV, respectively, in all samples measured by using the different photon energies ranging from 2444 eV to 7332 eV (fits are not shown). No signal is found at BE of 1559 eV in any of the Al 1s spectra, indicating an absence of metallic Al in the samples.[62,63]

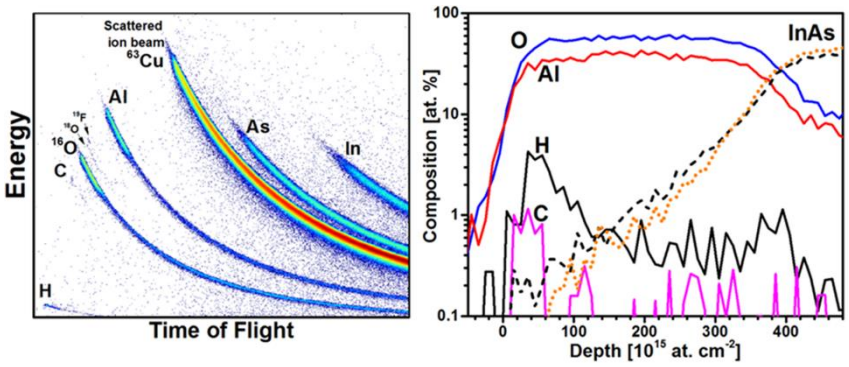

Figure 3. *ToF-ERDA results of the Al_2O_3 film quality grown by the self-built ALD. Films are homogenous and contain only low concentration of impurities. Typical observed elemental concentrations are on average: (59.0 ± 2.5) at-% of oxygen, (40.5 ± 2.5) at-% of aluminum, (0.6 ± 0.2) at-% of hydrogen and (< 0.06) at-% of carbon. The elemental concentrations are taken at the center part of the film.*

Next we have investigated how the controlled InAs oxidation procedure might be transferred to current applications. The previous InAs capacitor and metal-oxide-semiconductor field-effect transistor (MOSFET) tests for the crystalline oxidized layers have been indeed promising.[36,37,60] Thus a question is, in which way the controlled InAs oxidation can be used to develop the current devices based on various III-V semiconductors. The HEMT components, used increasingly in wireless communication systems, form one potential application area because in these devices, the gate insulator/III-V interface has a significant effect on the device performance.[64-69] For such tests, we have grown pseudomorphic GaInAs-channel HEMT structures with a GaInP barrier and a GaAs cap. (EXPERIMENTAL SECTION and Fig. (4a)). The reference devices were here standard recess-gate type components. The processed HEMT components were compared within their gate-modulation strengths and gate leakage currents. As can be seen in Fig. 4(b), use of the controlled InAs oxidation procedure decreases the leakage current without losing the gate controllability. The gate leakage current decreases by a factor of three on average, as compared to the reference components. Here it is also essential that the leakage-current measurements through the Al_2O_3/InAs(100) junctions, characterized above by HAXPES, show that the crystalline pre-oxidation decreases the leakage, as compared to the clean sputtered sample and the native oxide sample (Fig. S5). This result is also consistent with the previously found benefits for MOS capacitors and transistors.[30,36,37,60]

The current-voltage curves in Figs. 4(c) and 4(d) show that the channel can be properly closed by negative voltages (i.e., depletion-mode HEMT). Interestingly, it might be expected that the gate modulation strength (or controllability) would be higher for the reference device because its gate electrode lies closer to the channel after the recess etching.[64,67] However, the modulation strength of the controlled oxidized components is even a bit stronger (1.4 times on average) than that of the reference components, which indicates

that the electronic bands can be readily moved by the gate voltage for the oxidized sample (without significant Fermi-level pinning). These results are consistent with previous HEMT characterizations after liquid phase oxidation treatments of the gate.[68] Radio frequency measurements of HEMT are needed in future to clarify effects of the controlled gate oxidation on the gain and noise properties. Before that contact resistances of our devices need to be improved; low channel currents here are most likely due to non-optimized contact resistances in the first device trials. Anyhow, the presented HEMT results are expected to pave the way for utilizing the controlled oxidation of the gate area in the HEMT development because the enhanced gate controllability and decreased gate leakage are promising results. Finally, we still discuss how the crystalline InAs oxidation can be in future combined with a chemical etching procedure which is the common pretreatment of HEMT gate areas without use of the As capping step. Namely, a HCl-based gate etching provides an As-rich (or group-V rich) III-V surface,[70] which can be then crystallized by vacuum heating to an As-stabilized (2×4) starting surface for the controlled InAs oxidations described above.

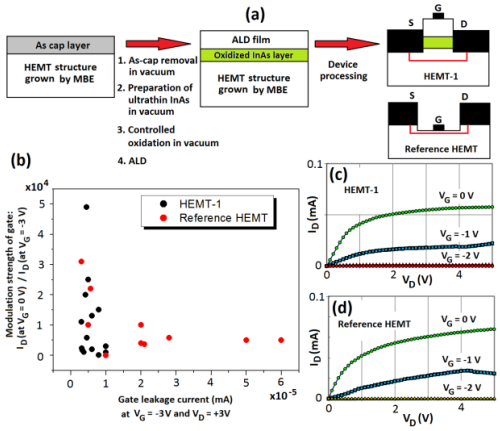

Figure 4. *(a) Schematic process flow to incorporate a thin InAs layer and its controlled oxidation for a HEMT device process. (b) Comparison of gate leakage current and gate modulation strength between HEMT-1 including the crystalline oxidation of InAs and reference HEMT; different dots mean different components measured. (c) and (d) Examples for gate-voltage (V_G) controllability of the current (I_D) between drain and source.*

CONCLUSIONS

Here we report the comparison of high-resolution photoelectron-spectroscopy results for the different Al_2O_3/InAs interfaces lying well below the topmost surface parts, in order to minimize the various possible vacuum-surface effects on the spectra. It is found that the pre-oxidized crystalline InAs interface layers exhibit clear negative BE shifts as compared to the InAs bulk crystal, which can be preliminarily associated with the Coulombic potential changes induced by oxygen ions. Thus, the presence of negative core-level shifts is not necessarily an indication of harmful point defects, but surprisingly can be a sign of oxidation of III-V. In contrast, our results suggest that knowledge of the atomic structure behind the +1 eV As 3d shift (rather than As_2O_3 type +3 eV shift) is the key to understand defect-level formation at the InAs interfaces. Concerning future research of atomic-structure models via theoretical calculations for the crystalline oxidized Al_2O_3/InAs interfaces, it has been found here that In 3d shift of +0.29 eV and As 3d shift of -0.51 eV provide a benchmark for the (3×1)-O interface model. The corresponding specific shifts for the *c*(4×2)-O interface structure are +0.77 eV for As 3d and 0.80 eV for In 3d. Finally, we have demonstrated a potential route to develop the gate part of widely used III-V HEMT components with the controlled InAs oxidation.

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ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website.

STM images and LEED patterns for the different InAs surfaces before ALD growth. Large-scale As3d spectrum from the (3×1)-O interface. HAXPES spectra of the valence band energy region for the interfaces. Leakage current curves for the different InAs interfaces.

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