A Detailed Examination of Polysilicon Resistivity Incorporating the Grain Size Distribution

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***Abstract*—Current transport in polysilicon is a complicated process with many factors to consider. The inhomogeneous nature of polysilicon with its differently shaped and sized grains is one such consideration. We have developed a method that enhances existing resistivity models with a 2-D extension that incorporates the grain size distribution using a Voronoi-based resistor network. We obtain grain size distributions both from our growth simulations (700, 800, and 900 K) and experimental analysis. Applying our method, we investigate the effect that variation in grain size produces with cases of different average grain sizes (2 nm–3 μm). For example, the resistivity of polysilicon with an average grain size of 175 nm drops from 11 to 4.5 kΩ·cm when compared with conventional 1-D modeling. Our study highlights the strong effect of grain size variation on resistivity, revealing that wider distributions result in significant resistivity reductions of up to more than 50%. Due to larger grains present with a grain size distribution, current transport encounters fewer grain boundaries while the average grain size remains the same resulting in fewer barriers along the current transport path. Incorporating the grain structure into the resistivity modeling facilitates a more detailed and comprehensive characterization of the electrical properties of polysilicon.**

***Index Terms*—Polysilicon, resistivity modeling, resistor network, simulation, SPICE.**

I. Introduction

POLYSILICON is used to mitigate the harmful parasitic surface conductivity (PSC) in microelectronics radio frequency applications [1]. PSC drops the resistivity from the kΩ range to Ω range in the high-resistivity silicon (HR-Si) substrate near oxide interfaces. Polysilicon film is used between the oxide and the HR-Si to raise the resistivity back to the kΩ range.

However, there is a lack of proper methods to estimate the effect of grain size distribution on the resistivity of polysilicon. The present study deals with extending the existing resistivity works to include the effect of grain size distribution to the resistivity of polysilicon. We continue along the research line started by Seto [2] and developed further by many other researchers [3], [4], [5], [6], [7]. The discontinuities found in polysilicon, in the form of grain boundaries, complicate modeling the current transport process compared with crystalline silicon. The discontinuities result in trapping states and segregation sites [8] at the grain boundaries which can trap charge carriers and neutralize dopant atoms. They in turn form a potential barrier that impedes carrier transport from one grain to the next. While lot of the effort has focused on polysilicon, similar mechanisms are present with other polycrystalline semiconductors [9]. The presented method could therefore be extended for them as well.

The connection between the resistivity modeling and the experiments has received much attention through four-point, Van der Pauw and Hall effect measurements with which the effect of temperature, doping concentration, dopant activation, mobility, etc. on resistivity is compared [2], [3], [6], [10]. It should be therefore noted that the focus of this work is to extend the existing works to incorporate the effects that arise due to the inhomogeneous nature of polysilicon and is predominantly a computational/modeling work.

This article is organized in the following way: first, in Section II, we investigate how the grain structures found in our molecular dynamics simulations of polysilicon growth affect the resistivity. We introduce a simple, averaged grain size and boundary thickness estimation with which we estimate the effect of growth temperature on resistivity. We then obtain the grain size distribution from the simulations. Our experimental analysis of polysilicon also provides us with a grain size distribution. The experimental side of the work is the focus of Section III. To investigate the effect of grain size distribution on resistivity, we have developed a method that extends the existing polysilicon resistivity models. Although the technique is generally valid, we demonstrate its operation to investigate and eliminate PSC. Details of the method are outlined in Section IV. Section V briefly examines a simpler,

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alternative approach for investigating the effect of grain size distribution on resistivity. In Section VI, we present our investigations on the effect of grain size distribution on resistivity when compared with 1-D, average grain-sized models.

II. Impact of Simulated Grain Structures on Resistivity

We have investigated the growth process of polycrystalline silicon films [11], [12] using LAMMPS molecular dynamics simulations [13] to advance the understanding of the effects of growth and its parameters on their electrical properties. Our simulations investigate the very start of the growth (first 10–20 nm) where the initial nucleation and grain structure formation takes place. As such, it should be noted that the grain sizes found in our simulations are significantly smaller than those found in our experimental investigations. We, however, consider the charge carrier trapping properties of the grain boundaries and the effect of it on the resistivity to be similar regardless of the grain size. Since resistivity in polysilicon is largely a grain boundary-limited process [2], [3], [4], the method we present in Section IV has applicability both with our small grain size simulations and the larger grain sizes found at the top of the polysilicon growth. Another caveat worth noting is that because we are simulating a physical growth process with an interatomic potential, the parameters of growth, such as the temperature, are not directly comparable with the parameters found in the typical chemical vapor deposition process.

Relevant measures obtained from the simulations are the grain size and grain boundary width. Other variables needed to model polysilicon resistivity, such as dopant concentration and trapping state density, do not play a direct part in the simulation of polysilicon deposition. At this stage, they are free variables whose influence is investigated.

For the resistivity calculations in this section, we use the model by Mandurah et al. [4]. Following the idea found in the so-called brick layer models [14], we create a block model and use it to investigate the effect of different growth parameters on the grain structure and thus on the resistivity. The block model consists of a cubic grain (grain size of W_g and resistivity ρ_g) and grain boundary pieces surrounding the grains (width of W_{gb} and resistivity of ρ_{gb}).

Visualization and analysis of the simulations are done in Ovito [15]. The structural classification algorithm polyhedral template matching [16] provides us with the identification between grain atoms and grain boundary atoms. Based on the local atomic neighborhood, it can recognize various ordered structures, such as the diamond structure relevant here for silicon. The proportions of atoms in the crystal structure (grain atoms) and the disordered structure (grain boundary atoms) are obtained. With the percentage of atoms in the grain, the percentage of atoms in the boundaries, and the total volume of the analyzed polylayer, we can find W_g and W_{gb} that satisfy the atom shares found in the simulations.

The simulations were done at three different temperatures: 700, 800, and 900 K. By analyzing these, we can establish a connection between the growth temperature and grain size, grain boundary width, and resistivity. The effect of growth temperature on grain boundary width, grain size, and the resulting resistivity is shown in Fig. 1. Lower temperatures produce thicker grain boundaries and smaller grains. With more grain boundary area, the more highly resistive nature of the grain boundary results in higher overall resistivities. The effect is particularly prominent here since the average grain size is very small (on the same size scale as boundary width).

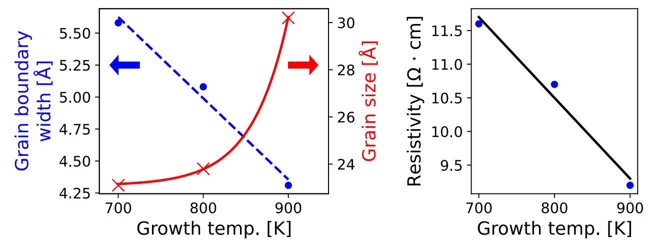

Fig. 1. Effect of growth temperature on grain structure and resistivity. Resistivities are calculated based on the Mandurah model with grain sizes and boundary widths from the simulation (for p-type doping $5 \cdot 10^{18}$ cm^{-3}). The left figure shows the grain boundary width (blue, dashed) and grain size (red, solid) as a function of temperature. Right shows the effect on resistivity.

In addition to grain size and boundary width analysis, we can also estimate the grain sizes using Ovito. We can then use these to examine the resistivity in a more detailed manner using the approach outlined in Section IV. The results for these can be found in Table II.

III. Experimental Investigations

Our sample is a p-type (boron) ⟨100⟩ substrate grown with the Czochralski method with a poly-Si layer of a thickness of 3 μm.

Scanning electron microscopy (SEM) imaging of poly-Si samples was performed using a Thermo Scientific Apreo S Field-Emission Scanning Electron Microscope. The secondary (SE) and backscattered (BSE) electron images were observed in high vacuum using Everhart–Thornley and in-lens/in-column Trinity detectors. No coating of the samples was done prior to the imaging.

The sample surface was polished; therefore, it was not possible to detect the grains or grain boundaries using SEM. To make the grains and grain boundaries visible, the samples were prepared prior to SEM measurements by immersion into a solution of hydrofluoric acid, acetic acid, and nitric acid (3:1:2), which works based on oxidation and dissolution [17]. After immersing the sample into the above-mentioned solution for 10 s followed by DI water rinsing, the grains and boundaries were observed using SEM. Fig. 2(a) (left) shows the SEM image of the surface.

Image analysis was performed using Fiji ImageJ [18]. The mask for the segmentation was done manually. Then with binary segmentation, we analyze grain size distribution. The segmentation is shown in Fig. 2(b) (left) and the resulting grain size distribution is shown on the right.

A polysilicon sample was also measured with SEM after slicing. One of the images is shown in Fig. 2(a) (right). Since the columnar structure is predominant up to a few hundred nanometers below the surface, a good estimate of the grain size and shape distribution at the topmost part of the sample can

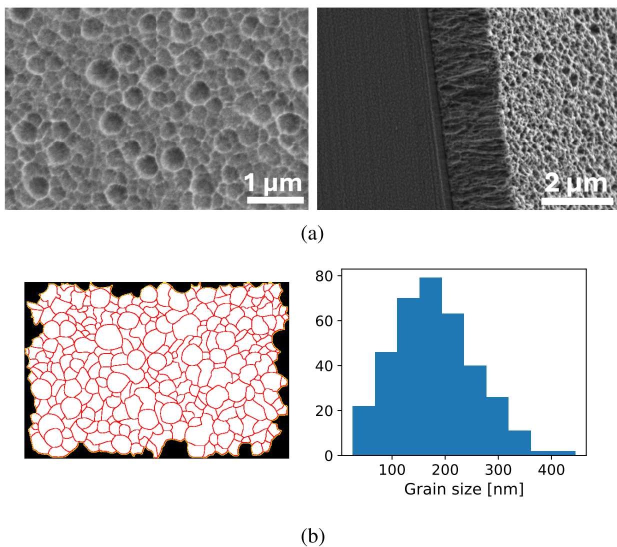

Fig. 2. SEM image analysis of the polysilicon sample provides us with a grain size distribution that can be used in our resistivity calculations. (a) SEM image of the polysilicon sample surface (left) and the sliced side showing the columnar polysilicon and the single-crystalline silicon below it (right). (b) Image segmentation, which is used to analyze grain size distribution of the sample.

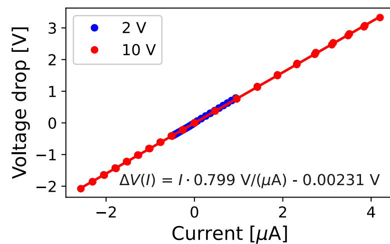

Fig. 3. Voltage drop as a function of current measured from our polysilicon sample using the four-point probe method. Blue points are measured with voltage range from −2 to 2 V, while red points with from −10 to 10 V. From the slope we can ultimately calculate the resistivity given the thickness of our sample.

be obtained from its surface image. This work aims to include the effect of the grain size distribution on surface resistivity, so in this context, it is sufficient to consider the resistivity parallel to the surface.

The resistivity of the polysilicon sample was measured with the four-point probe method [19]. To ensure a good contact, a set of round gold pads with even spacing were sputtered to the surface. The four-point measurement result is shown in Fig. 3. Without any surface treatment, the resistivity of the sample was 11 kΩ·cm (with values in the range 2.2–15 kΩ·cm). After this, the sample was annealed in an ultrahigh vacuum chamber (base pressure below 10^{-9} mbar) in oxygen ambient (pressure $7.5 \cdot 10^{-6}$–$1 \cdot 10^{-5}$ mbar) for 1 h at 370 °C. To ensure that we were not measuring a modified resistivity due to intermixing of gold and silicon, but an actual resistivity from possibly modified polysilicon itself, another set of gold pads were deposited. The resulting resistivity was $3.5\ \text{k}\Omega \cdot \text{cm}$.

IV. Voronoi-SPICE Method

The method outlined in Section II relies on the idea that current transport can be approximated with equally sized and shaped grains. However, nonuniformity has been noted to have significant effects [20]. As illustrated in the left side of Fig. 4, the inhomogeneous nature of the grain structure can provide current transport paths that reduce the number of highly resistive grain boundaries along the way.

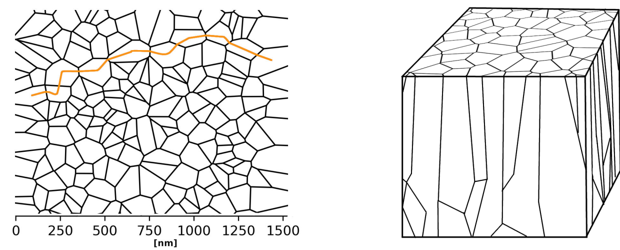

Fig. 4. Polystructure of inhomogeneous grain size distribution (left, average grain size 100 nm) can provide lower resistivity paths by minimizing the number of grain boundaries and maximizing the number of low-resistivity grains along the path. The example path (orange) encounters only nine grain boundaries, while a homogeneous 100-nm grain polystructure would have 14 grain boundaries. The column structure (right), often found in polysilicon films, has a very different grain size distribution depending on the direction. If the current direction is along the grains, the amount of encountered boundaries is much smaller making the effect of the boundaries very limited.

Previous works on polysilicon resistivity have been developed for 1-D analysis. A goal of this work is to investigate how much the grain size distribution affects calculated resistivity values. This would then provide a more detailed description of polysilicon resistivity useful for our further investigations on fine-tuning polysilicon.

The focus of our work is on the electrical properties of the topmost part of the polysilicon layer as a trap-rich layer for mitigating RF loss in the substrate [1]. As such, the relevant current conduction occurs mostly at the topmost few hundred nanometers and the deeper inner grain structure is therefore not within the scope of this work.

Our extension of resistivity modeling to two dimensions is based on the existing resistivity models [2], [3], Voronoi tessellation [21], and SPICE [22]. Voronoi tessellation is used to generate computationally usable polycrystalline-like structures. Individual grain-to-grain connections can be calculated with the established resistivity models. These individual connections are then connected to form a resistor network that we can simulate with a circuit simulator like SPICE. Ultimately, we get a process in which we can target specific grain size distributions, such as those found in real polysilicon samples. The method allows us to more accurately account for and quantify the differences in resistivities due to the nonuniformity in grain sizes and shapes.

A. Voronoi Diagrams

The first component of our tool is Voronoi tessellation [21]. It is a way of dividing a plane into regions (Voronoi cells). Such diagrams are used in many ways, one of which is to represent polycrystalline structures. Our Voronoi diagrams are generated with the Qhull [23] library. Our SEM measurement analysis (Section III) provides the grain size distribution for real polysilicon structures.

To produce similar cell size distributions with Voronoi tessellation, we control the size distribution with two parameters:

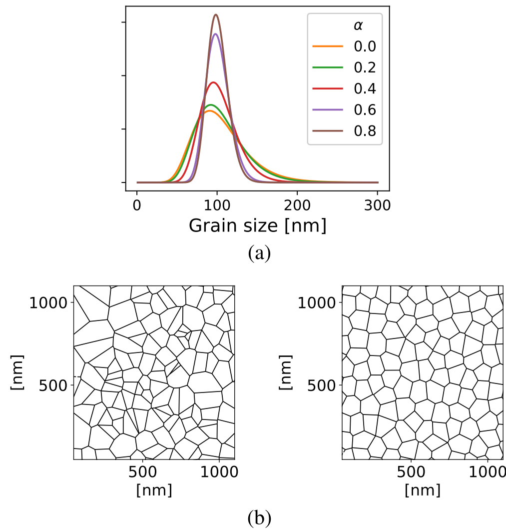

Fig. 5. Effect of regularity parameter on size distribution of the Voronoi diagram. Lower values produce more random diagrams allowing for larger and smaller sizes, while higher values are more ordered thus narrowing the range of possible cell sizes. (a) Grain size distribution with different regularity parameter values. (b) Example diagram with $\alpha = 0.0$ is shown on the left, the right shows $\alpha = 0.8$.

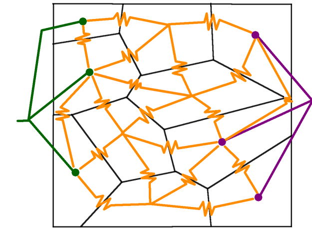

Fig. 6. Resistor network is formed from the Voronoi diagram, which represents the polycrystalline structure. The network is formed by connecting grains with resistors (orange) whose resistances are based on the potential barriers found at the grain boundaries. The network starts from the points on the left (green), which are connected to the voltage source. After all the grains are connected, the points on the right (purple) are connected to the ground.

the number of seed points in a given area and the regularity parameter α [24], which is given by

$$\alpha = \frac{\delta}{d_0}$$

where d_0 is the distance between seed points in a fully regular diagram of hexagons and δ is the acceptance threshold distance. A seed point is accepted if the distance between it and the existing seed points is below the threshold value.

Threshold $\delta = 0$ ($\alpha = 0$) results in a completely random Voronoi diagram. On the other end, when δ approaches d_0 ($\alpha = 1$), we get the uniform hexagon configuration. The effect of the regularity parameter is shown in Fig. 5(a), where we can see that the lower α values result in wider, more random cell size distributions.

The α parameter provides a way of narrowing the distribution. It, however, provides no way to widen the distribution. For these cases, we can pregenerate random diagrams, compare the target distribution and the Voronoi distributions, and discard the diagrams that provide too narrow distributions.

The α parameter controls the width of the generated grain size distribution as shown in Fig. 5(a). We wish to establish a connection between the width and resistivity. With our implementation, we, however, obtained distributions, which featured some large outlier grain sizes at the tails where we, on average, expect no grains. Given the limited size of the cell, these introduced a notable source of deviation to the resistivity values that is not related to the width of the distribution. To focus on how the width of the distribution and the positioning of the grains affect the resistivity, we filter these outlier grain sizes during the forming of the network. When the Voronoi diagram is generated, we first fit a log-normal distribution to the grain size distribution of the diagram. If we then encounter a notably large grain size, we sample a new grain size for that particular connection from the fit log-normal distribution.

B. SPICE

To examine the effect of grain size distribution on resistivity, we use the well-established circuit simulator SPICE. Specifically, Ngspice [25] is used with the Python interface PySpice [26].

We follow the thinking found in the model of Seto: current transport in polysilicon is a grain boundary-limited process. As such, grain resistivity has a negligible effect. The key is the potential barrier at the grain boundary that limits charge carrier transport.

Based on the potential barrier height (dependent on grain size, doping concentration, and trapping state density), grain size, and grain boundary length, we can calculate the resistance between two neighboring grains. Then it is a matter of connecting all the grains and their resistive grain boundaries into a resistor network, which allows us to investigate the effect of nonuniformity on the grain sizes. An example network is illustrated in Fig. 6.

The process of finding and forming the connections is programmatically done. The respective resistances of each connection are calculated as outlined in Section IV-C. By simulating the resistor network, we can obtain the resistivity of the whole Voronoi-diagram-based polysilicon structure.

C. Resistors

Resistivity calculations for the individual grain-to-grain connections in the Voronoi-SPICE model are based on the model of Seto (and later corrections by Lu). Proper derivations can be found in the original works by Seto [2] and Lu et al. [3].

The calculation is made for a 1-D grain-to-grain system of length L (grain size) with a grain center on each end and a grain boundary in the middle. A depletion region extends from the center boundary toward both the grain centers. The amount of charge trapped at the grain boundary and the width of the depleted region in the grains depend on the doping concentration and trapping state density. Our investigations have focused mostly on polysilicon with low doping. At these

low doping levels, some trap states remain unfilled. The width of the depletion region is the entire grain half on both sides of the boundary ($W = L/2$).

The resistivity of polysilicon is calculated by first solving the grain boundary potential barrier height V_B from Poisson's equation. By ensuring charge neutrality between ionized dopant atoms and charged traps, a formula for Fermi energy E_F (relative to the intrinsic case) can be derived. Carrier concentration n in the neutral region of the grain can then be estimated using the Maxwell–Boltzmann approximation. Charge carriers contributing to the overall current transport are those with high enough energy to overcome the potential barrier. Tunneling through the barrier is thought to be of negligible contribution and is ignored. Based on thermionic emission, one can calculate the current density of the charge carriers with high enough energy to overcome the barrier.

Later investigations [5], [6], [7] sought to provide different physically inspired corrections for matching experimental data and theoretical models; however, the model used here relies on a fitting factor f. It is a unitless scaling factor that is introduced since the thermionic-emission-based formulas overestimate the current density over the grain boundary. It is, in large part, to correct for scattering effects, which lowers the amount of charge carriers that can pass from grain to grain. It has very small to insignificant temperature dependence [3]. It is, however, dependent on the barrier height, which in turn is dependent on dopant concentration. This has been suggested to be due to diffusion mechanisms [6].

The resistivity (ρ) ultimately becomes

$$\rho = \frac{\sqrt{2\pi m^* kT}}{2Wq^2 fn} \exp\left(\frac{qV_B}{kT}\right) \quad (1)$$

where m^* is the effective mass of the free charge carrier, k is the Boltzmann's constant, T is the temperature, and q is the elementary charge.

With the grain size analyzed from the Voronoi diagram, we can proceed to estimate the grain boundary limited resistivity between the two connected grains.

Current transport in polysilicon is largely a grain boundary barrier-limited process. Our choice of doping concentrations in this work is mostly to highlight the barrier effects. For the trapping state energies and densities and the fitting factor f, we use the same values as in the article by Lu et al. [3].

V. Alternative Method for Estimating the Effect of Grain Size Distribution

Inspired by the work of Park et al. [27], we can also estimate the effect of grain size distribution on the resistivity in a simpler way without the Voronoi diagrams and SPICE networks.

For a sample with a given grain size distribution, width, and length, we want to estimate the effect of grain sizes on resistivity. We divide the sample into long, narrow channels. We sample random grain sizes until we reach the sample length. The process is done for each of the channels until the width is reached. The grain sizes are sampled from a log-normal distribution whose parameters are acquired by fitting them to the given grain size distribution.

TABLE I

Resistivity Differences Between the 1-D and Models That Account for the Grain Size Distribution. All Are Calculated With the Same Average Grain Size of 100 nm. Parallel Channels Refers to the Method Described in Section V, While Voronoi-SPICE Is Calculated With the Method Outlined in Section IV

	Resistivity [kΩ · cm]
Square grain / 1D	380
Parallel channels	360
Voronoi-SPICE	190

The resistances can be calculated with the 1-D resistivity model for generated grain sizes. All the grains in the channel get connected in series for the channel resistance. Connecting the channels in parallel provides us with the overall resistivity of the sample.

The resistivities calculated in this manner were slightly smaller than the 1-D model. The largest differences to 1-D values were around 10% with singular cases. Table I shows the averaged resistivity for the 100 nm, $\alpha = 0$ test case. The parallel channels' value is around 5% smaller than the 1-D value. Difference to the 1-D values was even smaller with the more narrow distributions found in Table II, with the method giving essentially the same values as those of the 1-D model.

This approach seemingly fails to capture the full effect of differing grain sizes, orientations, and positions in the polysilicon film. As the following section shows, we found the effect of the incorporation of grain size distribution into the resistivity calculations to be noticeably larger.

VI. Results

The 1-D resistivity values, depending on the situation, were found to be often over twice as large as the 2-D Voronoi-SPICE values. The random nature of grain ordering and sizes, however, introduced also quite noticeable variances in resistivity values.

In this section, we first introduce some results that highlight the relationships between grain size distributions and resistivities while also providing testing that our approach works as intended. After this, we provide results that use the whole process outlined in this work: acquiring a grain size distribution, fitting our Voronoi model to it, and calculating its resistive properties.

For testing, a grain size distribution generated with $\alpha = 0.0$ and 100 cell points in 1 μm^2 area resulting in an average grain size of 100 nm is used. A special case diagram can be constructed for verification between the 1-D model and the Voronoi-SPICE method by creating a diagram of equally sized squares such that the grains are aligned so that the grain boundaries are perpendicular to the electric field. Since there is no variation in grain size, orientation, or shape, it provides the same values as the 1-D formulas.

Resistivities for these can be found in Table I, which shows that the special case square grain/1-D model has roughly double the resistivity of the Voronoi-SPICE with the varying grain sizes.

To examine the effect of regularity parameter on resistivity, we performed calculations with 500 Voronoi diagrams per

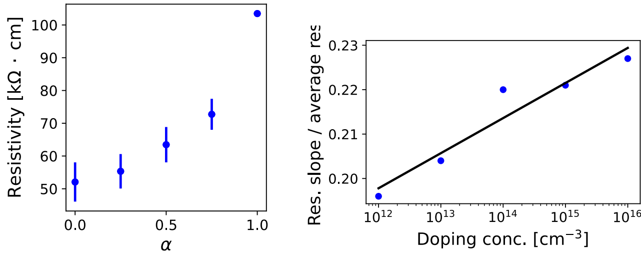

Fig. 7. Figure on left shows the resistivity as a function of the regularity parameter α. Bars show the standard deviation in resistivity values per α. Higher grain sizes found with the more spread out grain size distributions can provide current transport paths with fewer grain boundaries lowering overall resistivity. The relative standard deviation of the resistivity values gets smaller as α increases since the resulting grain size distribution becomes more regular. The slope for α dependence of the resistivity is calculated with different doping concentrations (on the right). The increase in doping concentration increases the importance of the potential barriers at grain boundaries thus in turn increasing the effect of α parameter.

α value ($\alpha = 0, 0.25, 0.5, 0.75, 1$). Each diagram contained 200 grains with an average grain size of 100 nm (about $1.5 \times 1.5\ \mu$m).

In Fig. 7 (left), the effect of the Voronoi diagram's regularity parameter on the resistivity is shown. As we increase the regularity parameter, we can see an increase in resistivity. More random structures tend to produce wider size distributions, which can provide current paths with fewer grain boundaries lowering overall resistivity.

Positioning of the grains inside the box has a significant effect, as this ultimately produces the different current paths. The current conduction path of least resistance (and least grain boundaries) can be thought of in terms of an effective grain size, which might differ from the average grain size. Since the resistivity of polysilicon is fairly sensitive to grain size, this can result in a noticeable deviation in resistivity values.

Relative standard deviation is calculated ($\sigma_\rho/\overline{\rho}$) to examine the variance in resistivity between different simulations and α values. We see smaller variation in resistivity values with the higher values of α as the resulting grain size distribution becomes narrower. Smaller values of α typically produce more random and broader size distributions, resulting in larger variations in resistivity values.

The α resistivity calculations are repeated for different doping concentrations. The relative increase in resistivity with increasing α is calculated for different concentrations (slope in Fig. 7 (left), $(\Delta\rho/\Delta\alpha)$). The slopes with different doping concentration values are shown in Fig. 7 (right). With low doping concentrations, the potential barrier has fewer charges trapped, and thus its effect is smaller. This in turn reduces the effect of width of grain size distribution (α). Increasing the doping increases the effect of the barriers (up until all the trap states are filled).

The 2-D resistivity calculation process with the Voronoi-SPICE method is done for distributions found in: 1) our molecular dynamics simulations (Section II) and 2) real polycrystalline silicon as analyzed from an SEM image of a sample (Section III). Using the average grain size and α parameter, we generate Voronoi diagrams with matching size distributions and construct the resistor networks. We also calculate the resistivity with 1-D, average grain-based calculations for comparison. The results can be found in Table II. Overall, 2-D values were found to be on average about half the 1-D values ($\rho_{2D} = 0.55 \cdot \rho_{1D}$). The limited size of the simulation box sets a size limit on the grain sizes found. The grain size distribution from the real polysilicon sample was significantly wider. To match the Voronoi tessellations, we generated many with $\alpha = 0$ and discarded those that resulted in too narrow distributions. With the grain size distribution from the SEM analysis of the sample, the resistivity dropped to a quarter of the 1-D value ($\rho_{2D} = 0.25 \cdot \rho_{1D}$). With very large grains, we obtain the expected behavior: the resistivity approaches that of single-crystal silicon.

TABLE II

EFFECT OF GRAIN SIZE DISTRIBUTION ON RESISTIVITY. TWO-DIMENSIONAL VALUES ARE CALCULATED USING THE VORONOI-SPICE METHOD WITH DIFFERENT GRAIN SIZE DISTRIBUTIONS AND COMPARED WITH 1-D AVERAGE GRAIN SIZE RESISTIVITY MODEL. GRAIN SIZE DISTRIBUTION DATA ARE FROM OUR MD GROWTH SIMULATIONS AND THE ANALYSIS OF SEM IMAGES. CALCULATIONS AT LARGE GRAIN SIZES (3000 nm AS AN EXAMPLE) SHOW THAT THE RESISTIVITY APPROACHES THAT OF SINGLE-CRYSTAL SILICON. THE SINGLE-CRYSTAL VALUE IS CALCULATED BASED ON [28]. EXPERIMENTAL DATA ARE FROM FOUR-POINT MEASUREMENTS (SECTION III). DOPING CONCENTRATION WAS CHOSEN TO BE 10^{15} cm^{-3}

Source of grain size data	Average grain size [nm]	Resistivity 1D [Ω · cm]	Resistivity 2D [Ω · cm]
Growth sim.	2.3	$5.5 \cdot 10^7$	$3.0 \cdot 10^7$
Growth sim.	2.4	$5.0 \cdot 10^7$	$2.8 \cdot 10^7$
Growth sim.	3.0	$3.2 \cdot 10^7$	$1.8 \cdot 10^7$
SEM	175	$1.1 \cdot 10^4$	$4.5 \cdot 10^3$
Voronoi tess.	3000	35	17
Single crystal Si		5	
Experimental (175 nm)		$2.2 \cdot 10^3 - 1.5 \cdot 10^4$	

VII. SUMMARY AND CONCLUSION

In this work, we have developed a method with which we can target specific grain size distributions found in polysilicon and estimate the effect of distribution on resistivity. Due to larger grain sizes found in size distributions, the current can find paths of low resistance by avoiding smaller grains. The grains themselves are of relatively small resistivity, whereas the grain boundaries with trapped charges produce barriers that impede current transport.

In our previous work, we performed molecular dynamics simulations of the growth of polysilicon. These provide us with computational polysilicon samples, whose grain structures we can analyze. Here, we have presented several ways of estimating the impact of the grain structure on resistivity: the block model of equally sized cubic grains, the series/parallel connected channels, and the Voronoi-SPICE-based method. We have also analyzed a polysilicon sample experimentally. The effect of grain size distribution of a real polysilicon sample on resistivity has also been estimated with the Voronoi-SPICE method.

A lot of work has been done on the modeling of polysilicon resistivity [2], [3], [4], [5], [6], [7], a large part of it is focusing on the mechanisms relating to grain boundary barriers and the

charge carriers trying to overcome them. However, as we have shown in this work, the inhomogeneity of polysilicon can also have a noticeable impact on the resistivity. By taking grain size distribution into account, we found resistivity to often drop to half of the average grain-size-based resistivity values. With wider size distributions, the drop in resistivity was found to be even larger.

More detailed handling of mechanisms involved in current transport (thermionic emission together with tunneling, drift-diffusion transport, barrier scattering, dopant diffusion, etc.) could be a future improvement to further widen the range of applicability of the approach. However, for the purposes of our work, the model of Seto [2] and Lu et al. [3] was sufficient. With it, we were able to show the effect that grain size distribution produces.

Another consideration would be the third dimension. However, a commonly found structure in polysilicon films is the columnar structure [29], [30] (see Fig. 4 right side). In such a system, grain boundaries and grain size distribution mostly play a part when charge carriers cross through these columnar grains perpendicular to the long axis of the grains. Finally, an interesting area of investigation would be boundary types, since not all grain boundaries feature the same trapping states. Grain boundaries with little mismatch (symmetric, low angle, etc. boundaries) would produce less trapping states than those with more mismatch. The effect of the distribution of different boundary types could be a future improvement.

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