TURUN YLIOPISTO
UNIVERSITY OF TURKU

GCMO-Based Memristors for Future Neuromorphic Processors

Anni Antola

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Dedicated to my family.

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ABSTRACT

This dissertation investigates resistive switching (RS) and neuromorphic functionality in memristor devices based on the mixed-valence perovskite manganite $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO), with emphasis on the role of substrates and interfacial processes in device operation. Particular focus is placed on how structural quality, substrate-induced defects, and interfacial redox processes influence the switching characteristics of the devices and enable both volatile and non-volatile RS.

Thin-film GCMO layers were fabricated using pulsed laser deposition on different substrates, allowing control of crystallinity and defect density through substrate selection and growth conditions. Structural properties were characterized using X-ray diffraction, and the electrical behavior of the devices was studied through current-voltage measurements together with retention and endurance tests. Memristor devices with different active areas and electrode configurations were formed by depositing patterned metal electrodes on the GCMO films, creating an active AlO_x/GCMO interface responsible for resistive switching.

The results show that the switching behavior of GCMO memristors is influenced by the structural quality of the films and the defect landscape induced by the substrate. High-quality epitaxial films exhibit stable bipolar resistive switching, while variations in crystallinity modify the state retention through increased oxygen back-diffusion in polycrystalline thin films. Through X-ray photoelectron spectroscopy and area-dependent RS, the redox-active Al/GCMO interface is found to play a central role in the formation and modulation of resistive states.

In addition to synaptic functionality in crossbar-compatible devices, the results indicate neuronal-like behavior such as leaky-integrate dynamics. These findings highlight the potential of GCMO memristors as building blocks for future neuromorphic device architectures.

KEYWORDS: GCMO, memristor, resistive switching, synaptic network, crossbar array, neuromorphic processor

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TIIVISTELMÄ

Tässä väitöskirjassa tutkitaan resistiivistä kytkeytymistä (resistive switching, RS) ja neuromorfista toiminnallisuutta memristoreissa, jotka perustuvat sekavalenttiseen perovskiittimanganiittiin $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO). Työssä tarkastellaan erityisesti substraattien ja rajapintaprosessien merkitystä laitteiden toiminnassa. Erityistä huomiota kiinnitetään siihen, miten rakenteellinen laatu, substraatin aiheuttamat viat sekä rajapintojen redoksiprosessit vaikuttavat laitteiden RS-ominaisuuksiin ja mahdollistavat sekä haihtuvan että ei-haihtuvan resistiivisen kytkeytymisen.

Ohuet GCMO-kalvot valmistettiin pulssilaserpinnoituksella erilaisille substraateille, mikä mahdollisti kiteisyyden ja vikatiheyden hallinnan kasvualustojen ja -olosuhteiden avulla. Rakenteellisia ominaisuuksia karakterisoitiin röntgendiffraktiolla, ja laitteiden sähköistä käyttäytymistä tutkittiin virta-jännitemittauksilla sekä tilojen pysyvyyden ja kestävyyden testeillä. Memristorilaitteita, joissa oli erilaisia aktiivisia pinta-aloja ja elektrodigeometrioita, valmistettiin pinnoittamalla GCMO-kalvojen päälle kuvioituja metallielektrodeja, jolloin muodostui resistiivisestä kytkeytymisestä vastaava aktiivinen AlO_x/GCMO-rajapinta.

Tulokset osoittavat, että GCMO-memristorien kytkeytymiskäyttäytyminen riippuu kalvojen rakenteellisesta laadusta sekä substraatin aiheuttamasta vikarakenteesta. Korkealaatuiset epitaksiaaliset kalvot osoittavat vakaata kaksisuuntaista resistiivistä kytkeytymistä, kun taas kiteisyyden vaihtelut vaikuttavat tilojen säilyvyyteen lisääntyneen hapen takaisindiffuusion seurauksena monikiteisissä ohutkalvoissa. Röntgenfotoelektronispektroskopian ja pinta-alasta riippuvan resistiivisen kytkeytymisen perusteella redoksisesti aktiivisen Al/GCMO-rajapinnan havaittiin olevan keskeisessä roolissa resistiivisten tilojen muodostumisessa ja muokkaamisessa.

Synaptiseen toiminnallisuuteen soveltuvat laitteet ovat yhteensopivia ristikkoverkkoarkkitehtuurien kanssa, ja tulokset osoittavat myös neuronaalista käyttäytymistä, kuten vuotavan integraation (leaky-integrate) dynamiikkaa. Nämä havainnot korostavat GCMO-memristorien potentiaalia tulevaisuuden neuromorfisten laitearkkitehtuurien rakennuspalikoina.

ASIASANAT: GCMO, memristori, resistiivinen kytkentä, synaptinen verkko, ristikkorakenne, neuromorfinen prosessori

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June 2026
Anni Antola

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Abbreviations

AFM	Atomic Force Microscopy
AI	Artificial Intelligence
ALD	Atomic Layer Deposition
ANN	Artificial Neural Network
BE	Bottom Electrode
BL	Bit line
CMOS	Complementary Metal-Oxide-Semiconductor
EBPVD	Electron Beam Physical Vapor Deposition
EDS	Energy-Dispersive X-ray Spectroscopy
GCMO	$Gd_{0.2}Ca_{0.8}MnO_3$
HRS	High-Resistance State
HV	High-Vacuum
IV	Current-Voltage
LAO	$LaAlO_3$
LCMO	$La_{1-x}Ca_xMnO_3$
LIF	Leaky Integrate-and-Fire
LRS	Low-Resistance State
LSMO	$La_{1-x}Sr_xMnO_3$
LTP	Long-Term Potentiation/Plasticity
MIM	Metal-Insulator-Metal
NGO	$NdGaO_3$
PCMO	$Pr_{1-x}Ca_xMnO_3$
P–F	Poole–Frenkel (Conduction)
PLD	Pulsed Laser Deposition
RESET	Reset Switching Process
RIE	Reactive Ion Etching
RS	Resistive Switching
RV	Resistance-Voltage
SCLC	Space-Charge-Limited Conduction
SEM	Scanning Electron Microscopy
SET	Set Switching Process
SMU	Source Measure Unit
SNN	Spiking Neural Network

SRO	$SrRuO_3$
STDP	Spike-Timing-Dependent Plasticity
STO	$SrTiO_3$
STP	Short-Term Potentiation/Plasticity
TE	Top Electrode
TMO	Transition Metal Oxide
UHV	Ultra-High-Vacuum
VCM	Valence Change Mechanism
WL	Word Line
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffractometry
XRR	X-ray Reflectivity

List of Original Publications

This dissertation is based on the following original publications, which are referred to in the text by their Roman numerals:

I A. Antola, I. Angervo, H. Huhtinen, M. Miettinen, A. Schulman and P. Paturi. *Structurally simplified GCMO crossbar design for artificial synaptic networks*. Applied Physics Letters, 124, 2024, 253502.

II A. Antola, J. Laaksonen, H. Huhtinen, I. Angervo, S. Granroth, A. Schulman, P. Laukkanen and P. Paturi. *Area-Dependent Resistive Switching and Interfacial Dynamics in GCMO-Based Memristors*. ACS Applied Electronic Materials, 7(9), 2025, 4242–4250.

III I. Angervo, A. Antola, A. Schulman, H. Huhtinen and P. Paturi. *The effect of substrate-induced defects on structural and resistive switching properties in $Gd_{0.2}Ca_{0.8}MnO_3$ thin films*. AIP Advances, 14, 2024, 045309.

IV I. Angervo, L. Miettinen, A. Antola, H. Huhtinen and P. Paturi. *Leaky-integrate functionality in $Gd_{0.2}Ca_{0.8}MnO_3$-based neuromorphic devices*. ACS Applied Electronic Materials. Submitted 2026.

Articles relevant to this work but not included in this dissertation:

V I. Angervo, A. Antola, T. Vaimala, A. Malmi, A. Schulman, H. Huhtinen and P. Paturi. *Importance of growth method and substrate-induced crystalline quality in Al/$Gd_{0.2}Ca_{0.8}MnO_3$/Au memristor devices*. Journal of Physics D: Applied Physics, 57, 2024, 415301.

VI V. M. M. Paasonen, I. Angervo, A. Antola, H. Huhtinen and P. Paturi. *Scalable and environmentally friendly production of perovskite manganite thin films for neuromorphic applications*. Thin Solid Films, 798, 2024, 140381.

Patents related to this work:

P1 P. Paturi, H. Huhtinen, A. Antola, I. Angervo and A. Schulman. *Memristor array and method of manufacturing thereof.* WO2025093822A1, 2025.

P2 P. Paturi, H. Huhtinen, A. Antola and I. Angervo. *Physical artificial neuron and method of manufacture thereof.* FI20253179, filed June 2025.

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1 Motivation

Rapid growth in artificial intelligence (AI) and data-driven applications is pushing conventional complementary metal-oxide-semiconductor (CMOS) technology towards its physical and architectural boundaries. In the traditional von Neumann architecture, memory and processing are physically separated, creating a fundamental performance bottleneck due to the continuous transfer of data between memory and processing units [1, 2]. Modern AI relies on massive parallelism and frequent memory access, increasing the power consumption of the system [3, 4]. One promising approach to solving these computational limitations is neuromorphic computing, an architecture inspired by biological neural systems, where memory and computation are co-located within interconnected synapses and neurons [5–7].

Neuromorphic computing requires hardware elements capable of both storing state and performing computation locally. Such functionality can be implemented using resistive switching (RS) devices [8, 9]. Resistive switching refers to the reversible modulation of electrical resistance under an applied electric field [10, 11], characteristic of memristive (memory-resistive) devices first theoretically formalized by Leon Chua in 1971 as a circuit element linking charge and magnetic flux [12]. Their operating history- and state-dependent resistance enables operation analogous to synaptic weight modulation [8, 13, 14]. Memristors can be arranged in dense crossbar arrays, implementing parallel, in-memory computation [5, 7, 15, 16].

Memristive behavior can arise from several microscopic mechanisms [13, 17, 18]. For phase-change materials, the resistivity modulation emerges from a reversible transition between the amorphous and crystalline phases of the material [19]. Ferroelectric devices utilize polarization reversal, i.e., spontaneous dipole alignment to modulate resistance [20], while spin-transfer torque magnetoresistive devices exploit the spin-manipulated magnetization of the device [21, 22]. In electrochemical metallization devices, the conduction change comes from metal ions drifting within the material stack [23–25]. In the widely researched oxide-based systems, such as the TiO_2-based memristor introduced by R. Stanley Williams' group at Hewlett-Packard Labs in 2008 [26], the switching is often governed by oxygen-vacancy-mediated valence-change mechanisms [10, 27, 28].

Among memristive material systems, transition-metal oxides (TMOs) provide a particularly versatile platform for resistive switching due to the strong coupling between electronic transport and defect dynamics [29, 30]. In these materials, the

migration and redistribution of oxygen vacancies under an applied electric field modifies the local electronic conductivity and interfacial barrier properties [27, 31, 32]. Depending on device structure and material properties, defect redistribution can either form localized conductive filaments or occur in a more spatially distributed manner within defect-rich regions, such as interfacial layers or two-dimensional slabs in the oxide [28, 33, 34].

For neuromorphic applications, interface-controlled resistive switching is especially desirable [27, 28]. Unlike filamentary switching, which involves the formation and rupture of narrow conductive paths and often results in abrupt and stochastic resistance changes [35, 36], interface-type switching enables continuous and reproducible resistance modulation through changes in electrode-oxide interface conductivity and barrier properties. These changes may result, for example, from oxygen-vacancy redistribution near the interface, modifying the local transition-metal valence and conductivity, or from reversible oxidation and reduction of the active electrode/oxide interface, which gradually changes the effective injection barrier [27, 28, 37]. This gradual, multistate nature is essential for implementing analog synaptic and neuronal functionality [38, 39]. Mixed-valence manganites are particularly well suited for interface-controlled switching due to their electronic structure and defect chemistry, which are highly sensitive to local oxygen stoichiometry in both the bulk and at metal–oxide interfaces [40]. Electric-field-driven oxygen ion or vacancy migration can modulate the interfacial electronic barrier and carrier transport without requiring the formation of conductive filaments [41, 42].

In this thesis, the discussion will center on a particular oxide-based memristive system, the mixed-valence perovskite manganite $Gd_{1-x}Ca_xMnO_3$, chosen for its tunable RS characteristics that stem from interfacial effects [43]. Previous works related to the manganite show intriguing promise of the material due to its complex magnetic phase transitions, and the role of oxygen vacancies in lattice coupling [44–49], establishing its capacity for bipolar resistive switching, forming-free operation across a wide doping range, and bio-plausible synaptic functionality [43, 50, 51]. Yet, these studies remained largely restricted to phenomenological observations of IV hysteresis and general transport properties.

Prior to this work, the relationship between the $Gd_{1-x}Ca_xMnO_3$ thin film structural quality and interfacial redox processes in regulating the switching mode and the emergence of bio-plausible functionality remained incompletely understood. The knowledge of these relationships is essential for both fundamental physics and reliable neuromorphic processor implementation in the future. Accordingly, this thesis studies $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) thin films and devices, connecting material/defect structure to resistive switching behavior in practical geometries. The central question addressed in this thesis is:

How do the material properties and interfacial physics of GCMO-based memristors determine their resistive switching behavior and enable both synaptic and neuronal functionality?

To answer this question, this work examines the structural, chemical, and electrical properties of GCMO thin films and devices using a wide range of characterization techniques. The study focuses on the role of substrate-induced crystallinity [III] and identifies the oxidized aluminum/GCMO interface as the primary driving force behind the observed resistive switching [II]. By linking material structure to electrical behavior, this thesis establishes the physical mechanisms governing resistive switching in GCMO memristors, investigates the emergence of synaptic [I] and neuronal properties [IV], and examines their suitability for next-generation neuromorphic processors.

2 Theory

2.1 Resistive Switching in Oxide Materials

2.1.1 Conduction Mechanisms in Oxides

Understanding the electrical transport properties of oxide-based memristors is vital to interpreting resistive switching. In memristive devices, current-voltage (IV) characteristics provide indirect but informative evidence of the dominant charge transport mechanism. Generally, transport is categorized as either interface-limited or bulk-limited [32, 52, 53]. In the interface-limited regime, conduction is dictated by how carriers are injected across the electrode-oxide barriers, while bulk-limited conduction is controlled by carrier transport through the oxide itself, often influenced by traps or space-charge effects. When analyzing these field-driven effects, the electric field is typically simplified to an effective estimate $E \approx V/d$ (V being voltage and d distance), while the actual field distribution may be non-uniform, especially in interface-dominated devices. Resistive switching in oxide-based devices does not arise from these transport mechanisms themselves, but from physical modifications of the regions that limit transport, including changes in interfacial barriers, redistribution of defects in the insulating bulk, or formation of localized conductive pathways. These structural and chemical changes alter the effective conduction regime observed in IV characteristics [10, 11, 29, 54].

Ohmic Conduction Ohmic conduction represents the simplest transport regime, corresponding to the linear scaling $I \propto V$ in a given resistance state and bias range. Ohmic conduction is associated with low-field transport, sufficiently ohmic electrical contacts, or highly conductive regions such as filaments or reduced interfacial barriers [52–54].

Space-Charge-Limited Conduction (SCLC) SCLC describes bulk-limited transport when injected carriers dominate over equilibrium carriers. At higher voltages, the injected carriers can exceed the equilibrium carrier concentration, creating a space charge or an internal electric field distribution that limits further carrier injection. Idealized trap-free SCLC gives $I \propto V^2$, while trap-controlled SCLC yields higher apparent power-law exponents [32, 53–55].

Poole–Frenkel (P–F) Emission Poole–Frenkel conduction is a bulk-limited, field-assisted emission of carriers from trap states in an insulating oxide. P–F emission can be observed in the cases of higher device resistance, when electrical transport happens through an insulating oxide containing defect states such as oxygen vacancies [32, 53, 54, 56].

Schottky Emission Schottky emission describes the thermionic excitation of carriers over a potential energy barrier at a metal-oxide (or metal/semiconductor) interface. Schottky-type emission is especially relevant when the contact barrier dominates the overall resistance, such as in interface-controlled cases [52, 53, 56].

Tunneling Tunneling is applicable in ultra-thin oxides or electrode interfaces where barrier width becomes sufficiently small (typically below a few nanometers), as electrons may tunnel through these thin insulating barriers. This tunneling can either be direct or via defects or traps, e.g., Fowler–Nordheim tunneling [32, 53, 57].

Hopping Transport In the bulk of correlated oxides such as manganites, charge transport often occurs through thermally activated hopping between localized states, rather than conventional band transport. This transport is commonly described as small-polaron hopping, arising from strong coupling between electronic and lattice degrees of freedom. Hopping transport, and therefore the bulk conductivity, is highly sensitive to defect concentration, oxygen stoichiometry, and lattice distortions, making it particularly relevant in mixed-valence manganites [40, 53, 54, 58, 59].

Relation to Resistive Switching Behavior Conduction mechanisms are commonly described based on the functional dependence of current on voltage, although similar IV behavior can emerge from different microscopic processes [32, 53]. Often, multiple mechanisms coexist in a single device, with different transport processes contributing in series or parallel depending on the device state and bias [32, 54]. Resistive switching can be viewed as an electrically driven modification of transport-limiting regions, which changes the relative contributions of interface-limited and bulk-limited conduction processes, altering the effective conduction regime observed in IV measurements [10, 30].

The dominant conduction mechanism often depends on the resistive state of the device [54]. The low-resistance state (LRS) can exhibit ohmic-like conduction due to highly conductive pathways or reduced barrier resistance, while tunneling may contribute when interfacial barriers become sufficiently thin [32, 53]. In contrast, the high-resistance state (HRS) is typically governed by interface-limited Schottky emission or bulk-limited P–F conduction, reflecting transport across more insulating regions or defect-controlled barriers [32, 53, 54].

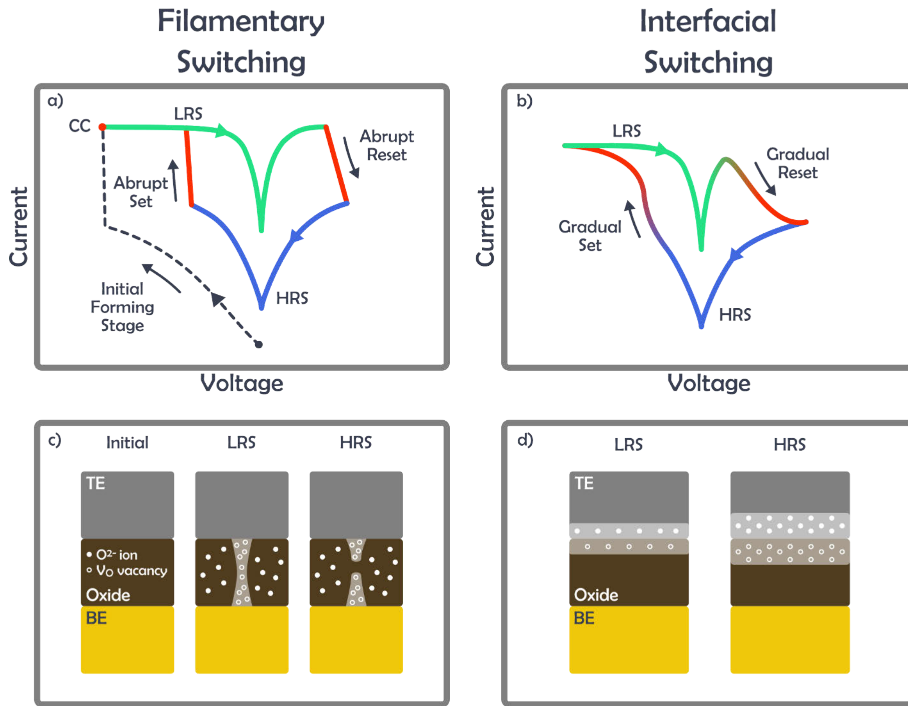

Figure 1. Comparison of filamentary and interface-controlled valence change mechanisms (VCM). (a) Schematic IV characteristics of filamentary switching showing abrupt SET/RESET transitions, an electroforming step, and current compliance (CC). (b) Schematic IV characteristics of interface-controlled switching exhibiting gradual and continuous resistance modulation. (c) Schematic illustration of conductive filament formation via oxygen vacancy linking between the top electrode (TE) and bottom electrode (BE). (d) Schematic illustration of resistive switching driven by modulation of an interfacial oxide layer via redox-driven oxygen migration.

However, these assignments are not unique from IV fitting alone: ohmic conduction follows $I \propto V$, whereas Schottky emission, P–F emission, and trap-assisted tunneling can all produce similar nonlinear voltage dependencies. Therefore, these mechanisms should be treated as effective transport descriptions rather than unique microscopic assignments unless supported by separate experimental evidence [32, 53].

2.1.2 Filamentary and Interfacial Resistive Switching

Resistive switching refers to the reversible change in device resistance induced by an applied electric field [10]. This behavior is often observed as a pinched hysteresis loop in current-voltage measurements, reflecting the operating history-dependent resistance state of the device [12, 26].

In oxide materials, resistive switching is primarily caused by the migration of

oxygen ions and vacancies, or the so-called valence change mechanism (VCM) [10]. An oxygen vacancy (V_O) is a point defect corresponding to a missing oxygen ion (O^{2-}) in the crystal lattice, often treated as effectively positively charged, and can drift under an applied electric field [10, 27]. Depending on the material complex and defect distribution, this field-driven ionic motion can lead to varied spatial redistribution of vacancies. In some cases, the ions/vacancies can be pushed to form a narrow conductive filament bridging the two electrodes, or in other cases, the vacancy redistribution can occur more uniformly across the oxide thickness or it can be confined near the electrode-oxide interfaces [10, 27]. Accordingly, oxide-based RS mechanisms are commonly classified into three broad categories: filamentary switching, interfacial switching, and bulk-controlled switching [18, 27, 28, 60]. This redistribution modifies transport-limiting regions, such as interfacial energy barriers or conductive pathways, thereby altering the overall device resistance characteristics.

Typical oxide-based memristors follow the metal-insulator-metal (MIM) structure, where the oxide material is sandwiched between two electrodes, and their fabrication is well established using CMOS-compatible thin-film deposition techniques [10, 11, 17]. Depending on the case, these top and bottom electrodes (TE and BE, respectively) can either be symmetric (same material) or asymmetric (different material), affecting the nature of the metal-oxide interfaces. At each metal-oxide interface, a potential barrier typically forms due to differences in work function and electronic structure between the electrode and oxide [52]. These interfacial barriers can also dominate charge injection and can therefore control the overall device resistance [27]. Under an applied electric field, oxygen vacancies migrate within the oxide, the drift direction determined by the local electric field.

The schematics in Fig. 1 illustrate conventional vertical MIM devices, which are commonly used to introduce general RS mechanisms. However, oxide memristors can also be realized in lateral geometries, where the active oxide film is grown directly on an insulating substrate and contacted without a continuous metallic bottom electrode. This lateral or planar configuration can be advantageous when substrate-controlled thin-film crystallinity, strain, and texture are central to the device behavior, motivating its use in this thesis.

Filamentary switching describes the case where the oxygen vacancies form a conductive filament that ruptures and regenerates based on the polarity of the electric field. The abrupt nature of the SET (filament formation) and RESET (filament rupture) operations is typical for filamentary switching [10, 34, 36]. Filamentary switching often requires larger forming voltages to form the initial filament. With compliance, the current can be limited thus controlling the filament formation to prevent overgrowth [10]. Because current flows through a localized conductive filament, the low-resistance state is largely independent of device area [10, 27]. Filamentary RS is often binary-like or digital, and the devices suffer from significant variability due to stochastic filament formation and rupture [10, 34, 36]. The typical IV char-

acteristics of filamentary switching can be observed in Fig. 1a and c. Filamentary switching can exhibit either bipolar or unipolar switching behavior depending on the material system and device structure. In bipolar switching, opposite polarity voltages are needed to switch the system between high- and low-resistance states, while unipolar switching occurs with varied amplitude voltages in one polarity [27].

In interface-type switching, the asymmetry of the electrode materials allows the modification of the interfacial barrier at one of the electrodes, the active electrode [27, 28]. In most cases, the active electrode will experience natural oxidation, creating an insulating barrier [41, 61–63]. Under an applied electric field, oxygen ions or vacancies migrate across the interface, modulating the thickness and defect concentration of the insulating interfacial layer. This oxygen vacancy redistribution modifies the effective Schottky barrier height and width, and can influence multiple transport processes such as tunneling and trap-assisted conduction. Such changes directly affect the carrier injection and transport across the interface, leading to gradual and reversible resistance modulation without formation of localized conductive filaments [18, 27]. The gradual and analog nature of the resistance modulation, as seen in Fig. 1b and d, is the fundamental characteristic in bipolar interface-type switching. Interface-type devices do not require high forming voltages or compliance to get operational [27, 28, 39]. As the oxygen redistribution happens more uniformly at the interface, both the HRS and LRS have distinct area dependency, and this property can be considered a key identifier of non-filamentary RS [27, 28, 64].

For some material systems, resistive switching is not confined to a single localized filament or a narrow interface region, but may involve the formation of multiple conductive paths distributed throughout the oxide layer [10, 29]. Such multifilamentary switching can result in comparatively uniform and gradual resistance modulation compared to single-filament devices [10]. In these cases, the overall conduction can exhibit partial or full device-area dependence, depending on the size, density and distribution of conductive filaments [10].

Overall, oxygen ion and vacancy migration enable reversible RS by locally modulating the material's conductivity and interfacial energy barriers [10, 29, 31]. While ionic motion is inherently slower than electronic transport and exhibits strong field and temperature dependence, oxide-based RS remains attractive due to its low operating power, scalability, and compatibility with conventional semiconductor processes [10, 17]. Compared to alternative memristor-based memory concepts such as phase-change memory, oxide-based RS offers lower switching energy and higher density implementation, making it a promising candidate for emerging memory and neuromorphic computing applications [17, 19].

In this thesis, area scaling, forming requirements, self-compliance and cycle-to-cycle variability are treated as essential experimental indicators: filamentary switching typically shows weak LRS area dependence and higher stochasticity [10], whereas interface-type switching tends to exhibit more gradual, area-related resistance mod-

ulation consistent with barrier-controlled conduction [28, 39, 61].

2.2 Mixed-valence Manganites

2.2.1 Structural Properties and Electronic Transport

Binary metal oxides with the general chemical formula MO_x (M being metal, O oxygen) have long served as model systems for experimentally studied resistive switching. Common examples include TiO_2 [26, 65, 66], Ta_2O_5 [33, 67], and HfO_2 [34, 68, 69], where switching is often filamentary in nature.

Many complex oxides crystallize in the perovskite structure with the general formula ABX_3, whose high-symmetry reference form is the ideal cubic perovskite [40, 70]. In this ideal cubic perovskite structure (space group $Pm\bar{3}m$), the large A cation is located at the cubic unit cell corners, the smaller B-site cation at the body center, and the X anions at the face centers. In the perovskite oxide case, the anions are oxygen ions, forming ABO_3 [70]. These materials offer flexibility in tuning the electronic transport properties, as the crystal lattice complexity allows for more freedom to modify the material composition [40, 71, 72].

Perovskite oxide structures include manganites, where the B-site cation is manganese (Mn), with the chemical formula of $AMnO_3$. These perovskite manganites can also be doped, $A_{1-x}A'_xMnO_3$, in which the aliovalent A-site doping provides an additional degree of freedom to tailor the electronic behavior and control over the charge carrier and oxygen ion concentrations [40]. Examples of such memristive mixed-valence manganites include $Pr_{1-x}Ca_xMnO_3$ (PCMO) [38, 41, 73] and $La_{1-x}Ca_xMnO_3$ (LCMO) [74, 75], where praseodymium Pr^{3+} and lanthanum La^{3+} are rare earth elements and calcium Ca^{2+} alkaline earth metal. The crystal lattice is determined by the Goldschmidt Tolerance Factor t [40, 76, 77], which can be calculated from the ionic radii of these elements:

$$t = \frac{r_A + r_\mathrm{O}}{\sqrt{2}\,(r_B + r_\mathrm{O})}, \tag{1}$$

where r_A, r_B, and r_O are the effective ionic radii of the A-site cation, the B-site cation (here Mn), and oxygen, respectively. For aliovalently doped manganites, $A_{1-x}A'_xMnO_3$, the relevant A-site radius is typically defined as the composition-weighted average,

$$\langle r_A \rangle = (1-x)\, r_A + x\, r_{A'}, \tag{2}$$

while the B-site radius may be approximated by a corresponding average over Mn valence states (e.g., Mn^{3+}/Mn^{4+}) when mixed valence is present. Values of $t \approx 1$ favor the ideal cubic perovskite, whereas $t < 1$ generally indicates increasing MnO_6 octahedral tilts and orthorhombic/rhombohedral distortions, which strongly impact the Mn–O–Mn bond angle and thereby the electronic bandwidth and transport behavior

[40, 71]. An increased fraction of Mn^{3+} ions introduces Jahn–Teller distortions, arising from the energy minimization of the system by structural or geometric distortion [40, 72, 78]. The Jahn–Teller effect hence drives deviations from cubic symmetry, resulting in elongated or compressed MnO_6 octahedra.

Characteristic for mixed-valence manganites is the coexistence of multiple manganese valence states, most commonly Mn^{3+} and Mn^{4+} [40, 79]. For example, in $Gd_{1-x}Ca_xMnO_3$, replacing trivalent gadolinium (Gd^{3+}) with divalent calcium (Ca^{2+}) leads to a change in the Mn oxidation state to preserve charge neutrality. In the ideal stoichiometric case, each Ca^{2+} substitution effectively converts one Mn^{3+} ion into Mn^{4+}, thereby controlling the Mn^{3+}/Mn^{4+} ratio. This means that the doping level x changes the Mn-valence ratio, which in turn directly influences the carrier concentration and alters the electrical conductivity [40]. Charge transport in manganites occurs largely through hopping between adjacent Mn ions mediated by oxygen. This process is called the double-exchange mechanism, in which an electron hops between Mn^{3+} and Mn^{4+} sites via hybridization with oxygen $2p$ orbitals [40, 79]. However, the strong coupling between electronic and lattice degrees of freedom leads to the formation of polarons, in which charge carriers locally distort the crystal lattice [40, 78]. As a result, conduction typically proceeds through thermally activated hopping rather than conventional band transport. This polaronic transport produces non-linear current-voltage behavior and makes the electrical conductivity highly sensitive to temperature, lattice strain, and defects.

Oxygen stoichiometry plays a central role in this system. Oxygen vacancies alter the Mn^{3+}/Mn^{4+} ratio by locally compensating charge imbalance, thereby modifying both carrier concentration and lattice distortion. Because bulk electronic transport in manganites depends on this valence balance, oxygen vacancy redistribution can significantly influence the local conductivity of the material. In resistive switching devices, however, the oxygen migration can also be associated with modification of interfacial regions. Oxygen ions and vacancies are mobile under an applied electric field and can redistribute within the lattice or accumulate near interfaces [10, 31, 80]. This redistribution modifies both the interfacial barrier structure and carrier injection, while also affecting the electronic transport in near-interface regions. This strong coupling between oxygen defect dynamics and electronic transport makes mixed-valence manganites particularly suitable for resistive switching applications [10, 40, 72].

2.2.2 $Gd_{1-x}Ca_xMnO_3$

$Gd_{1-x}Ca_xMnO_3$ is a mixed-valence perovskite manganite, in which the electrical transport is dictated by the competition between double-exchange interaction and Jahn–Teller distortions as discussed in Section 2.2.1 [40, 72, 78]. The calcium doping concentration x primarily controls the Mn^{3+}/Mn^{4+} ratio in the ideal stoichiomet-

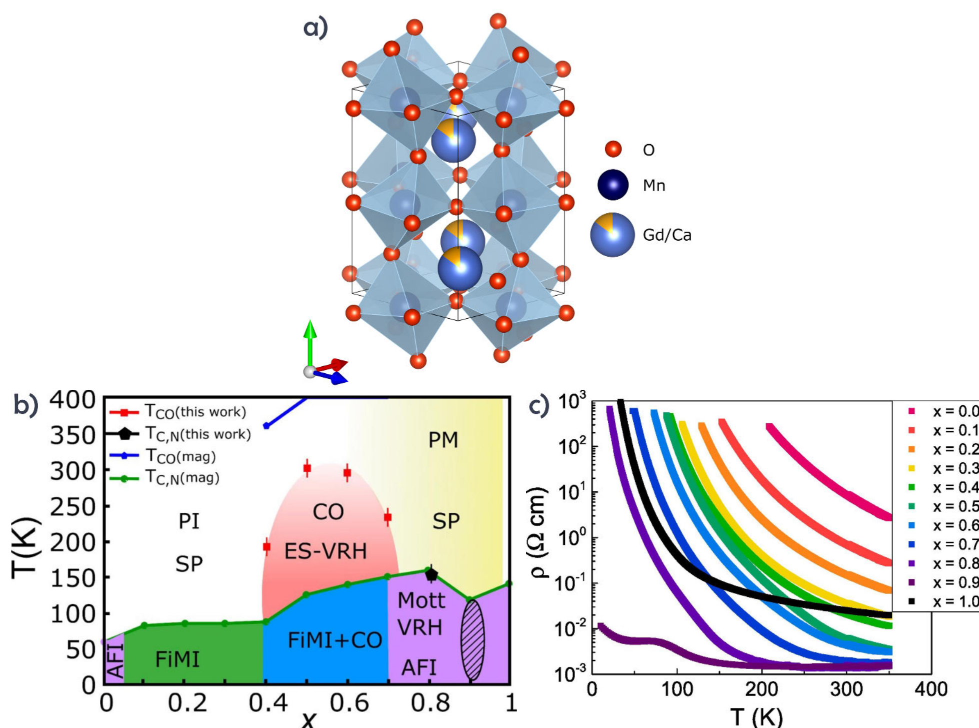

Figure 2. Structural and composition-dependent properties of $Gd_{1-x}Ca_xMnO_3$ thin films. (a) Orthorhombic perovskite crystal structure of $Gd_{1-x}Ca_xMnO_3$ visualized using VESTA. The structure consists of corner-sharing MnO_6 octahedra forming the perovskite framework, where Mn occupies the B-site, oxygen forms the octahedra, and the A-site is occupied by mixed Gd/Ca cations. The structure corresponds to the orthorhombic *Pnma* space group reported for $Ca_{0.85}Gd_{0.15}MnO_3$ [81]. (b) Revised magnetic and electronic phase diagram of $Gd_{1-x}Ca_xMnO_3$ thin films as a function of Ca concentration. Abbreviations: PI, paramagnetic insulator; PM, paramagnetic metal; FiMI, ferrimagnetic insulator; AFI, antiferromagnetic insulator; CO, charge order; SP, small-polaronic conduction; Mott-VRH, Mott variable-range hopping; ES-VRH, Efros–Shklovskii variable-range hopping; FMM, ferromagnetic metal. The crosshatched region denotes coexistence of the AFI phase and an arrested FMM phase. T_{CO} denotes the charge-ordering temperature, while $T_{\mathrm{C,N}}$ denotes the Curie or Néel transition temperature. (c) Temperature-dependent resistivity of $Gd_{1-x}Ca_xMnO_3$ thin films measured using a four-probe configuration, full Ca-doping range. Panels (b, c) are reprinted with permission from [48].

ric case and thereby modifies the electrical transport [40, 44]. Due to the small ionic radius of Gd^{3+}, the MnO_6 octahedra exhibit significant tilting (Fig. 2a), which narrows the electronic bandwidth and promotes carrier localization [40, 70, 76, 77]. As a result, Gd-based manganites possess lower bandwidth and are generally more insulating and defect-sensitive than their La- or Pr-based counterparts [40, 42, 70]. This enhanced defect sensitivity makes their transport properties particularly responsive to oxygen stoichiometry and interfacial modifications. The phase diagram and resistivity curves in Fig. 2b and c summarize the strong composition dependence of the GCMO thin-film system and motivate the choice of $x = 0.8$, which lies in the high-temperature paramagnetic region at room temperature and has relatively low resistivity within the studied range, supporting both interface-controlled resistive switching and lateral current transport in the devices of this thesis. The composition-dependent phase diagram shown in Fig. 2b and the related understanding of GCMO transport and resistive switching have been established largely through previous work by the same research group [43, 44, 48, 50].

At low Ca concentrations, strong Jahn–Teller distortions and carrier localization lead to highly insulating bulk behavior, and resistive switching is observed only at high voltage amplitudes [42–44]. With increasing Ca concentration, the effective resistivity of the oxide, particularly near the active interface, decreases towards a more conductive yet still thermally activated hopping regime [43, 44]. For compositions in the range $x = 0.7$–0.95, resistive switching characteristics are particularly enhanced. Within this compositional window, the P–F trap energy reaches a minimum of approximately $0.3\,\mathrm{eV}$ near $x = 0.8$, indicating relatively shallow traps [43]. Although P–F conduction in memristive devices typically arises from trap-assisted transport in defect-rich interfacial or near-interface regions rather than ideal bulk material, the bulk composition influences the trap landscape and oxygen-vacancy formation energy. The reduced trap depth enhances field-assisted carrier emission and promotes interfacial barrier modulation, coinciding with the highest observed resistive switching ratios. Accordingly, the specific composition $x = 0.8$ ($Gd_{0.2}Ca_{0.8}MnO_3$, hereafter GCMO) is utilized in this work. All experimental investigations presented in this thesis are performed on this composition.

Resistive switching in $Gd_{1-x}Ca_xMnO_3$ has been reported to follow the same interfacial redox principles observed in other mixed-valence manganites [42, 43]. To form the interface-type $Gd_{1-x}Ca_xMnO_3$-based memristor, the thin film must be combined with a highly oxidizable metal as the active electrode [43, 61, 62, 82]. The metal-manganite interface has a self-limiting redox reaction that occurs during deposition due to the difference in oxidation energies (Gibbs free energy of oxidation) [10, 29, 60]. When utilizing aluminum (Al) top electrodes, a thin (few-nanometer) native AlO_x layer forms spontaneously at the Al-manganite interface due to the high oxygen affinity of aluminum attracting the mobile oxygen in the perovskite lattice [61, 63, 64]. The migration of oxygen ions leaves behind a depletion region in

$Gd_{1-x}Ca_xMnO_3$, close to the metal-oxide interface [31, 80]. The interfacial oxide and close-to-interface depletion regions of the perovskite manganite act as the primary contributors behind resistive switching, separating the metallic electrode from the bulk of the manganite and introducing a redox-sensitive barrier [28, 62, 82]. The changes in the overall oxygen content of $Gd_{1-x}Ca_xMnO_3$ are expected to be small, with the dominant oxygen redistribution localized near the interface, as the increased interface resistance in comparison to the bulk resistance creates a lower electric field deep within the bulk [62, 64].

Under an applied electric field, oxygen vacancies (V_O), and correspondingly oxygen ions (O^{2-}), redistribute across the Al/(AlO_x)/$Gd_{1-x}Ca_xMnO_3$ interface, leading to reversible changes in the local stoichiometry of the interfacial oxide [10, 31, 80]. These electric field-driven processes result in alterations of the AlO_x layer, dynamically modifying its thickness and/or oxygen concentration and distribution [28]. Resistive switching in Al/$Gd_{1-x}Ca_xMnO_3$ devices is generally understood to originate from redox-driven modifications of the interfacial region, altering the effective Schottky-like barrier and the relative contributions of P–F and ohmic conduction, thereby controlling charge injection and the overall resistivity across the interface in an analog-like, gradual way [10, 28, 41, 43, 51]. Depending on the extent of redox modification, the device can exhibit both non-volatile and volatile switching behavior [42, 43, 50].

In the SET process, oxygen vacancy redistribution modifies the interfacial defect density and reduces the effective barrier width and resistive contribution of the oxide layer, enhancing P–F and quasi-ohmic conduction in the LRS [43, 53, 54, 82]. In the RESET process, oxygen redistribution re-oxidizes the interfacial region and widens the depletion region, increasing the effective series resistance and restoring a transport regime with a stronger Schottky-like contribution [43, 53, 56, 82]. Transitions between these regimes correspond directly to the reversible redox-driven evolution of the interfacial barrier [41–43].

2.3 Memristors and Neuromorphic Functionality

2.3.1 Synaptic Plasticity

Neuromorphic computing aims to replicate the primary functionalities of biological neural systems using electronic devices, with synaptic plasticity being one of the central requirements [8, 83, 84]. In biological synapses, the synaptic weight is continuously modified in response to neuronal activity through processes such as potentiation and depression. In neuromorphic memories, this concept is implemented by storing the synaptic weight as a non-volatile or semi-volatile device conductance, so that learning corresponds to electrically increasing or decreasing the conductance with voltage pulses. This plasticity can either be long-term or short-term (long-

term plasticity/potentiation (LTP) and short-term plasticity/potentiation (STP), respectively) [8, 85]. Depending on the retention of the conductance change, it can be implemented with either non-volatile or volatile memristors [85]. For neuromorphic memories, the relevant electrical analogue of synaptic plasticity is a gradually programmable device conductance: long-term plasticity can be represented by multiple retained conductance states, while short-term plasticity corresponds to transient conductance changes that relax with time.

In oxide-based resistive switching devices, gradual and multistate conductance changes arise from controlled redistribution of defects or ions, enabling the implementation of artificial synapses [10, 28, 41, 84]. Interface-type resistive switching, such as that of Al/GCMO devices, is particularly well suited for this purpose, as resistance modulation occurs through interfacial processes rather than abrupt filament formation [43, 50]. This can lead to improved endurance, reduced variability, and enhanced analog control, crucial for practical synapse-mimicking applications, as synaptic weights must be updated repeatedly and gradually without large cycle-to-cycle fluctuations or premature device failure [39, 86]. High variability and unpredictability may require external compensation circuitry, increasing the system complexity and power consumption. Some of the key considerations for practical devices are the linearity of the conductance change, the symmetry between potentiation and depression, and the achievable dynamic range between the high- and low-resistance states [39, 87].

The energies required to modify resistance states in memristive devices can be significantly lower than those of conventional CMOS-based memory and computing configurations, owing to their nanoscale active volume and efficient in-memory operation [17]. In neuromorphic circuits, this means that the synaptic weight is stored directly as the device conductance, and computation can be performed by applying voltage pulses to the same devices rather than transferring data between physically separated memory and processing units. Memristors can also support spike-timing-dependent plasticity (STDP), a biologically inspired learning rule suitable for spiking neural networks (SNNs) [50, 88]. Based on STDP, the values of these synapses are updated only in the case of the input pulses occurring at the correct timescale in relation to each other.

To utilize non-volatile memristors as synapses, the most common configuration is crossbar arrays, consisting of rows and columns of interconnected devices [15, 89]. This allows the imitation of a neural network in hardware. It can be considered a direct mapping of synaptic weights to device conductance/resistance, supporting in-memory matrix-vector multiplications, analog multiply-accumulate operations, and on-chip learning [17, 89]. Some issues in such structures that should be considered are the persistent sneak-path currents, the need for selectors, read/write disturbances, and IR-drop in larger arrays [90, 91].

2.3.2 Leaky-Integrate Neuronal Behavior

Beyond synaptic functionality, neuromorphic systems also require neuronal elements capable of temporal integration and threshold-based firing [8, 83]. This is especially important for temporal data processing in spiking neural networks, where information is carried by the timing and sequence of input spikes and the neuron must integrate these inputs over time while also generating an output spike only when the accumulated signal exceeds a threshold. In biological neurons, the membrane potential integrates incoming synaptic inputs and gradually decays in the absence of stimuli. While detailed neuron models, such as the Hodgkin–Huxley model [92], capture the full dynamics of ion channels and membrane potentials, reduced descriptions are often sufficient when considering temporal integration and leak processes. One such description is the leaky integrate-and-fire (LIF) model [93, 94], in which firing can be treated as a separate thresholding operation. Electronic counterparts of this behavior can be implemented using volatile memristors, since the leaky-integration component of neuronal activity corresponds to their intrinsic dynamics: pulse-induced conductance accumulation and spontaneous conductance relaxation after the stimulus is removed [95, 96]. In practical circuits, the firing event can be implemented using a CMOS comparator or thresholding element monitoring the memristor's conductance evolution [97].

Volatile switching modes occur when electrically induced resistance changes relax spontaneously, within a small time window, once the external stimulus is removed [30, 95]. In oxide-based memristors, such temporary resistivity change is often associated with transient redox states, metastable defect configurations, or thermally activated back-diffusion of oxygen ions [31, 80]. This intrinsic relaxation introduces a natural leakage term, enabling temporal integration of input pulses followed by decay towards a high-resistance state [96]. This relaxation acts as the leakage term in the LIF model, causing the effective membrane potential to decay in the absence of input. One of the advantages of volatile memristors is that their relaxation timescale can be tuned by changing the pulsing sequence, material composition, or device geometry [98, 99]. As in synaptic applications, the neuronal behavior is highly energy efficient due to the pulsing-induced behavioral changes [17].

In Al/GCMO devices, the coexistence of volatile and non-volatile switching regimes could enable the emulation of both synaptic and neuronal-like dynamics within the same material system [43, 50]. By appropriately engineering the material stack and selecting pulse amplitude, duration, and repetition rate, the device response could be mapped onto LIF neuron models, where conductance accumulation corresponds to membrane potential integration and resistance relaxation represents leakage [50, 51]. This dual synaptic-neuronal functionality could strengthen the potential of interface-type manganite devices for compact and energy-efficient neuromorphic circuits and processors [28, 83].

3 Experimental Methods

3.1 Thin Film and Device Fabrication

3.1.1 Pulsed Laser Deposition

Pulsed laser deposition (PLD) is used to grow the GCMO thin films, which serve as the functional oxide layer of the memristive devices studied in this work. PLD enables the deposition of complex oxide thin films with controlled stoichiometry, composition, and film thickness, all of which are crucial variables for oxide-based memristive devices. Compared to alternate oxide deposition techniques, such as sputtering or chemical vapor deposition, PLD offers improved control over crystalline quality and defect density [100, 101].

In PLD, a pulsed, high-energy excimer laser beam is directed and focused on a rotating ceramic target of the deposited oxide material. Each pulse ablates a small amount of the material, forming a plasma plume that expands towards a laser-heated substrate in a controlled oxygen atmosphere and pressure. The ablated species condense on the substrate surface to form a thin film with a cationic composition closely matching that of the target, while the oxygen stoichiometry is governed by other process parameters, such as the oxygen background pressure, substrate temperature, and post-deposition cooling conditions. To improve the epitaxial quality of the deposited film, an annealing treatment is carried out under elevated oxygen partial pressure and increased temperature, after which the system is allowed to cool down to room temperature. The substrate will have a homogeneous layer of the deposited material, and the crystallinity of the film will depend on substrate and fabrication parameters [III, IV][100, 102]. A schematic figure of the PLD system is presented in Fig. 3. In this work, a COHERENT COMPex KrF excimer laser ($\lambda = 248$ nm) and a COHERENT Compact Evolution heating laser are used.

The ceramic GCMO targets are prepared by the solid-state reaction method as follows [102]: Gd_2O_3 oxide is calcined for 12 hours in air at $1300\,^{\circ}$C, whilst $CaCO_3$ and MnO_2 are dried at $200\,^{\circ}$C. Depending on the intended GCMO composition, suitable stoichiometric amounts are ground finely and pressed into a pellet to be calcined for 60 hours in air at $750\,^{\circ}$C. The pellet is ground finely again, and 24-hour sintering in air at $1300\,^{\circ}$C is carried out. The described grinding–sintering process is repeated twice to ensure the stoichiometry and phase purity of the resulting ceramic target.

Controlling the process parameters, such as the excimer laser fluence and pulse

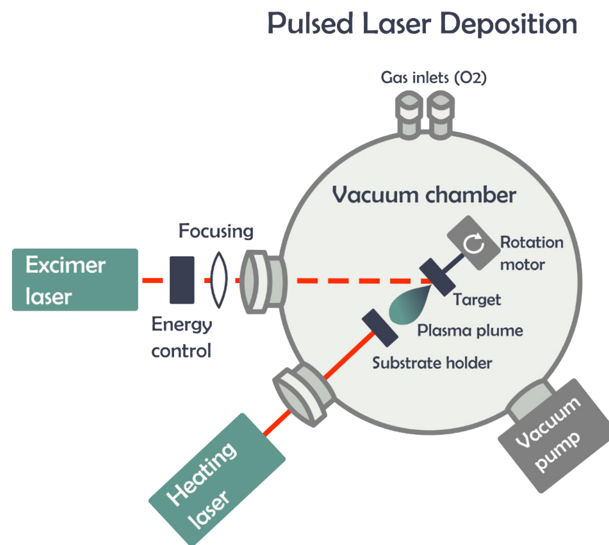

Figure 3. Pulsed laser deposition (PLD) schematic. An excimer laser delivers short laser pulses that are focused by external optics and directed through an optical window into the vacuum chamber. The laser beam ablates material from a solid target mounted on a rotating holder, producing a plasma plume composed of energetic species. The plume expands towards a heated substrate holder, where the material condenses to form a thin film on the substrate surface. Oxygen (O_2) inlets control the chamber atmosphere and deposition pressure, while a vacuum pump maintains the required base pressure and operating pressure.

frequency, substrate material and temperature, deposition chamber atmosphere, and possible annealing treatments, enables high-quality growth of many perovskite oxide thin films. In this work, the excimer laser fluence, or energy density, is kept around 1.0–2.0 J/cm^2 and the repetition rate at 5 Hz. The target-substrate distance is fixed at 35 mm and kept constant for all depositions. A typical deposition uses around 1500 pulses, yielding a GCMO film thickness of approximately 60–80 nm, depending on laser energy and deposition conditions. For optimal GCMO crystallinity and epitaxial growth, the deposition temperature of $700\,^{\circ}$C is used, while the oxygen partial pressure is kept steady at 0.1 Torr. The same temperature also acts as the annealing temperature, while the oxygen flow is increased to atmospheric pressure. These parameters follow the optimized conditions established in previous works [102].

PLD enables the growth of highly uniform GCMO thin films with precise thickness control and low surface roughness, while also allowing careful control of the microstructure and defect density of the resulting films [45, 100, 102]. Because the deposited oxide layer directly influences charge transport, defect states, and resistive switching behavior, careful control of deposition parameters is essential [10, 29, 103]. The resulting film quality and the structural, compositional, and chemical properties are examined using techniques such as X-ray diffractometry (XRD), X-ray reflectivity (XRR), atomic force microscopy (AFM), and scanning electron microscopy (SEM) as required.

3.1.2 Substrates and Buffer Layers

The GCMO thin film forms the active memristive layer in the fabricated lateral devices. In the device geometries utilized in this work, the film is grown directly on the selected substrate without a continuous metallic bottom electrode, making the substrate choice directly relevant to the structural and electronic quality of the resulting devices [III, IV]. By selecting specific substrates and buffer layers, the crystallinity of manganite thin films can be tuned across a broad range, from highly ordered epitaxial films to polycrystalline or poorly ordered structures [101, 104].

For highly oriented, single-crystalline, epitaxial growth aligned with the substrate surface, the substrate lattice parameters should closely match those of the manganite, as lattice mismatch introduces strain [104–107]. As the mismatch increases, defect formation, such as dislocations, becomes more likely [106, 108]. If the mismatch becomes sufficiently large or if the substrate surface itself is non-crystalline, long-range epitaxial ordering cannot be maintained and the film may grow in a polycrystalline or poorly ordered form [101, 104]. Such structural defects and grain boundaries can influence electronic transport and defect migration processes in oxide materials [109, 110]. The substrate must also withstand the high temperatures and oxygen pressures required during PLD growth and post-annealing [100].

Common substrates suitable for epitaxial manganite growth include, for exam-

Table 1. Structural parameters of GCMO and the selected substrates used for thin-film growth. For perovskite substrates (STO, LAO, NGO), GCMO typically grows with a $45°$ in-plane rotation relative to the substrate lattice, giving an effective in-plane lattice parameter shown in parentheses. For Si/SiO_2, the listed lattice parameter refers to crystalline Si, while the actual growth surface contains native amorphous SiO_2, so no well-defined epitaxial lattice mismatch is assigned. Reference for GCMO ($x = 0.8$) from [44]. ICSD references: GCMO ($x = 0.85$) (12626) [81]; STO (262269) [111]; LAO (170772) [112]; NGO (76050) [113]; MgO (52026) [114]; Si (197680) [115].

Material	Structure	a ($\sqrt{2}a$) (Å)	b (Å)	c (Å)	Notes
GCMO ($x = 0.8$)	Orthorhombic	5.296	5.336	7.489	Reference lattice.
GCMO ($x = 0.85$)	Orthorhombic	5.281	5.300	7.460	ICSD reference.
$SrTiO_3$ (STO)	Cubic	3.905 (5.523)	3.905	3.905	Small mismatch.
$LaAlO_3$ (LAO)	Cubic	3.791 (5.361)	3.791	3.791	Small mismatch.
$NdGaO_3$ (NGO)	Cubic	3.851 (5.446)	3.851	3.851	Small mismatch.
MgO	Cubic	4.214 (5.959)	4.214	4.214	Large mismatch.
Si/SiO_2	Cubic Si + amorphous SiO_2	5.430	5.430	5.430	Si lattice shown; amorphous surface, no defined epitaxial mismatch.

ple, single-crystalline $SrTiO_3$ (STO, (100)) and $LaAlO_3$ (LAO) substrates [104, 105]. Both materials share the perovskite structure and offer close in-plane lattice matching, compatible thermal expansion coefficients, and well-defined crystallographic orientations. These factors promote high-quality epitaxial manganite films with low defect density [104, 107]. STO, in particular, is widely used as a perovskite platform due to its cubic lattice and excellent structural compatibility with manganites [105, 106].

In addition to lattice-matched perovskite substrates, materials with larger lattice mismatch, such as MgO, can also be used when polycrystalline growth is acceptable or desired. Furthermore, buffer layers may be introduced between the substrate and the active film in order to modify the interfacial lattice mismatch and promote specific crystalline ordering of the deposited oxide layer [101]. For example, perovskite buffer layers can be deposited on Si substrates to enable the integration of complex oxide thin films on otherwise non-epitaxial surfaces. Nevertheless, amorphous or poorly crystalline oxide films can still exhibit resistive switching behavior [10, 29].

In this work, several substrates with varied lattice mismatch and structural properties are employed to investigate how the structural quality of GCMO thin films influences the resistive switching behavior of the devices [III, IV]. Relevant structural parameters of GCMO and the substrates used for thin-film growth are summarized in Table 1. As discussed in Sections 2.2.1 and 2.2.2, the resulting structural distortions, such as changes in octahedral tilting and defect formation, directly influence the electronic transport and therefore the resistive switching characteristics of the devices.

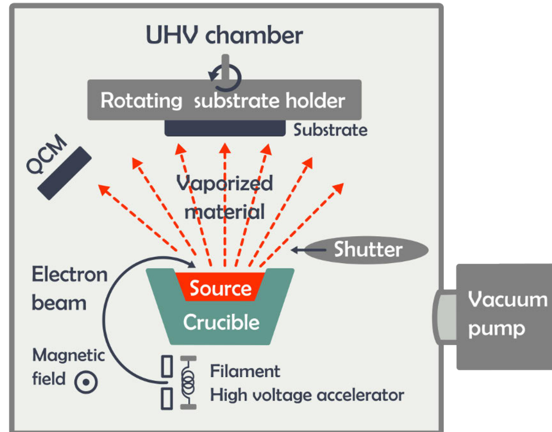

Figure 4. Schematic of an electron beam physical vapor deposition (EBPVD) system. A focused high-energy electron beam is generated, accelerated and directed onto a solid source material placed in a water-cooled crucible inside a high-vacuum chamber. The electron beam locally heats and evaporates the target material, producing a vapor flux directed towards the substrate. The evaporated species condense onto the substrate surface, forming a thin film. The deposition rate is controlled by the electron beam power and monitored using a quartz crystal microbalance (QCM), while a vacuum pumping system maintains the low base pressure required for stable evaporation and high-purity film growth.

3.1.3 Electron Beam Physical Vapor Deposition

Electron beam physical vapor deposition (EBPVD) is one of the fundamental fabrication techniques when creating the MIM-stacks commonly used in memristor research [10, 60, 101]. It is widely employed due to its ability to deposit both metallic and oxide thin films with high purity, thus covering the needs of fabrication for all electrodes and active switching layers. As a physical vapor deposition method, EBPVD operates under high-vacuum (HV) or ultra-high-vacuum (UHV) conditions, minimizing unwanted oxidation and impurity incorporation. When depositing oxide materials, a controlled oxygen partial pressure can be used to tune the thin-film stoichiometry [101].

When an electric current is passed through a tungsten filament, the filament heats up, causing thermionic emission of electrons [101]. These electrons are accelerated by a high voltage and directed and focused with a magnetic field (electromagnetic lens) onto a solid source material placed in a water-cooled and grounded crucible. The localized heating from the electron beam melts and evaporates this material, generating a vapor flux that travels through the vacuum chamber towards the rotating substrate. As the vaporized material reaches the substrate, the vapor condenses and forms a thin film. A substrate-covering shutter and a quartz crystal monitor (QCM) allow precise control of the deposition rate and total film thickness. The required

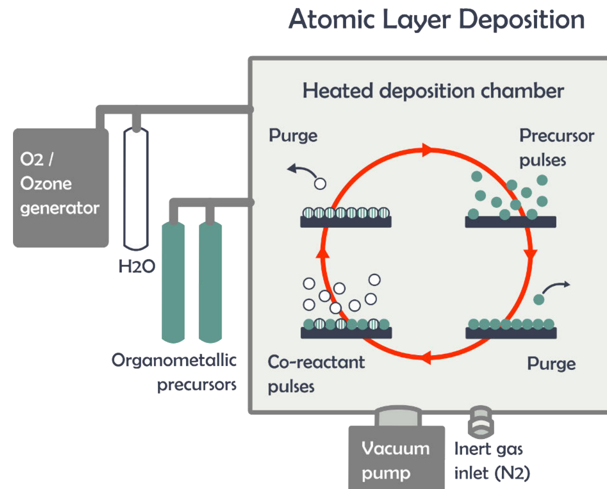

Figure 5. Atomic layer deposition (ALD) schematic. The process is carried out in a heated reaction chamber where the substrate is placed on a sample tray. Thin films are grown through sequential, self-limiting surface reactions by alternately pulsing gaseous precursors into the vacuum-controlled chamber. Typical precursors include metal-organic compounds and oxidants such as H_2O, O_3, or O_2. Each precursor pulse is followed by a purge step using an inert carrier gas (N_2) to remove excess reactants and reaction by-products. Film growth proceeds by approximately one monolayer per cycle, enabling precise control over thickness, composition, and uniformity. Chamber pressure and gas flow are regulated by vacuum pumping and gas handling systems throughout the deposition cycle.

filament current and acceleration voltage depend on the evaporation material, while continuous pumping maintains the low base pressure necessary for stable evaporation. A schematic of the EBPVD system is shown in Fig. 4. The system used in this work consists of an Elettrorava electron beam evaporator with a high-voltage power (HVP) supply and an INFICON XTC/3 thin-film deposition controller.

In this work, EBPVD is used to deposit the metallic electrodes on top of the GCMO thin films. The active electrode material, Al, is deposited with an acceleration voltage of $10\,\mathrm{kV}$, a deposition rate of 2 Å/s, a filament current of approximately 30–$40\,\mathrm{mA}$, and a base pressure on the order of 10^{-7} mbar. For Au electrodes, the parameters are $8\,\mathrm{kV}$, 1 Å/s, 40–$50\,\mathrm{mA}$, and a base pressure on the order of 10^{-6} mbar, respectively. Ensuring the purity and quality of the electrodes in interface-type memristors is crucial, especially in the case of the active electrode Al, as the resistive switching mechanism in GCMO devices is governed by interfacial redox processes at the Al/GCMO interface [10, 29, 43].

3.1.4 Atomic Layer Deposition

Atomic layer deposition (ALD) enables the fabrication of thin films with ultra-precise thickness control due to its layer-by-layer nature [101, 116]. In memristive devices,

the fabrication of the material layers can be especially crucial as the electrical characteristics, such as leakage, switching, and active area control, are highly dependent on the material uniformity and thickness [10, 29, 103]. In addition to precise thickness control, ALD also provides excellent conformality due to the sequential, self-limiting surface reaction-based process [116]. The method is often used for the oxide layer within the memristor stack, but it can also be used for adding buffering insulating layers to control the active area size and limit leakage paths with an engineered device structure.

The chemical reactions in ALD occur as a sequential process in a controlled vacuum environment [116]. One cycle of such a process starts with introducing a gaseous precursor into the deposition chamber, where the gas will chemically react with the substrate surface with atomic-scale uniformity until all reactive sites are covered (chemisorption to all available reactive sites). The reaction byproducts and excess precursor are then removed by purging the chamber with inert gas such as N_2. The introduction of the second precursor, or a co-reactant, continues the building by reacting with the chemisorbed species to complete the formation of a monolayer. The cycle is completed by another purge, where the excess gases and byproducts are removed, after which the cycle can repeat. Typical ALD processes for the deposition of oxides use precursors that are organometallic, in combination with H_2O vapor, O_2, or O_3 as co-reactants. The system is usually kept in a vacuum or with a slight inert gas pressure during operation. The substrate, chamber, and precursor temperatures must be carefully controlled to ensure surface-limited reactions and avoid unwanted decomposition. A schematic of the ALD process is shown in Fig. 5.

In this work, the active GCMO layer is deposited using PLD, while ALD is selectively employed to introduce an additional insulating buffer layer that defines the device geometry and controls the electrode-oxide interface. To miniaturize the active memristive area, a thicker insulating oxide can be deposited and patterned to form controlled-size vias. For this purpose, Al_2O_3 is deposited with ALD to a thickness of approximately 30 nm using an Anric ALD system (AT-410) with trimethylaluminum ($Al(CH_3)_3$, TMA) and H_2O as precursors. Typical deposition parameters include a deposition temperature of 150°C, 3 TMA pulses with 11 s purge time, 2 H_2O pulses with 13 s purge time, and a chamber base pressure of 200 mTorr under continuous N_2 flow. These conditions yield a growth rate of approximately 1.1 Å per cycle.

In addition to acting as an insulating layer, ultra-thin ALD-grown Al_2O_3 (1–10 nm) can be used as a buffer or stabilizing layer between the GCMO film and the active Al electrode. Such a layer can help to control the formation and uniformity of the naturally occurring interfacial oxide, improving device reproducibility and stabilizing the redox-active interface responsible for resistive switching [117].

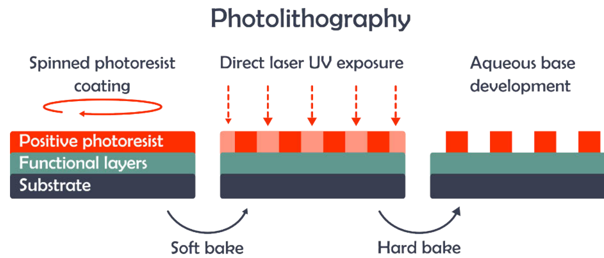

Figure 6. Schematic illustration of basic photolithography. A photoresist layer is spin-coated onto the substrate and soft-baked, after which the resist is exposed using a focused laser beam in a direct laser writing system. After a second baking step, exposed resist is developed in an aqueous alkaline solution, selectively removing regions depending on the exposure pattern and leaving a patterned photoresist layer on the substrate.

3.1.5 Patterning: Lithography, Lift-off, Ion Milling, Reactive Ion Etching, Wet Chemical Etching, Wire Bonding

The fabrication of functional memristive devices requires not only thin-film deposition but also precise patterning to define device geometries, electrode layouts, and active regions [101]. Several patterning approaches are introduced in this work, including photolithography, lift-off, ion milling, reactive ion etching (RIE), and wet chemical etching. All of these techniques rely on either hard shadow masks or lithographically patterned photoresist to stencil the desired device structures.

Photolithography Photolithography is the primary patterning method used in this work due to its high resolution and reproducibility [101]. The process begins by spin-coating a broadband positive photoresist (MEGAPOSIT SPR 220-3.0) onto the substrate, followed by a soft bake (90 s at 120°C). The resist is exposed to ultraviolet (UV) light either through a photomask, by direct UV laser exposure (in this work, Dilase 125 by KLOE), or by electron-beam-assisted exposure. UV illumination induces chemical changes in the resist that modify its solubility. After the exposure, a hard bake or post-exposure bake (90 s at 120°C) can be carried out to fully stabilize the resist coating before the development with an aqueous base developer (e.g., MF-24A). The resulting resist pattern can act as a stencil for the subsequent additive (lift-off) or subtractive (etching) processes. The fabrication steps for photolithography are collected in Fig. 6. Separate hard shadow masks may also be used during thin-film deposition to physically define the deposited pattern, but their resolution is limited by the mechanical constraints of mask fabrication and alignment.

Subtractive Patterning: Etching The defined resist mask can be combined with subtractive etching techniques such as argon ion milling, reactive ion etching, or wet chemical etching to replicate the resist pattern onto the underlying thin film [101].

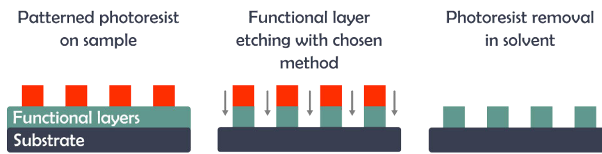

Figure 7. Schematic illustration of pattern transfer by etching after photolithography. After patterning of the photoresist, the exposed regions of the underlying layer are selectively removed using one of several etching techniques: ion milling, reactive ion etching, or wet chemical etching. In all cases, the photoresist acts as an etch mask, and removal of the remaining resist after etching leaves the patterned thin film on the substrate.

The basic principles of the etching process are illustrated in Fig. 7.

Physical etching can be achieved with argon ion milling, which can be thought of as chipping away the material on an atomic level by bombarding the surface with inert Ar^+ ions [101]. It is particularly useful for materials that lack suitable chemical etchants, such as noble metals (Au, Pt). However, ion milling is non-selective and can cause re-deposition of sputtered material onto feature sidewalls, reducing pattern quality.

Reactive ion etching (RIE) achieves selectivity by employing a chemically reactive plasma [101]. The plasma made of the reactive gas is accelerated towards the substrate surface to carry out the etching. By selecting reactive ions (e.g., precursor containing CF_4 or Cl_2) that form volatile compounds with the target material, the etching is highly selective with well-defined side-walls. Because of its selectivity and anisotropy, RIE is preferred when fine device features or multilayer stacks must be patterned without damaging adjacent layers.

Wet chemical etching also relies on chemical reactions with the etched thin film, but now with a liquid etchant [101]. Although inexpensive, fast, and highly selective, wet etching is typically isotropic, leading to undercutting beneath the resist mask and less precise feature definition. For GCMO, a selective aqueous etchant has been developed based on chloride chemistry [VI]:

$$[\mathrm{HCl}] = 0.12\,\mathrm{M}, \quad [\mathrm{KI}] = 5\,\mathrm{M}, \quad [\mathrm{Ascorbic\,acid}] = 0.1\,\mathrm{M}.$$

The etchant reduces Mn to water-soluble Mn^{2+}, while the iodide/ascorbic-acid chemistry controls the redox conditions and stabilizes the solution [VI]. The etchant is highly selective due to the chemical reactions being towards the manganese within the GCMO structure, thus sparing the substrate, the electrodes, and other deposited layers.

Additive Patterning: Lift-Off The same patterned resist can also be utilized in additive patterning, as in the lift-off process for metal electrodes [101]. After the de-

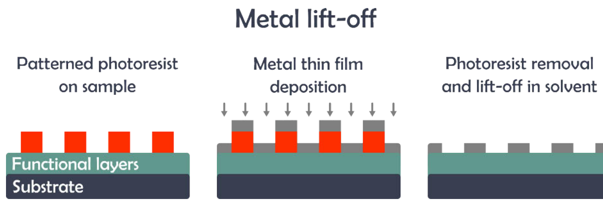

Figure 8. Schematic illustration of the lift-off process. Following patterning of the photoresist, a metal layer is deposited over the entire sample surface by electron beam physical vapor deposition (EBPVD). The sample is subsequently immersed in a solvent to dissolve the underlying photoresist, removing the metal deposited on top of the resist and leaving the patterned metal features on the substrate.

posited material covers the entire substrate, the resist is removed with a solvent. This simultaneously lifts off the excess material resting on the resist, leaving behind only the metal in the originally patterned areas. The patterning steps related to the lift-off process can be seen in a schematic Fig. 8. One known issue in lift-off patterning is the remnant ”ears” at the electrode edges, but the method is otherwise extremely gentle on the pre-existing material stack.

Electrical Interfacing: Wire Bonding and Probing After the completed patterning, the finalized chip must be electrically connected for the subsequent electrical characterization. Most device layouts require one bond per electrode. In this work, ultrasonic wire bonding is used to attach 33 µm Al wire (HB05, TPT) to the electrode pads, enabling mounting onto standard chip carriers used in measurement systems. For rapid prototyping or testing, electrical contact can also be made using probe needles in a probe station, which allows direct access to device electrodes without permanent bonding.

3.2 Thin Film Characterization

3.2.1 X-ray Diffractometry

When determining the quality of thin films, one of the most important techniques is X-ray diffractometry (XRD), as it can provide non-destructive access to information on the crystal structure, lattice constants, strains, phase purity, and crystallinity/epitaxial quality [118]. These structural characteristics influence the memristive behavior of oxide thin films, making XRD an important diagnostic tool even before device fabrication begins [10, 29, 103]. Complementary to XRD, X-ray reflectivity (XRR) provides information on film thickness, density, and interfacial roughness [118, 119].

XRD allows identification of whether the switching layer is epitaxial, polycrystalline, or amorphous, each of which can influence the resistive switching charac-

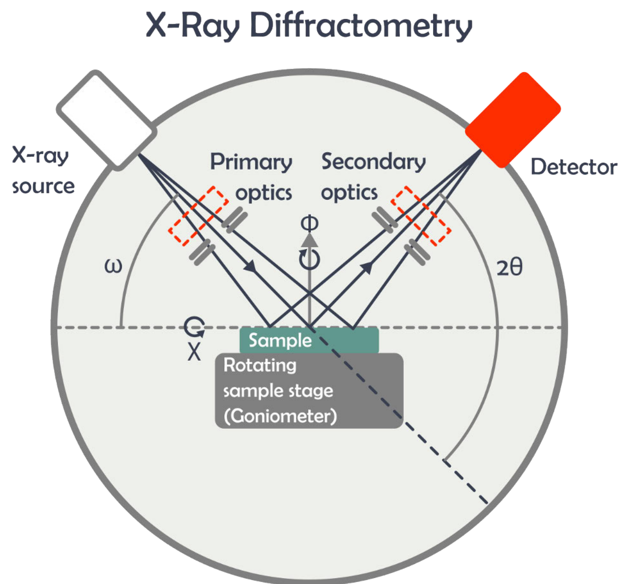

Figure 9. X-ray diffractometry (XRD) measurement geometry schematic. A monochromatic X-ray beam generated by an X-ray source is conditioned by incident-beam optics and directed onto the sample at an incident angle ω. The beam is diffracted by periodic lattice planes in the crystal, and the diffracted intensity is recorded by a detector as a function of the diffraction angle (2θ). Additional rotational degrees of freedom of the sample stage include azimuthal rotation (Φ) and tilt (χ), together with translational positioning (x, y, z), enabling comprehensive structural characterization. Receiving optics on the detector side improves angular resolution and signal quality. The measurement provides information on crystal structure, phase composition, lattice parameters, and crystallographic orientation of the thin film.

teristics of oxide memristors. In thin films, analysis of diffraction peak widths can provide information on crystallite size and microstrain within the lattice [118]. Texture analysis can further reveal the preferred crystallographic orientation of polycrystalline films. Grain boundaries and dislocations can act as preferential pathways for oxygen vacancy migration, influencing switching uniformity, state volatility, and endurance [109, 110]. Even in the case of epitaxial growth, the mismatch of lattice parameters between the thin film and substrate can introduce strain. XRD measurements can quantify uniform strain through shifts in diffraction peak positions relative to the bulk lattice parameters. Such strain reflects the degree of lattice stretching or compressing due to the film growth accommodating the mismatch, and can significantly change the electrical transport [105, 106, 118].

XRR is effective for determining film thicknesses in the nanometer range (1–$100\,\text{nm}$), depending on the instrumental sensitivity [118]. While it uses the same measurement setup as XRD, it operates at shallow incident and reflected angles where X-rays undergo specular reflection from the film and substrate interfaces rather than diffraction from lattice planes. This produces interference oscillations, known as Kiessig fringes, whose periodicity allows the film thickness to be determined. The critical angle of total external reflection and the fringe amplitudes further provide information on the electron density of the film, which can be related to the mass density of the material and may reveal porosity that can lead to leakage or unstable switching [118, 119]. Interfacial roughness, also accessible through XRR, is another key parameter, as rough interfaces increase the likelihood of short-circuiting and device-to-device variability.

Most modern diffractometers, including the PanAnalytical Empyrean system used in this work, employ a five-axis goniometer. The sample sits in the middle of this goniometer circle; ω describes the angle between the sample surface and the incident beam, relevant in rocking-curve measurements. To describe the angle of the detector, θ or 2θ is used in standard Bragg–Brentano scans, governed by Bragg's law:

$$n\lambda = 2d \sin\theta. \tag{3}$$

With knowledge of the used X-ray wavelength λ, the diffraction order n, and the measured diffraction angle 2θ, the lattice spacing d can be calculated. The XRD setup also allows in-plane rotation of the sample around the surface normal, denoted Φ. This rotation is commonly used in pole-figure measurements to determine the crystallographic texture of the film. The tilt angle χ describes tilting of the sample away from the surface normal and is used together with Φ in texture analysis. In addition, the diffractometer includes translation stages allowing positioning of the sample along the x, y and z directions. These different degrees of freedom are illustrated in Fig. 9.

The Empyrean diffractometer is equipped with a Cu LFF HR (long fine focus, high resolution) X-ray tube, operating voltage $40\,\text{kV}$ and current $45\,\text{mA}$. The effec-

Table 2. Representative optical configuration parameters of the PanAnalytical Empyrean X-ray diffractometer used for thin-film measurements in Bragg–Brentano geometry.

Component	Purpose	Value
Divergence slit	Incident beam width	$1/4°$ or $1°$
Mask	Beam width on sample	4–10 mm
Incident Soller slit	Axial divergence	0.02–0.04 rad
Anti-scatter slit	Background reduction	7.5 mm
Diffracted Soller slit	Axial divergence (detector side)	0.04 rad

tive incident beam is dominated by Cu $K_{\alpha1}$ and $K_{\alpha2}$ radiation ($\lambda_{K\alpha1} = 1.54056$ Å, $\lambda_{K\alpha2} = 1.54439$ Å; combined Cu K_{α} $\lambda \approx 1.5418$ Å), as the system employs a Bragg–Brentano HD (high definition) mirror that conditions the incident beam and reduces bremsstrahlung background contributions. Residual Cu K_{β} radiation ($\lambda = 1.39222$ Å) is further suppressed by the detector energy discrimination and optical configuration. In addition, weak parasitic lines such as W L_{α} radiation ($\lambda \approx 1.4815$ Å), originating from tube components or surrounding optics, may appear in the diffraction pattern.

The primary and secondary optics include masks and slits that shape the beam, control divergence, and limit unwanted background scattering. The standard detector (PiXcel solid-state detector) can be complemented with additional detectors optimized for specialized measurements such as grazing-incidence diffraction or reflectivity. The overall measurement geometry is illustrated in Fig. 9, while the optical configuration used in this work is summarized in Table 2.

3.2.2 X-ray Photoelectron Spectroscopy

In memristor research, especially in the layered structures of material stacks, analyzing the chemical composition and oxidation states within thin-film memristor stacks is important, and X-ray photoelectron spectroscopy (XPS) is ideally suited to meet these requirements [120–122]. Resistive switching often involves redox reactions, oxygen vacancy redistribution, or interfacial chemical modification, all of which can be detected through changes in the binding energies of core-level electrons. XPS is therefore essential for identifying how the active electrode and oxide layer interact during memristor operation. The working principle behind XPS is the photoelectric effect, in which irradiation with X-rays causes the emission of electrons from the material. Every element has characteristic electron binding energies, which can be determined from the measured kinetic energies of photoelectrons emitted using the photoelectron relation:

$$E_B = h\nu - E_K - \phi, \tag{4}$$

where E_B is the binding energy, $h\nu$ the photon energy, E_K the measured kinetic energy, and ϕ the spectrometer work function [120].

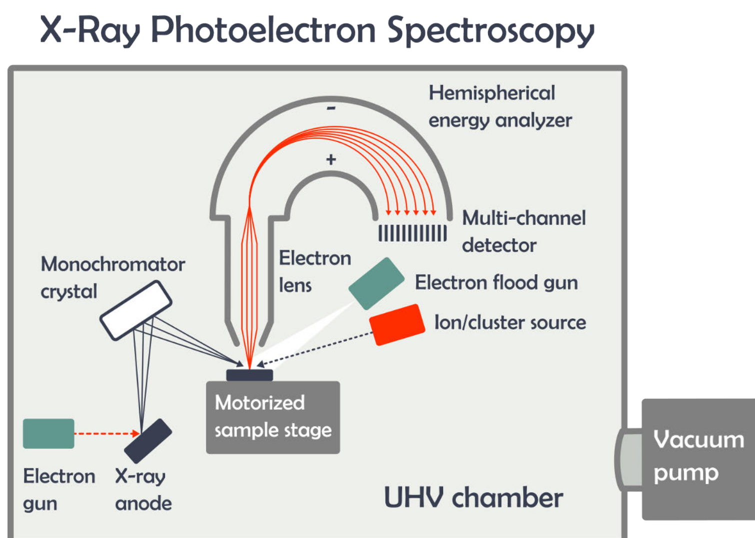

Figure 10. Schematic illustration of an X-ray photoelectron spectroscopy (XPS) system. The setup consists of an X-ray anode and monochromator crystal that generate and monochromatize the incident X-ray beam, which is directed onto the sample mounted on a motorized stage inside an ultra-high-vacuum (UHV) chamber. Photoelectrons emitted from the sample surface are collected and focused by electron lenses into a hemispherical energy analyzer and detected by a multichannel detector. An electron flood gun can be used for charge compensation during measurement, while an ion/cluster source enables surface cleaning or depth profiling. The chamber vacuum is maintained by a vacuum pumping system. XPS provides surface-sensitive information on elemental composition, chemical states, and surface chemistry.

XPS measurements are performed under UHV to minimize scattering of photoelectrons and to maintain surface cleanliness [120, 122, 123]. In the system used in this work (Thermo Scientific Nexsa), X-rays are generated by an Al (Kα, 1486.7 eV) X-ray source, in which an electron gun fires high-energy electrons towards a metal anode, causing it to emit X-rays. These X-rays are filtered with a monochromator crystal and directed to the sample surface. Because many oxide films are insulating, an electron flood gun supplies low-energy electrons to neutralize surface charging caused by photoelectron emission. The emitted electrons are collected and focused using an electrostatic lens system and analyzed by a hemispherical energy analyzer. The voltage difference between the hemispheres separates the electrons according to kinetic energy, and the multichannel detector records the resulting spectrum. This enables identification of elemental species and their chemical states with high surface sensitivity, typically 1–10 nm, depending on electron kinetic energy (smaller kinetic energy corresponding to higher surface sensitivity).

As most interesting phenomena happen within the material stack at the interfaces, an ion or cluster source (MAGCIS dual-mode ion and cluster source) can remove material layer-by-layer, revealing the changes as a function of sputtering time. Monoatomic Ar^{+} ions are sometimes too aggressive and might alter the oxidation state of the atoms, so a cluster of ions can provide a softer etching of the surface layers. Depth-resolved XPS enables reconstruction of chemical profiles across the device stack and reveals interfacial redox processes. A schematic of the X-ray photoelectron spectroscope is displayed in Fig. 10.

XPS spectra allow quantitative determination of oxidation states by analyzing the positions and integrated areas of core-level peaks [120, 122]. This enables the detection of the interfacial changes between the active switching layer and the active electrode, and it is particularly important for manganite-based memristors, where the Mn^{3+}/Mn^{4+} ratio and interfacial oxidation directly influence electronic transport and switching behavior [54, 124, 125]. Peak fitting in this work is performed using CasaXPS (version 2.3.25PR1.0), with Gaussian–Lorentzian product pseudo-Voigt line shapes GL(m), where the mixing parameter m controls the Lorentzian contribution.

3.2.3 Scanning Electron Microscopy and Energy-Dispersive X-ray Spectroscopy

Scanning electron microscopy (SEM) can be used both for evaluating the initial thin film quality and for inspecting fully patterned memristor devices [101, 121, 126]. SEM provides nanoscale information on film morphology, grain structure, surface roughness, and pattern quality [126]. When combined with energy-dispersive X-ray spectroscopy (EDS), SEM additionally enables spatially resolved elemental and compositional mapping across thin films, interfaces, and device structures [126].

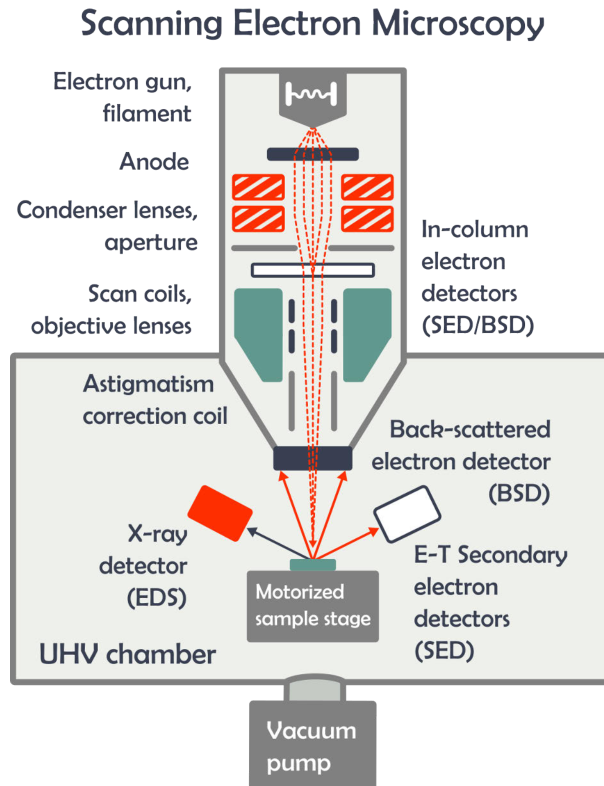

Figure 11. Schematic illustration of a field-emission scanning electron microscope (FE-SEM) equipped with energy-dispersive X-ray spectroscopy (EDS). The instrument operates in an ultra-high-vacuum (UHV) chamber maintained by a vacuum pumping system. A focused electron beam is generated by a field-emission electron gun consisting of a filament and anode, and is shaped by condenser lenses, apertures, scan coils, stigmation correction coils, and objective lenses before interacting with the sample mounted on a motorized stage. Signals produced by beam–sample interactions include secondary electrons (SE), backscattered electrons (BSE), and characteristic X-rays. These are detected using in-column and Everhart–Thornley (E–T) secondary electron detectors (SED), backscattered electron detectors (BSD), and an X-ray detector for EDS analysis. SE and BSE imaging provide high-resolution surface and compositional contrast, while EDS enables elemental analysis and chemical mapping.

The imaging power of SEM is based on the electron–matter interactions when an electron beam is focused on a sample surface. Topographical information is provided by secondary electrons (SE), which are generated by inelastic scattering near the surface. Compositional contrast can be examined with backscattered electrons (BSE), as the elastic scattering of the primary beam varies depending on the atomic weight of the material. This dual contrast provides essential information on surface quality, grain morphology, and the fidelity of lithographically patterned features [126].

In EDS, the focus is on the characteristic X-ray emission arising from electron relaxation. When the primary electron beam ionizes inner-shell electrons, atoms relax by emitting X-rays with element-specific energies. Detecting and analyzing these X-rays allows identification of elemental composition and spatial distribution [126]. This is particularly useful for verifying the stoichiometry of oxide layers.

For a general SEM system setup, the electron gun is responsible for generating electrons that are then directed, focused, and accelerated towards the sample surface [126]. The electron–matter interactions, e.g., secondary and backscattered electrons, and the material characteristic X-ray emission can be detected with multiple different in-column and in-chamber detectors. A schematic of the scanning electron microscope is shown in Fig. 11. The system used in this work is a Thermo Scientific Apreo S, equipped with a Schottky field-emission gun (FEG) electron source, modifiable vacuum operation modes, an electrostatic final lens, and a compound lens system (electrostatic, field-free magnetic, and magnetic immersion configurations). The microscope is configured with multiple in-lens and in-column SE/BSE detectors with energy filtering, and an Everhart–Thornley detector (E–T).

For elemental and compositional analysis, an Ultim Max 100 EDS spectrometer (Oxford Instruments) is employed together with AZtec EDS analysis software. This configuration enables high-throughput spectral acquisition, real-time elemental mapping, and automated feature-based compositional analysis, providing statistically robust characterization of material distributions across device structures.

3.2.4 Atomic Force Microscopy

Analyzing the topographical and surface roughness information on the sample can be done with atomic force microscopy (AFM) [126, 127]. AFM operation is based on the interactions between a fine, nanometer-sharp needle tip and the sample surface. As the tip scans across the surface it experiences short-range forces, including van der Waals, electrostatic, capillary, and repulsive Pauli forces. The needle is connected to a flexible cantilever, which will deflect due to the interaction forces. A laser beam reflected from the back of the cantilever onto a position-sensitive photodetector converts these deflections into height information, producing a three-dimensional topographical map of the surface. Unlike with electron-based microscopy, AFM does not require a vacuum to operate in, and the operation is not dependent on the con-

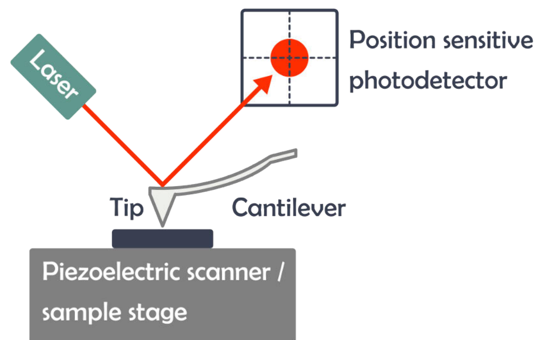

Figure 12. Atomic force microscopy (AFM) schematic. A sharp probe mounted on a flexible cantilever is scanned across the sample surface, where interatomic forces (van der Waals, electrostatic, and contact forces) between the tip and the surface cause cantilever deflection. These deflections are monitored using an optical beam deflection system and used to reconstruct high-resolution topographic maps of the surface. AFM provides nanoscale information on surface morphology, roughness, and nanomechanical properties of thin films or substrates.

ductivity of the sample. AFM is generally considered a non-destructive technique, particularly for relatively hard materials such as metals and oxides when operated under appropriate imaging conditions. The lateral resolution of AFM is limited by tip geometry, while the out-of-plane height resolution can reach nanoscale, allowing surface height variations related to grain structure and growth morphology to be resolved in favorable cases.

There are multiple different modes of operation that are suited for different material systems [126]. In contact mode, the tip operates in the repulsive regime of the tip-surface interaction potential, often described by the Lennard–Jones potential, where strong short-range forces provide highly sensitive height information and lateral resolution. The tapping/intermittent-contact mode or other dynamical modes are suitable for cases where the tip-surface contact time needs to be limited due to, for example, the sample being too soft or delicate. The oscillatory movement of the tip allows the characterization of the surface while reducing the lateral drag forces. In this work, surface characterization is performed using an Innova atomic force microscope (Bruker) operated in either contact or tapping mode with μMasch probes (UltraSharp CSC11/AlBS). The nominal tip radius is below $10\,\mathrm{nm}$, while the exact cantilever stiffness depends on the selected cantilever and measurement mode.

AFM provides quantitative roughness metrics (e.g., root mean square, RMS roughness) and reveals grain boundaries, pinholes, and pattern dimensions [127]. In this work, roughness is evaluated using the root-mean-square roughness, extracted from the height or height-sensor channel of forward and/or backward AFM scans after basic image leveling or flattening. The scan size may vary depending on the

surface features of interest and should therefore be considered when comparing roughness values. Variations in surface topography can lead to non-uniform current distributions and localized breakdown paths, increasing device-to-device variability. Therefore, AFM-based roughness analysis is important for optimizing deposition processes and ensuring reproducible device fabrication [10, 103].

3.3 Electrical Characterization

3.3.1 Measurement Setups (Keithley, ArC ONE)

Electrical characterization is central to evaluating memristor performance, as the switching behavior, stability, and reliability of the devices are determined entirely through electrical measurements [103]. The instrumentation should support quasi-static current-voltage (IV) sweeps, pulsed programming, endurance cycling, retention testing, and time-dependent measurements with high precision and low noise.

For precision direct current (DC) and pulsed IV characterization, Keithley source-measure units (SMUs) are used, primarily the Keithley 2614B in combination with a Keithley Series 7000 Multiplexer. The SMU provides accurate voltage sourcing and current measurement, enabling the extraction of key device parameters such as SET/RESET dynamics, HRS/LRS resistance ratios, and non-linear conduction characteristics. The multiplexer allows automated measurement of multiple devices on the same chip, improving throughput and statistical reliability.

For crossbar-based measurements, the ArC ONE memristor characterization platform is employed [128]. Crossbar arrays can suffer from sneak-path currents, where unselected cells provide unintended conduction paths that distort the measured response. Although this issue is often discussed for vertical passive crossbar arrays, it is fundamentally related to shared word line (WL)/bit line (BL) connectivity and can also occur in lateral crossbar-type geometries such as those used in this work. ArC ONE mitigates this using $V/2$ biasing, in which all unselected WLs and BLs are biased at half of the selected-cell bias [128, 129]. This reduces unwanted currents through neighboring devices and improves readout fidelity. $V/2$ biasing is particularly effective for memristors with non-linear or self-rectifying IV characteristics, which are considered ideal for passive crossbar architectures [129].

The combination of precision SMUs and the ArC ONE platform provides a comprehensive measurement environment for both single-device and array-level characterization.

3.3.2 Measurement Protocols

Standardized measurement protocols are essential for ensuring repeatability, comparability, and physical interpretability of memristor characterization [103]. Because

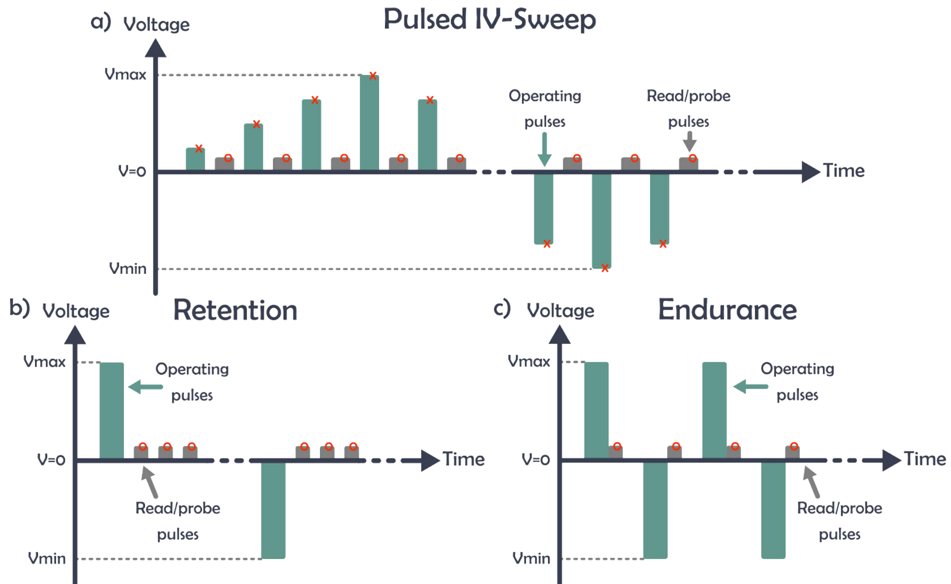

Figure 13. (a) Basic pulsed current-voltage (IV) measurement schematic. Voltage pulses of defined amplitude and duration are applied across the device under test while the resulting current response is recorded. In this thesis, pulsed voltage sweeps used pulse widths of 2–20 ms, interpulse delays of 0–10 ms, and, when included, read voltages below 1.0 V, with exact values depending on the measurement. The pulsed measurement scheme reduces Joule heating and mitigates irreversible degradation, enabling reliable characterization of electrical transport, switching behavior, and resistive states of thin-film devices. (b) Basic retention measurement schematic, where the device is programmed into a specific resistive state and its resistance (or current) is monitored over time under a low, non-perturbative read bias to assess temporal stability and non-volatility. (c) Basic endurance measurement schematic, where repeated voltage pulse sequences cycle the device between resistive states while monitoring the corresponding current or resistance, enabling evaluation of switching stability and cycle-to-cycle reproducibility over repeated switching events.

memristors exhibit history-dependent behavior, identical measurement sequences are applied across all devices for accurate comparison. Characterization begins with pulsed IV sweeps to identify SET and RESET behavior, hysteresis behavior, cycle-to-cycle variability, and asymmetry between positive and negative polarity [103]. The basic pulsed IV schematic can be seen in Fig. 13a. Pulsed IV measurements minimize Joule heating and reduce irreversible degradation of the device [103, 130]. Between programming pulses, optional low-voltage read pulses can be applied to monitor the altered device resistance without disturbing the state. The read voltage is chosen to avoid triggering unintended switching.

Voltage sweeps are performed using pulsed measurements with pulse widths of 2–20 ms, interpulse delays of 0–10 ms, and, when used, read voltages below 1.0 V. The exact voltage limits, pulse widths, interpulse delays, read voltages, and number of repeated cycles are given in the corresponding figure captions or related text. In Keithley 2614B measurements, the current is sampled identically during all programmed and read/probe pulses: the current is collected inside the pulse, delayed by a set time after turning the source on. Unless otherwise specified, each programming or read pulse produces one current value rather than a continuous time-resolved current trace over the full pulse duration. In ArC ONE IV measurements, the current is measured during the applied pulsed voltage sweep itself, near the end of each voltage pulse. Separate ArC ONE read operations are included only in protocols explicitly designed to contain them. These read operations use the TIA4P mode, i.e., Kelvin sensing at a controllable read voltage, and the reported resistance state value is obtained by averaging the measured response over the programmed number of reading cycles, typically 50 recorded data points. When mean or median resistance values are reported, they refer to statistics over repeated sweeps, pulses, cycles, or devices, not to a time-resolved median within a single pulse unless explicitly stated.

Once stable switching is established, retention is evaluated by programming the device into a defined resistive state and monitoring its resistance over time under non-disturbing read conditions, utilizing the internal read-operation (Fig. 13b). Non-volatile (synaptic-like) behavior is indicated by stable resistance over long timescales, while volatile (neuronal-like) behavior is characterized by spontaneous relaxation back to the initial state, often following exponential or power-law decay. Retention measurements reveal the temporal stability of the programmed resistive state and help distinguish between volatile and non-volatile switching behavior [103].

Endurance quantifies cycle-to-cycle reproducibility of SET and RESET operations and helps approximate device lifetime [103, 130]. As shown in Fig. 13c, the device is repeatedly cycled between its high-resistance state and low-resistance state using SET and RESET pulses. One cycle usually consists of a single pulse or a train of pulses per polarity, and the current response is collected with the internal read-operation. Endurance testing may also be performed at elevated temperatures to accelerate aging [103, 130]. Because endurance can degrade the device, it is typi-

cally the final measurement in the characterization sequence.

Beyond the basic SET/RESET and retention tests, specialized pulsing schemes can probe neuromorphic behavior [41, 42, 103]. For example, integration-and-leakage sequences can be used to mimic neuronal membrane dynamics, incremental SET pulse trains can reveal analog or multistate switching capability, and paired-pulse protocols can be used to test short-term plasticity. These measurements provide insight into the dynamic response of the memristor and its suitability for neuromorphic computing applications [15, 89].

4 Results and Discussion

Table 3. Summary of the GCMO samples and devices included in Publications [I, II, III, IV].

Pub.	Substrate	Film structure	Layers	Device type	Main behavior / role
[I]	STO	PLD-grown crystalline GCMO	GCMO: 80 nm; Al_2O_3: 10 nm; Al: 50/150 nm; Au: 100 nm	Crossbar-type Al/GCMO devices with Al-filled $15 \times 15\,\mu m^2$ vias through Al_2O_3; 3×3 arrays	Synaptic-like, multistate, non-volatile RS
[II]	STO	PLD-grown crystalline GCMO	GCMO: 100 nm; Al: 150 nm; Au: 50 nm	Lateral Al/GCMO crosspoint devices with active-area widths of 50, 100, 200, and 300 μm	Area-dependence study; multistate, non-volatile RS
	STO	PLD-grown crystalline GCMO	GCMO: 100 nm; Al: 30 nm; Au: 50 nm	Lateral Al/GCMO crosspoint devices with 400 μm-wide Al stripes for XPS depth profiling	Interface-mechanism study; non-volatile HRS/LRS chemical comparison
[III]	STO	Epitaxial/textured PLD-grown GCMO with uniform film surface	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	Consistent non-volatile RS; distinguishable LRS and HRS under retention
	MgO	Polycrystalline PLD-grown GCMO with cracked/deteriorated film surface	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	Consistent bipolar RS and endurance; volatile/ leaky retention behavior
	NGO	Polycrystalline or partly textured PLD-grown GCMO with cracked/deteriorated film surface	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	Partly reproducible RS with state drift; no clearly retained LRS/HRS separation
	Si-STO-epi	Epitaxial PLD-grown GCMO on epitaxial STO-buffered Si; two GCMO phases observed	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	RS in 3/4 junctions; distinguishable retention states but anomalous/ reversed switching behavior
	Si-STO	PLD-grown GCMO on polycrystalline STO-buffered Si; cracked/deteriorated film surface	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	No clear RS with the used device design
	Si	PLD-grown GCMO on Si; cracked/ deteriorated film surface	GCMO: 80 nm; Al: direct wire bonding; Au: 200 nm	Planar lateral devices contacted through Au pads and Al wire bonds, wire diameter 33 μm	Poor reproducibility; excluded from detailed RS discussion
[IV]	STO	Fully textured, c-axis-oriented PLD-grown GCMO	GCMO: 70 nm; Al: 150 nm; Au: 50 nm	Lateral Al/GCMO crosspoint devices with $40 \times 40\,\mu m^2$ active area	Standard RS; LRS remains distinguishable from HRS in retention
	MgO	Polycrystalline PLD-grown GCMO	GCMO: 70 nm; Al: 150 nm; Au: 50 nm	Lateral Al/GCMO crosspoint devices with $40 \times 40\,\mu m^2$ active area	Volatile LRS; leaky-integrate/neuronal-like functionality
	STO with 7 nm MgO buffer	PLD-grown GCMO on MgO-buffered STO; GCMO structurally similar to MgO-grown film	GCMO: 70 nm; MgO buffer: 7 nm; Al: 150 nm; Au: 200 nm	Lateral Al/GCMO crosspoint devices with $50 \times 50\,\mu m^2$ active area	Volatile LRS; leaky-integrate/neuronal-like functionality

Table 3 summarizes the main GCMO samples and device structures discussed in the following sections and in the related Publications [I, II, III, IV]. The table is intended to guide the comparison between substrate-induced film structure, device geometry, and the resulting resistive switching behavior.

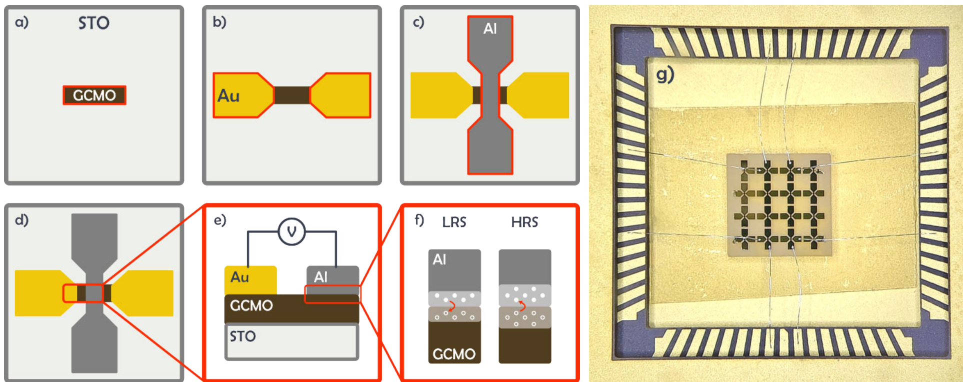

Figure 14. Fabrication sequence and final structure of the planar crosspoint device. (a) Patterned GCMO layer, (b) deposition of Au contact pads, (c) deposition of Al stripes intersecting the GCMO regions to form active junctions, (d) schematic layout of the full patterned device, (e) schematic cross-sectional view of the device stack, (f) schematic illustration of oxygen migration at the Al/GCMO interface in the high-resistance state (HRS) and low-resistance state (LRS), and (g) photograph of a fabricated chip wire bonded to a chip carrier for electrical characterization.

4.1 Device Architectures

4.1.1 Planar Crosspoint Structures

To investigate the influence of fabrication parameters on device performance, planar crosspoint structures are employed as a versatile test platform [II, IV, VI][42]. This geometry enables systematic variation of substrates and buffer layers, electrode materials, and device dimensions while maintaining straightforward processing [II, IV, VI].

In the planar configuration, the passive Au electrode is patterned on top of the GCMO film, and the active Al electrode is deposited orthogonally, forming a lateral crosspoint on the film surface. In this geometry, the current flows laterally along the GCMO film and resistive switching occurs at the Al/GCMO interface. Consequently, the effective active region is determined by this interface rather than by a vertically stacked electrode overlap area. In contrast, the active device area in conventional vertical memristor structures is typically defined by the overlap between the two electrodes [28, 103]. A schematic overview of the fabrication steps (a–c), finalized pattern (d), device cross-section (e), schematic of oxygen at Al/GCMO interface (f), and the final chip (g) are shown in Fig. 14.

For the planar crosspoint devices fabricated in this work, the thickness of the GCMO layer is typically in the range of 60–80 nm, grown on top of the chosen substrate material. The Al active electrodes and Au contact pads are deposited with thicknesses between 30 nm and 200 nm depending on the specific experiment. The lateral dimensions of the planar devices are varied to investigate size-dependent behavior, with nominal active regions ranging from $40 \times 40\,\mu\text{m}^2$ to $400 \times 400\,\mu\text{m}^2$.

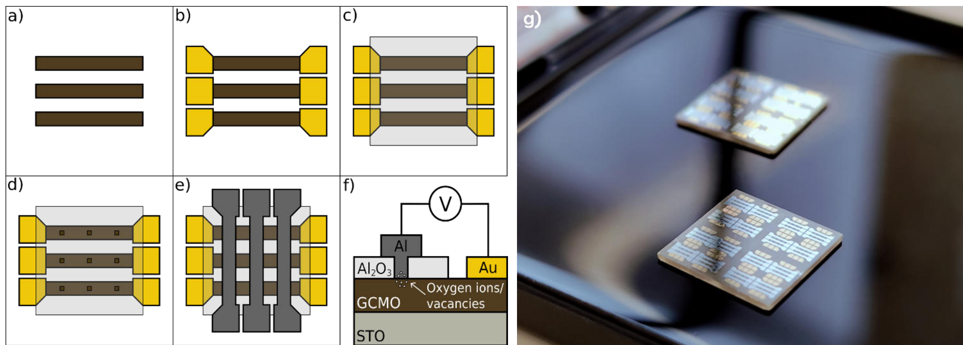

Figure 15. Schematic illustration of the crossbar array fabrication and structure. (a) Patterned GCMO layer as bottom connections, (b) deposition of Au contact pads, (c) optional deposition of an insulating layer, (d) via formation through the insulating layer to define active junctions, (e) deposition of orthogonal Al top electrodes, and (f) cross-sectional view of a single memristor cell within the array. (g) Photograph of finished patterned chips with multiple crossbar array structures. Figures (a–f) adapted from this work [I].

The structural quality of the deposited GCMO films is verified using XRD and XRR as required, while device patterning and electrode dimensions are inspected using AFM, SEM, and EDS. These characterization techniques are described in more detail in the corresponding sections in Section 3.

Planar devices offer several practical advantages in processing and characterization [103]. Fabrication is straightforward and compatible with standard photolithography processes, of which wet chemical etching is utilized for the PLD-fabricated GCMO and EBPVD, combined with lift-off for the metal electrodes. Electrical characterization is straightforward due to direct access to large contact pads, enabling rapid screening of multiple devices on a single chip. Depositing the active layer directly onto the optimized substrate improves the overall quality of the resulting thin film. In addition, lowering the surface roughness of the active material is crucial for minimizing variability between devices [103].

However, the planar geometry introduces some limitations [103]. The lateral layout limits scalability compared to fully vertical crossbar architectures, where device area can be reduced more aggressively [103]. The planar geometry is also less suitable for scaling to larger arrays due to the GCMO bulk and line resistances hindering the accessibility of devices further away from the electrical contact sites [128]. Despite these limitations, planar crosspoint structures provide an efficient and reliable platform for evaluating material properties and interface-controlled switching mechanisms before transitioning to fully vertically integrated device architectures.

4.1.2 Crossbar Arrays

For most practical applications, such as synaptic arrays, memristive devices are implemented in a crossbar array configuration [5, 7, 15, 16, 103]. In this architecture, bottom and top electrodes are usually arranged orthogonally in a stacked geometry, and the active material is sandwiched between them. Each intersection between a bottom and top electrode, i.e., the word and bit lines, defines an individual memristor cell.

Compared to singular planar crosspoint structures, the crossbar layout connects multiple devices through continuous electrode lines [103]. In the present implementation, this is achieved by elongating the patterned GCMO regions to form shared bottom connections between adjacent memristor devices [I]. As in the planar geometry, current transport still involves lateral conduction through the GCMO film, and the active interface is at the intersections with the active electrode. However, unlike isolated planar devices, the crossbar structure allows multiple cells to be integrated into a compact, addressable array [103]. Because current is transported laterally along the GCMO lines, the finite resistivity of the oxide introduces line resistance, limiting scalability to larger arrays. As described, the crossbar array still remains well-suited for small-scale test configurations [I][128].

The fabrication sequence (a–e), the cross-section of one junction (f) and the completed chips (g) are illustrated in Fig. 15. The fabrication begins with patterning of the GCMO layer as the bottom connection lines, followed by deposition of Au contact pads. An insulating layer, such as Al_2O_3 or SiO_2, may be deposited to electrically separate crossing electrodes depending on the fabrication scheme. Vias can then be etched in the insulating layer to expose the GCMO surface and define the electrode intersection region. Finally, Al top electrodes are deposited orthogonally to the bottom lines, completing the array structure. The effective switching region remains the Al/GCMO interface, similar to the planar crosspoint configuration. The introduction of the insulating layer and via definition allows precise control of the active device area. This control is critical in array configurations, where small variations in device area directly translate into resistance variability and reduced uniformity across the array [103].

Apart from the additional optional insulating layer and via definition, the fabrication process largely follows the procedures described for the planar crosspoint devices. The GCMO thin films are deposited by PLD, while the metallic electrodes (Al and Au) are deposited using EBPVD. When required by the array design, an insulating oxide layer can be deposited by ALD to electrically isolate crossing material layers. Vias through the insulating layer can then be defined by etching to expose the underlying GCMO surface and form the active junction regions. In the devices reported in [I], the vias defining the junctions had lateral dimensions of approximately $15 \times 15\,\mu m^2$. In this work, the vias are opened using Ar ion bombardment, although

reactive ion etching (RIE) could provide improved control for this process step due to material selectivity.

An alternative architecture places a separate bottom electrode beneath the GCMO layer in a fully vertical stack, further improving integration density by minimizing the lateral current flow through the active material. However, because GCMO growth is sensitive to the lattice parameters of the underlying layer, the choice of compatible bottom electrode materials is limited [III, IV]. Some highly conducting oxides could prove suitable: $SrRuO_3$ (SRO) or $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) because they share the perovskite structure and provide a matching lattice template [42]. Regardless of the specific stacking sequence, the fundamental crossbar principle remains the same.

Crossbar arrays can naturally perform analog vector-matrix multiplication by ohmic summation of currents along shared word and bit lines [5, 7, 15, 16, 89]. This offers clear advantages in scalability and integration density compared to separated planar crosspoint structures. However, shared access also introduces challenges. Electrical crosstalk between neighboring cells, sneak-path currents, can complicate readout in passive arrays [5, 90, 128, 129, 131]. In the present experiments, sneak-path effects are mitigated through the measurement protocol and biasing scheme described in Section 3. In addition, achieving uniform switching behavior across large arrays requires precise control over film thickness, interface quality, and electrode patterning [103]. Variations in these parameters directly affect device-to-device reproducibility.

Despite these challenges, the crossbar architecture represents the most relevant configuration for larger-scale implementation of GCMO-based memristors in synaptic arrays and neuromorphic computing systems, where dense integration and parallel computation are essential [16].

4.1.3 Active Interface

Fully understanding and optimizing the GCMO-based memristors requires knowledge of the physically active region behind resistive switching [27–29]. In perovskite manganites such as PCMO, this switching is generally attributed to electric-field-driven motion of oxygen ions or vacancies, which locally adjusts the manganese valence and the electronic conductivity of the interfacial barrier [37, 41, 62, 80]. By extension, the switching in GCMO devices is anticipated to originate from oxygen redistribution at the GCMO/active-electrode interface [II]. In the present structure, aluminum serves as the top electrode and, owing to its high oxygen affinity, is central to the interfacial redox processes [II].

Upon Al deposition on GCMO, oxygen migrates from the near-interface region of GCMO into the Al layer, forming an interfacial Al oxide and simultaneously altering the oxygen stoichiometry in GCMO [II][61]. Under applied bias, this process becomes field-assisted, promoting reversible oxygen exchange across the interface

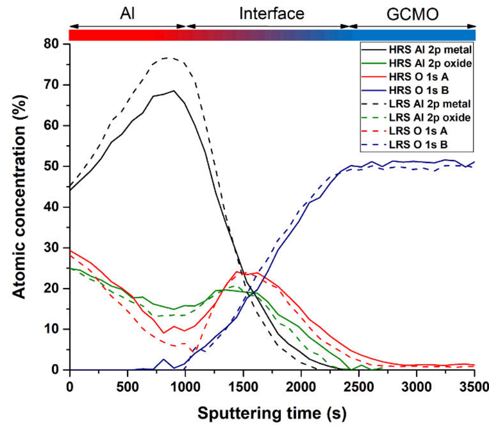

Figure 16. X-ray photoelectron spectroscopy (XPS) depth profiles of Al 2p and O 1s core-level signals for Al/GCMO devices programmed into the high-resistance state (HRS) and low-resistance state (LRS). The memristor devices consisted of a $100\,\mathrm{nm}$ PLD-grown GCMO film on STO, $50\,\mathrm{nm}$ Au ohmic contact pads, and $30\,\mathrm{nm}$ Al stripes forming a $400 \times 400\,\mu\mathrm{m}^2$ Al/GCMO crosspoint area. Atomic concentrations are normalized to the total detected signal, while other detected elements are omitted for clarity. Reproduced from this work [II].

[II][62, 80]. The consequent changes in thickness and stoichiometry of the interfacial oxide modulate the effective electronic barrier between the metal contact and the oxide, thereby enabling programming of the device resistance [II][37, 62]. The resistive switching in this GCMO-based system is expected to be governed by relatively uniform interfacial processes rather than filament formation, similar to other perovskite manganite systems [28, 41].

To probe the chemical states across the Al/GCMO stack, XPS depth profiling is performed on representative devices in the HRS and LRS [II][37, 132]. Before the XPS measurements, the devices are electrically switched into the target resistance states, and the retained states are verified with a low-voltage read pulse prior to depth profiling. Because the XPS analysis area is relatively large compared to the lateral dimensions of typical memristor junctions, these measurements are performed on planar crosspoint devices with large active areas so that the detected signal predominantly originates from the Al/GCMO junction region [II]. The analysis focuses primarily on the Al 2p and O 1s core levels, which directly probe the formation and evolution of the interfacial AlO_x layer. The Al 2p spectra can be deconvoluted into metallic and oxide-related components, while the O 1s spectra are fitted with contributions associated with lattice oxygen in the GCMO bulk (O 1s B) and higher binding energy species arising from Al–O bonding and oxygen defect states (O 1s A). The resulting depth profiles of Al 2p and O 1s chemical states for representative HRS and LRS devices are presented in Fig. 16. The XPS data have been collected and interpreted by J. Laaksonen. Three regions can be distinguished: the Al pad, the

GCMO bulk, and an interfacial region between them. The interface is characterized by the coexistence of metallic aluminum, oxidized aluminum species, and the gradual emergence of GCMO lattice oxygen. In the depth profiles, this region is defined by the first appearance of the GCMO lattice-oxygen contribution (O 1s B) and its subsequent increase to the bulk concentration, corresponding approximately to 600–$2300\,\mathrm{s}$ in HRS and 900–$2300\,\mathrm{s}$ in LRS [II]. The sputtering axis is kept in units of time because a reliable single sputter-rate conversion cannot be assigned across the material stack, where the sputter yield changes between metallic Al, oxidized Al, and GCMO.

The high oxygen signal at very low sputtering times is attributed to native oxidation of the air-exposed Al surface, which is comparable for both resistance states and is distinct from the buried Al/GCMO interface. Between the HRS and LRS devices, clear differences in the oxygen distribution can be observed after removal of the Al-surface layers [II][37, 61, 62]. In the HRS device, the fraction of oxidized aluminum is noticeably higher than in the LRS device, and the transition from metallic Al to bulk GCMO appears to occur over a slightly broader sputtering interval. In contrast, the LRS device exhibits a marginally sharper transition, indicated by a steeper slope, with a lower overall oxide fraction in the aluminum region. However, differences in transition width should be interpreted cautiously, since sputtering time does not correspond directly to physical depth across a multilayer stack with material-dependent sputter yields. A broader transition in HRS could indicate enhanced interdiffusion and progressive oxidation, consistent with the formation of a thicker or more stoichiometric AlO_x barrier. In the LRS device, the comparatively reduced oxide fraction implies partial reduction of the interfacial layer, resulting in a thinner or less insulating barrier, and these changes can also be observed in the corresponding gradual hysteresis present in the IV characterization [II].

The identification of the Al/GCMO interface as the active region has direct implications for device optimization, as it provides a pathway to improving stability, endurance, and dynamic range [I, II, III, IV]. The switching-relevant region appears to be specifically the bottom side of the Al layer in contact with GCMO, where both the Al electrode and the GCMO film contribute through interfacial oxygen exchange. Control of oxygen mobility and interfacial oxidation kinetics is therefore central to the development of GCMO-based memristive architectures intended for scalable crossbar arrays and neuromorphic computing applications [42]. While the XPS depth profiles provide strong evidence for interfacial oxidation changes, complementary structural characterization, such as cross-sectional transmission electron microscopy (TEM), could further clarify the detailed structure and thickness of the interfacial oxide layer.

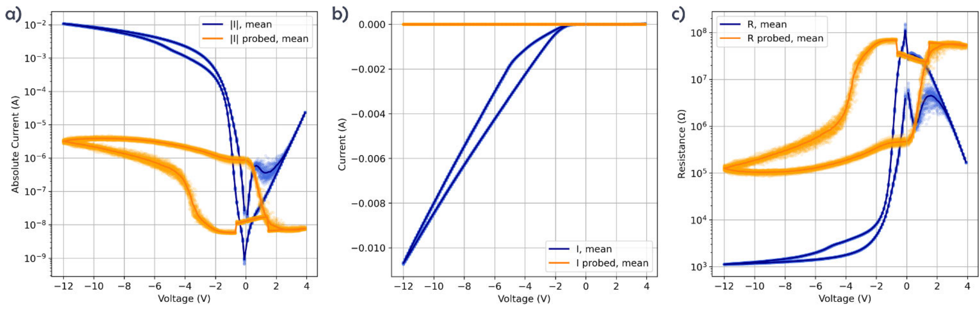

Figure 17. Representative cycled pulsed IV electrical characteristics (Keithley 2614B) of a single lateral Al/GCMO crosspoint device shown using different data representations: (a) absolute current-voltage ($|IV|$), (b) current-voltage (IV), and (c) resistance-voltage (RV). The device has an active area of $300 \times 300\,\mu$m^2 and consists of a 100 nm PLD-grown crystalline GCMO film contacted by 150 nm Al and 50 nm Au electrodes. In each panel, the blue curve corresponds to the primary switching measurement, while the orange curve represents the low-bias read/probe measurement of the same device at -0.4 V. The data show 50 repeated pulsed IV sweep cycles (20 ms pulses, $V_{\min} = -12$ V and $V_{\max} = 4$ V) together with the calculated mean curve. Redrawn from this work [II].

4.2 Synaptic Behavior

4.2.1 Non-Volatile Resistive Switching

The resistive switching behavior in GCMO-based devices grown on STO substrates is usually non-volatile, with well-defined high-resistance and low-resistance states under electrical bias [I, II, III, IV]. A particularly advantageous feature of these interface-type switching devices is the lack of a required initial filament-forming step [28]. In this thesis, forming-free operation refers to the absence of a separate high-voltage electroforming step or dedicated conditioning before the observation of resistive switching; any preliminary sweeps are performed within the normal operating voltage range and are used only to verify or stabilize the device response. The forming-free operation simplifies initial device conditioning, allows low power operation, and enhances the uniformity of switching parameters across different junctions [18, 28].

The polarity of the device operation depends on the chosen ground; when the Au electrode is grounded, negative oxygen ions (O^{2-}) are attracted towards the Al electrode on positive bias (equivalent to effectively positive oxygen vacancies V_O drifting towards the Au electrode), causing the RESET to HRS [II][10, 27, 61]. Conversely, grounding the Al electrode reverses this operational polarity. As seen from the IV measurement results represented in Fig. 17, the switching is extremely stable over repeated cycles, the operation is bipolar with asymmetric SET and RESET voltages, with slight self-rectification arising from the rectifying Al/GCMO interface (difference in work functions) [II][43, 133]. The conduction in similar GCMO-based

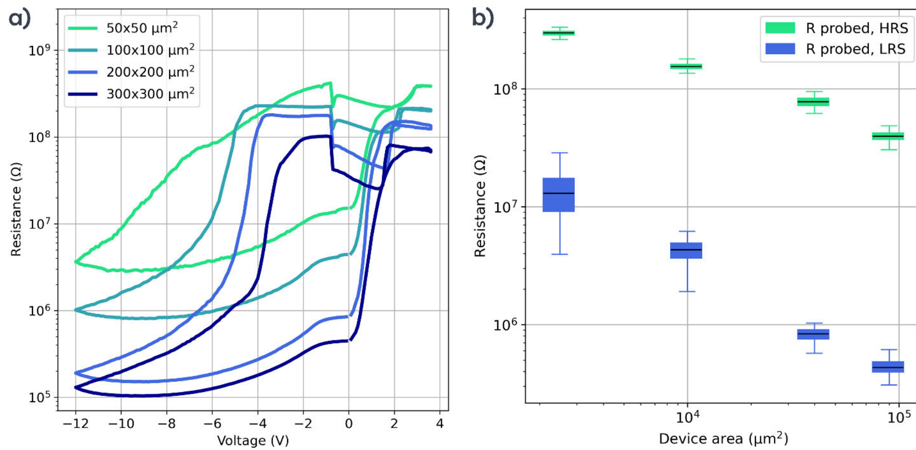

Figure 18. Area dependence of device resistance in lateral Al/GCMO crosspoint devices: 100 nm PLD-grown crystalline GCMO contacted by 150 nm Al and 50 nm Au electrodes. Four devices with active-area side lengths of 50, 100, 200, and $300\,\mu$m. (a) Mean resistance-voltage (RV) characteristics measured from the low-bias read/probe data at -0.4 V. Mean values calculated from 100 repeated pulsed IV sweeps (Keithley 2614B, 20 ms pulses, $V_{\text{min}} = -12$ V and $V_{\text{max}} = 4$ V) for each device size. (b) Box plot representation of the HRS and LRS resistance distributions for the corresponding device sizes. Values extracted from the read/probe data at -0.4 V over the 100 repeated pulsed IV sweeps. Redrawn from this work [II].

interface-type devices has been reported to follow Poole–Frenkel emission during the SET process (from HRS to LRS) and Schottky-type conduction during the RESET process (from LRS to HRS) [43]. The probed curve exhibits the two reachable resistance states with the chosen operating voltage sequence.

Area-scaling, non-volatility, retention and endurance characteristics, the multi-state usage and device-to-device variability are discussed in the following sections.

4.2.2 Area Dependence of Resistive States

The dependence of resistance on device area provides insight into the switching mechanism [10, 27, 28, 64]. As discussed in Section 2.1.2, the area scaling of the resistance, especially the low-resistance state, serves as a primary indicator to distinguish between interfacial switching and localized filamentary conduction [28]. Figure 18a displays the mean probed resistance values for devices with varying device active areas, while Figure 18b provides a statistical representation of the resistance distributions at the chosen read voltage [II]. The devices used in this analysis are planar crosspoint structures with active areas of $50 \times 50\,\mu\text{m}^2$, $100 \times 100\,\mu\text{m}^2$, $200 \times 200\,\mu\text{m}^2$, and $300 \times 300\,\mu\text{m}^2$, defined by the intersection of the Al electrode and the patterned GCMO region.

Both the HRS and LRS exhibit an approximately inverse dependence on device

area ($R \propto 1/A$), consistent with transport governed by the full interfacial area. For interface-controlled conduction, the resistance can be expressed as $R = k/A + R_0$, where the slope k reflects the effective interface resistivity and R_0 accounts for series contributions such as electrode and contact resistances. Correspondingly, the conductance follows an approximately proportional dependence on area ($G \propto A$), indicating spatially distributed current flow across the junction.

The inverse area scaling is clearly observed in the LRS (Fig. 18b), where the resistance decreases systematically with increasing device area. This behavior is consistent with a uniform current distribution across the AlO_x/GCMO interface and supports an interfacial switching mechanism. In this mechanism and device geometry, GCMO is not only a passive oxygen source: it provides the oxygen-exchange reservoir, the lateral transport path, and the semiconducting near-interface electronic structure that, together with the oxidized Al layer, defines the rectifying AlO_x/GCMO barrier and enables its reversible modulation. In contrast, localized filamentary conduction would yield an area-independent LRS resistance, which is not observed here. These observations indicate a relatively uniform current distribution across the active interface and are consistent with an interface-controlled mechanism, where the resistance is governed by mostly homogeneous modulation of the Schottky barrier height or width across the entire junction area [II][28].

Minor deviations from ideal inverse scaling are observable in the HRS, particularly for smaller device areas. These variations can arise from a combination of measurement limitations at high-resistance levels, enhanced edge effects, and local inhomogeneities in the interfacial defect landscape [II][10, 37, 103]. In the HRS, current may preferentially flow through localized regions with a higher electric field, such as electrode edges, altering the effective conduction area. Such effects become increasingly significant as the device size decreases, where statistical variations in defect distribution have a larger relative impact on the total conductance [103].

Overall, the observed area-dependent scaling strongly supports the interpretation that switching in these GCMO-based devices is predominantly governed by interfacial barrier modulation rather than the formation of a stochastic, localized filament [II][27, 28]. While this behavior is consistent with interface-controlled transport, further distinction between fully homogeneous conduction and possible multifilamentary contributions would require scaling to smaller device dimensions or the use of spatially resolved characterization techniques, such as transmission electron microscopy.

4.2.3 Retention and Endurance

Retention and endurance are important metrics that define the stability and reliability of the programmed synaptic weights [42, 103, 130]. In this thesis, non-volatile switching refers to resistance states that remain distinguishable within the experi-

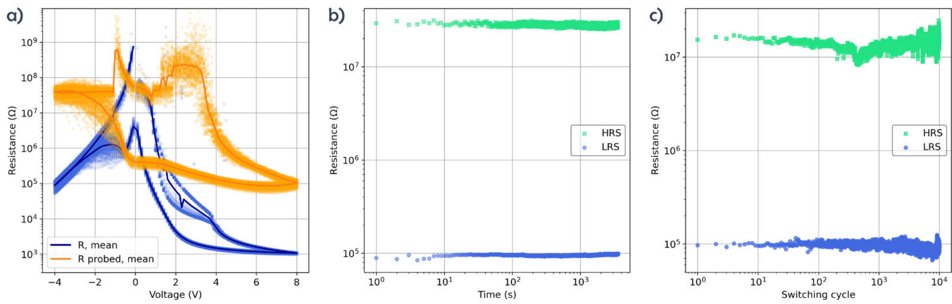

Figure 19. Switching, retention, and endurance characteristics of one GCMO-based memristive device fabricated on an STO substrate with an approximately 100 nm thick GCMO film, 70 nm Al, and 50 nm Au in a lateral crosspoint geometry with a $50 \times 50\,\mu$m^2 active area. (a) Representative RV characteristics measured with the Keithley 2614B using 20 ms pulses and a 10 ms interpulse delay. The primary switching resistance is shown in blue and the low-bias probe/read resistance in orange, measured at 0.4 V. The scatter points show repeated pulsed IV sweeps, while the solid lines show mean values. (b) Retention performance measured with ArC ONE under a -0.4 V read bias. The HRS is obtained after an IV sweep ending in the high-resistance state and is verified by readout before the retention measurement. The LRS is programmed using five 20 ms pulses at -8.0 V before the retention measurement. (c) Endurance performance measured with ArC ONE under repeated SET/RESET cycling. One endurance cycle consists of one 20 ms pulse at 4.0 V and one 20 ms pulse at -8.0 V, with the resistance read at -0.4 V after programming. The apparent SET/RESET polarities differ between panel (a) and panels (b, c) due to Keithley and ArC ONE measurements using opposite grounding configurations.

mentally measured retention window after removal of the programming stimulus, whereas volatile switching refers to a programmed state that spontaneously relaxes towards the initial resistance state within the measured time window. The classification can depend on the programming conditions, since pulse amplitude, polarity, width, number of pulses, and read delay determine how strongly the interfacial oxygen distribution is modified and whether the programmed state relaxes within the measured time window.

In our GCMO-based planar crosspoint devices (representative RV characteristics shown in Fig. 19a), retention measurements (Fig. 19b) reveal that both the HRS and LRS remain stable over extended periods with minimal drift, when programmed to the corresponding states, the RV curve suggests [I]. This suggests the robustness of the interfacial redox configuration and its capability for longer-term non-volatile memory storage. While some minor resistance drift in the LRS is common for perovskite manganites due to the relaxation of oxygen vacancy profiles [133–135], the overall window remains wide enough to distinguish states reliably. Although the measurements up to 4000 s presented here demonstrate stable retention over the investigated time window, longer retention measurements up to 8 h have been reported for similar GCMO-based devices [I]. Linear fitting of the measured drift suggests retention exceeding 10 years [I]. However, this extrapolation only describes gradual

drift under the measured conditions and does not account for sudden breakdown, nonlinear long-term relaxation, or thermally accelerated degradation. Accelerated retention testing at elevated temperatures, which is commonly used to extrapolate long-term stability, is not performed in this work.

Endurance testing (Fig. 19c) demonstrates the capacity for repeated switching without irreversible degradation or breakdown-like failure. From a synaptic perspective, this indicates that the device can reliably undergo frequent ”learning” (SET) and ”forgetting” (RESET) cycles [103, 130]. These GCMO-based devices typically maintain a stable resistance window over the measured cycles, reported up to 10^5 switching cycles [I]. This endurance reflects a reversible and controlled redistribution of oxygen vacancies at the Al/GCMO interface, ensuring consistent performance over prolonged operation [II][37, 61, 62].

The stability of the programmed states over the testing period reinforces the non-volatile nature of the switching mechanism. The observed retention and endurance characteristics indicate that these devices are suitable candidates for hardware-based neural networks, where consistent and repeatable weight updates are required for accurate learning [103, 130].

4.2.4 Gradual and Multistate (Analog) Switching

Beyond binary switching between HRS and LRS, GCMO-based devices support gradual conductance modulation, necessary for emulating biological synapses [I, II, VI][50, 51]. The multistate switching behavior discussed in this section is characterized using basic crosspoint devices and crossbar array structures reported in [I] and [II]. By controlling, for example, the amplitude of the applied voltage pulses or the number or width of the operating pulses, the resistance can be tuned incrementally between the HRS and LRS. This behavior originates from the progressive modulation of the interfacial AlO_x layer, in which oxygen ion migration occurs in a continuous manner under successive stimuli [II][37, 39, 84]. This enables a stepwise adjustment of the Schottky barrier properties, resulting in a gradual resistance change [27, 28, 43, 51]. This capability for multistate switching further corroborates the interface-type nature of the GCMO-based devices [II]. In filamentary systems, achieving intermediate states often requires the external manipulation of current compliance to limit the growth of localized conductive paths [5, 136, 137]. In contrast, the GCMO devices, like many non-filamentary devices, exhibit natural multistate behavior without the need for external current limiting [18]. Since the switching is area-distributed and governed by the gradual redistribution of oxygen ions across the entire junction, the resistance changes are inherently self-limiting and continuous [II][28].

As shown in Fig. 20a showcasing mean probed RV data obtained using the pulsed IV measurement protocol described in Section 3, multistate switching can

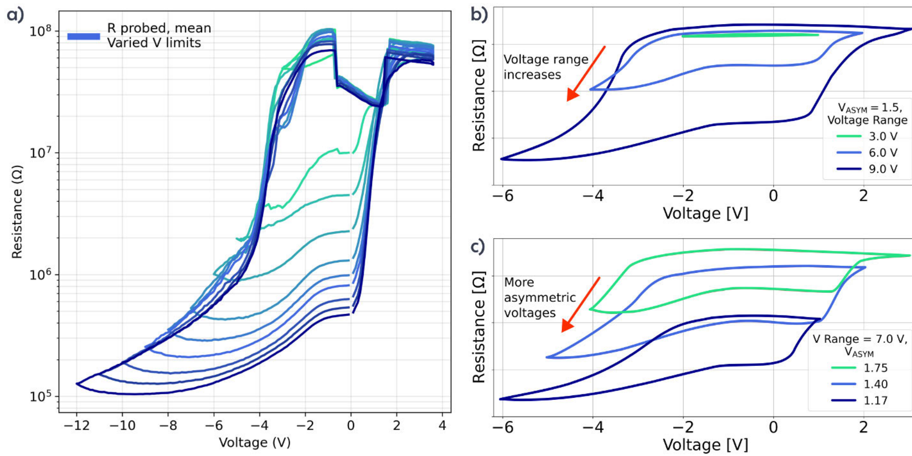

Figure 20. Effect of voltage-window parameters on resistance-voltage (RV) characteristics measured under low-bias probe conditions. (a) Multistate resistive switching behavior measured from the largest lateral Al/GCMO crosspoint device with an active area of $300 \times 300\,\mu$m^2. RV data obtained from repeated pulsed IV sweeps (Keithley 2614B, 20 ms pulses, read/probe voltage of -0.4 V). Mean values calculated from 50 repeated sweeps for each voltage window. (b) Schematic illustration of how changing the total voltage range at constant voltage asymmetry, $V_{\mathrm{asym}} = 1.50$, modifies the probed HRS and LRS resistance levels. (c) Schematic illustration of how changing V_{asym} at constant voltage range, $V_{\mathrm{range}} = 7.0$ V, modifies the probed resistance levels. Panel (a) is redrawn from this work [II]; panels (b, c) are redrawn from this work [I].

be achieved by varying the sweep range of the applied voltage [II]. Increasing the voltage amplitude expands the achievable resistance window (Fig. 20b), as a stronger electric field drives a larger volume of oxygen ions across the interface [I][51, 87]. Furthermore, introducing voltage asymmetry, where the positive and negative sweep limits are not equal, shifts both the HRS and LRS towards lower resistance values (Fig. 20c) [I]. This shift can be caused by an imbalance between the SET and RESET operations, which prevents the complete recovery of the interfacial oxidation. This reduction of the interfacial oxide barrier results in a net increase in conductance, allowing the device to operate within a lower resistance regime [51].

The ability to access intermediate conductance levels is essential for hardware-based neuromorphic computing [15, 87, 89]. In such architectures, the device conductance represents a synaptic weight, and the capacity for gradual tuning allows for more complex learning algorithms to be implemented directly in the crossbar hardware. In this work, repeated pulsed measurements demonstrate that multiple intermediate resistance states can be reproducibly accessed. However, retention has been systematically assessed only for selected high- and low-resistance conditions, as previously shown in Fig. 19; consequently, the long-term stability of the full set of intermediate resistance states has not yet been quantified. Therefore, the intermediate states are interpreted here as accessible programmed resistance levels, while their

retention stability, pulse-based potentiation/depression linearity, update symmetry, and statistical reproducibility remain to be established in future investigations. Although multistate and gradual resistance modulation is presented in [I, II, VI], these additional metrics are required to fully assess the suitability of the intermediate states for analog synaptic weight storage.

4.2.5 Device-to-Device Variability

Device-to-device variability is important for the large-scale implementation of neuromorphic crossbars [15, 138, 139]. It can be evaluated using arrays of nominally identical cells, as shown in the optical and bonded-chip images (Fig. 21a–b). The fabrication steps of such crossbar arrays follow those presented in Figures 14 and 15, with the device area ($50 \times 50\,\mu\text{m}^2$) defined by the cross-section of the GCMO stripe and the Al electrode. The full crossbar has been characterized as discussed previously in Section 3.3.2, with the ArC ONE measurement platform and IV sweeps [128]. The HRS/LRS resistance behavior at selected voltage endpoints (V_{min} and V_{max}) is chosen for comparative analysis. While the devices exhibit consistent switching polarity and operational mechanisms across the array, fluctuations are observed in the absolute resistance levels and switching thresholds.

The spatial heatmap and corresponding box plot (Fig. 21c–d) reveal the distribution of HRS and LRS values across the 6×6 array at a read voltage of -0.6 V. Notably, all devices in the crossbar displayed resistive switching with the chosen operating scheme, with HRS/LRS ratios reaching up to 10^3. The improved apparent uniformity compared with the data reported in [I] is most likely related to improved fabrication precision in the later device batch. Although the nominal material stack remains Al/GCMO/Au, the fabrication flow is simplified here by omitting the additional oxide layer, reducing possible sources of lithographic and interfacial variability. One device showed slightly reduced performance during this comparison, it later recovered, indicating some cycle-to-cycle variability among the devices. The observed non-uniformity between devices is primarily attributed to local variations in interface quality, stoichiometry, and oxygen vacancy density [103]. Furthermore, a clear resistance gradient is visible along the GCMO stripes, indicating that the operating voltage or film properties are influenced by the spatial position on the chip (e.g., due to line resistance) [90, 128].

In interface-type switching, the resistance is highly sensitive to the effective Schottky barrier height, so even minor fluctuations in the interfacial oxidation state during fabrication can lead to the observed dispersion in resistance levels or the optimal operation parameters [28, 37]. While decreasing the active area is essential for high-density integration, it typically increases variability due to a reduced averaging of local defects. Therefore, further optimization of lithographic uniformity and interface engineering is required to tighten these distributions for reliable large-scale

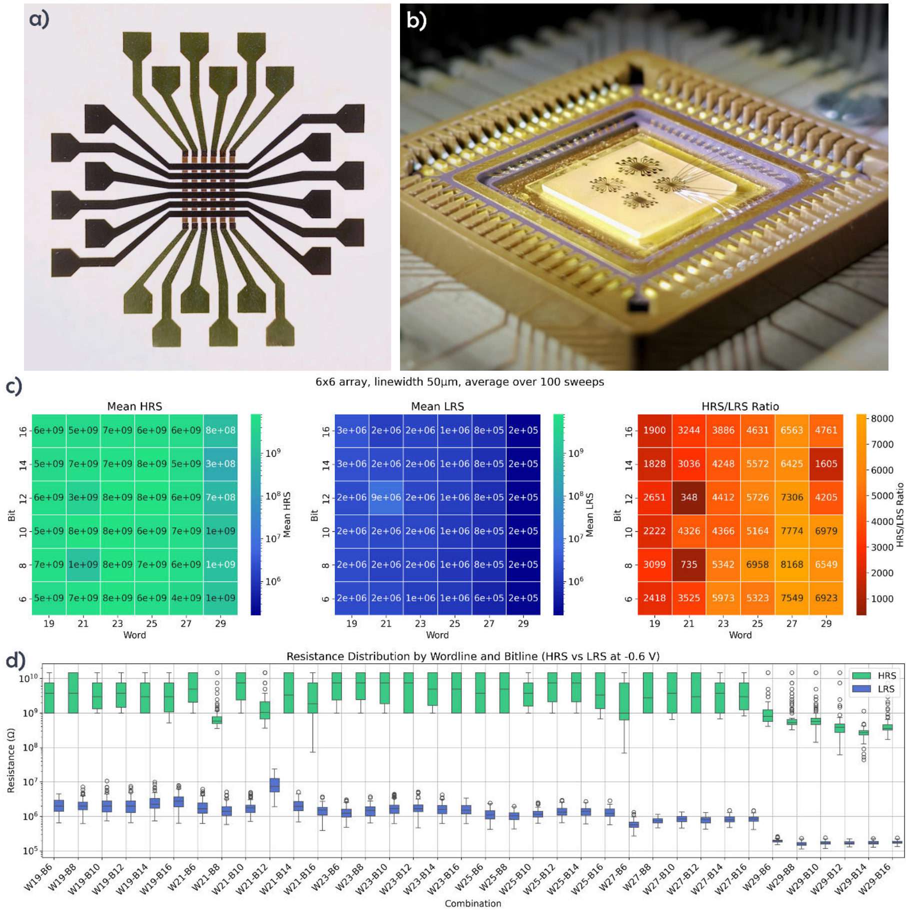

Figure 21. Device-to-device variability in a 6×6 lateral GCMO crossbar array. (a) Optical image of the fabricated crossbar array. (b) Photograph of the chip wire bonded to a carrier for electrical characterization. (c) Heatmaps and (d) corresponding box plot of high-resistance state (HRS) and low-resistance state (LRS) resistance values for the $50\,\mu$m linewidth array, extracted from IV sweeps measured with ArC ONE using a read voltage of -0.6 V and a programming window from 3 to -6 V over 100 repeated sweeps.

synaptic arrays [I][103].

4.3 Neuronal Behavior

4.3.1 Volatile Resistive Switching

While the previous sections reported the Al/GCMO interface as a promising candidate for non-volatile, synaptic memory, certain device configurations and operating conditions exhibit an alternative operational regime: volatile resistive switching [30, 95]. In this mode, the low-resistance state is transient. Upon the removal of the external electrical stimulus, the device does not maintain its programmed state but spontaneously relaxes back towards its initial high-resistance state baseline [80, 95]. The LRS leakage or relaxation is a known property in some manganite-based devices, albeit the relaxation time and magnitude vary significantly [III, IV][133–135].

Figure 22 illustrates this contrast through a comparative study of crosspoint devices of active areas $40 \times 40\,\mu\text{m}^2$ fabricated on STO and MgO substrates [IV]. Both configurations exhibit clear resistive switching with a comparable HRS/LRS ratio during initial characterization (Fig. 22a–b). However, their temporal stability differs fundamentally: while devices on STO substrates exhibit more robust retention (Fig. 22c) required for longer-term memory, devices on MgO show a rapid, spontaneous decay of the LRS (Fig. 22d). The experimental data presented in this figure are collected by I. Angervo and L. Miettinen.

In the measurements presented here, the volatile and non-volatile regimes are primarily observed in different sample types rather than systematically mapped within the same device. STO-based devices exhibit non-volatile retention under the programming conditions used in Fig. 22, whereas MgO-based and MgO-buffered devices exhibit volatile LRS relaxation under the corresponding pulse conditions [IV]. Therefore, the present data indicate a strong link between substrate-induced film structure and the dominant switching regime. However, the distinction may also depend on programming conditions, such as pulse amplitude, pulse width, number of pulses, pulse history, and read delay. Minor LRS drift in otherwise non-volatile STO-based devices indicates that relaxation is not completely absent, but under the tested programming conditions, it is too slow to be classified as the leaky component of neuronal-like operation, where relaxation should occur on a timescale comparable to the applied pulse sequence and temporal integration window [140, 141]. In this work, a systematic pulse-parameter map within a single GCMO device is not performed. Therefore, it remains unresolved whether volatile and non-volatile regimes can be continuously accessed within one device, or whether they are primarily fixed by substrate-induced crystallinity.

This short-term memory or volatility represents a reversible modulation of the interfacial barrier [37]. In this regime, the field-driven redistribution of oxygen ions

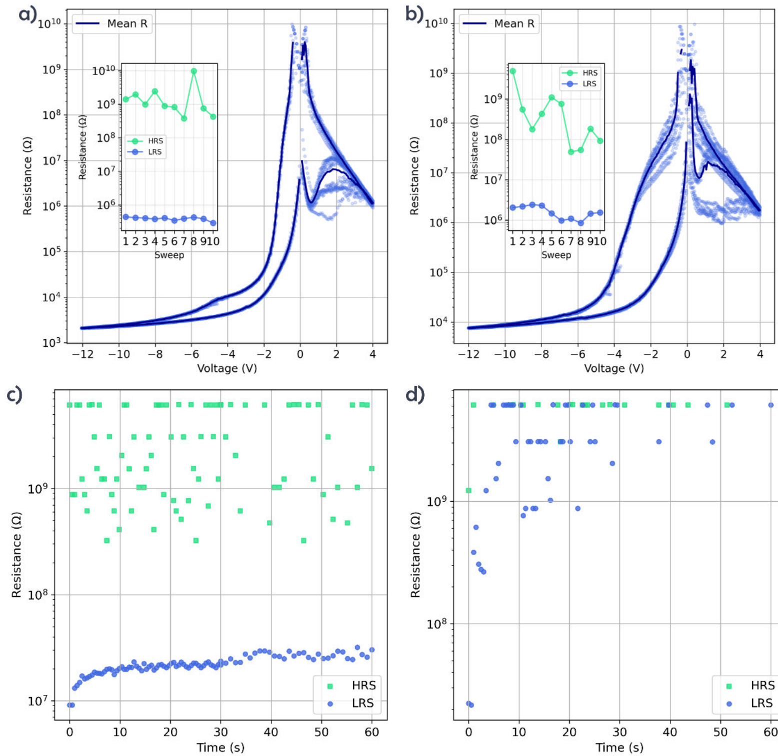

Figure 22. Comparison of switching behavior in GCMO-based crosspoint devices fabricated on different substrates. The devices consist of an approximately 70 nm thick GCMO film contacted by 150 nm Al and 50 nm Au electrodes, with an active Al/GCMO interface area of $40 \times 40\,\mu$m^2. Representative resistance-voltage (RV) characteristics measured with ArC ONE using 2 ms pulses are shown for devices on (a) $SrTiO_3$ (STO) and (b) MgO substrates, with the insets highlighting the switching ratio extracted from the RV data at -0.4 V. Corresponding retention measurements for devices on (c) STO exhibiting non-volatile switching and (d) MgO exhibiting volatile switching, where the low-resistance state spontaneously relaxes towards the high-resistance state. Retention measured at a read bias of -0.25 V after programming with single 2 ms voltage pulses of -12 V for SET and 4 V for RESET, corresponding to the end points of the IV/RV sweeps. The larger apparent HRS variability in the retention data is attributed to the high-resistance level approaching the practical readout limit of the ArC ONE setup, where small current fluctuations lead to comparatively large variations in the calculated resistance. Redrawn from this work [IV].

is energetically unstable in the absence of a bias, causing the system to return to equilibrium via back-diffusion [80]. This behavior could provide a direct hardware analogue of the excitation and decay phases of biological neurons, where the influence of a stimulus naturally fades over time [17, 96].

The observed volatility is attributed to interfacial processes that fail to produce a fully stabilized or metastable oxide configuration [III, IV][31]. Potential physical mechanisms include reversible redox reactions at the Al/GCMO interface, the modulation of shallow defect states, and the redistribution of mobile oxygen species. In this volatile regime, the interfacial Schottky barrier is temporarily lowered by the applied field but lacks the structural locking mechanism necessary to remain in a state after the field is withdrawn [IV]. Surface morphology of PLD-grown manganite films typically exhibits a granular microstructure observable in SEM or AFM measurements [III]. Such microstructural features may locally influence oxygen diffusion pathways and interfacial redox dynamics, potentially contributing to the observed volatility.

4.3.2 Substrate-Dependent Crystallinity

The switching dynamics of GCMO-based memristors are fundamentally coupled to the structural properties of the thin film, determined by the underlying growth substrate [III, IV]. The epitaxial strain state, crystallinity, and defect structure are governed by the lattice matching between the manganite and the substrate, as well as the specific growth conditions [105, 106]. Figure 23 presents the θ–2θ XRD scans for GCMO films deposited on various substrates, with the STO substrate scan having all the peaks annotated (hkl). The acquisition of the XRD (θ–2θ) scans is by I. Angervo and L. Miettinen [III, IV]. In addition to the crystallographic reflections, the STO reference scan also reveals the characteristic Cu Kα and Kβ radiation components of the X-ray source, together with weak parasitic peaks corresponding to wavelengths consistent with tungsten L-series radiation, likely originating from tube components or imperfect monochromation, producing secondary diffraction features at slightly shifted angles. These instrumental contributions are distinguishable in the high-quality STO substrate scan and therefore serve as a reference for interpreting peak positions in other samples. Similar peak identification can be performed on all samples, with the strongest and sharpest peaks corresponding to the substrate peaks, while thin-film peaks are usually weaker due to the significantly smaller scattering volume of the thin film.

Films grown on perovskite substrates with relatively small lattice mismatch, such as $SrTiO_3$ (STO) and $LaAlO_3$ (LAO), exhibit clear and intense diffraction peaks, particularly the GCMO reflections (220)/(004) and (440)/(008) as seen in Fig. 23 scans. Because the orthorhombic lattice parameters a and b for GCMO are nearly identical, these grouped reflections produce peaks at practically indistinguishable 2θ positions

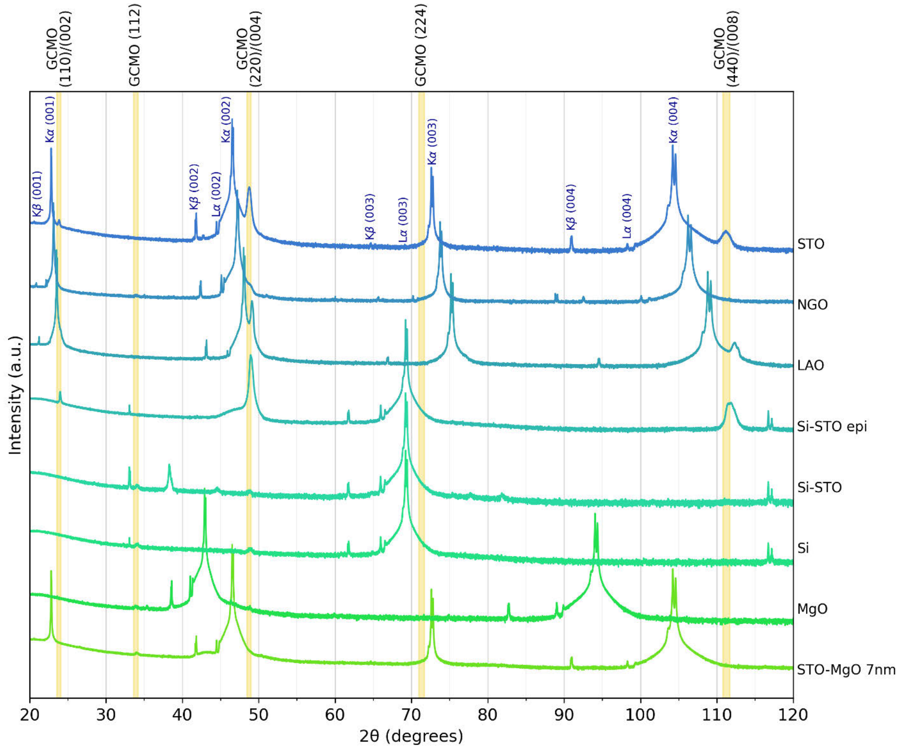

Figure 23. X-ray diffraction (θ–2θ) patterns of $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) thin films deposited on different substrates. The $SrTiO_3$ (STO) reference scan includes indexed substrate and film reflections and reveals characteristic Cu Kα and Kβ radiation components together with weak parasitic peaks corresponding to wavelengths consistent with tungsten L-series radiation from the X-ray source. These instrumental features serve as a reference for peak identification in other samples. Differences in peak intensity, sharpness, and multiplicity reflect variations in crystallographic orientation, crystalline quality, and degree of polycrystallinity, while systematic shifts in GCMO peak positions indicate substrate-induced epitaxial strain and corresponding changes in out-of-plane lattice parameters. Data related to works [III, IV].

in a θ–2θ scan. However, considering the typical epitaxial relationship, the $(00l)$ orientation is more likely. This indicates a preferred crystallographic orientation, consistent with highly oriented growth of the GCMO layer [III, IV] [104–107]. Complementary structural characterization is performed in [III] using SEM to examine film topography, while [IV] includes additional texture analysis through selected θ–2θ scans and 2θ–ϕ scans of specific peaks. The resulting high structural order provides a stable lattice environment that is expected to confine ionic defects and suppress their spontaneous back-diffusion, enabling the formation of non-volatile resistance states required for synaptic memory behavior [IV][43]. For the perovskite substrate $NdGaO_3$ (NGO), several expected GCMO reflections overlap with substrate peaks, making the film contribution less straightforward to identify in the θ–2θ scan [III].

In addition to differences in peak intensity and orientation, noticeable shifts in the GCMO diffraction peak positions are observed depending on the substrate. These shifts qualitatively indicate variations in the out-of-plane lattice spacing, which can be caused by substrate-induced epitaxial strain. Films grown on LAO exhibit particularly pronounced peak shifts despite the small nominal lattice mismatch discussed in Section 3.1.2. The effective LAO cubic lattice parameter is $5.36\,\text{Å}$ (corresponding to the $45°$ rotated in-plane match), while the GCMO in-plane lattice parameters are $5.30\,\text{Å}$ and $5.34\,\text{Å}$. The tensile strain causes out-of-plane contraction as the film expands in-plane, which manifests as diffraction peaks shifting towards higher angles. This behavior is consistent with coherent epitaxial growth, where the in-plane lattice of the film elastically conforms to the substrate, producing a compensating distortion of the out-of-plane lattice parameter [105–107]. In contrast, substrates with larger lattice mismatch promote earlier formation of misfit dislocations, enabling partial strain relaxation and resulting in peak positions closer to reported bulk GCMO values, noting that literature lattice parameters themselves exhibit some variation depending on composition and measurement conditions [III, IV][44]. The strain reflects the degree of lattice coherence rather than simply the magnitude of lattice mismatch.

For Si substrates, the introduction of an STO buffer layer alone is not sufficient to induce epitaxial GCMO growth; the buffer layer needs to be epitaxial or suitably ordered as well [IV]. For the non-epitaxial STO-buffered Si substrate and the Si substrate with native surface oxidation, the diffraction patterns for GCMO show weak reflections with no dominant orientation as seen in Fig. 23 scans, indicating reduced crystalline order [III]. The presence of multiple weak reflections suggests partially polycrystalline growth, whereas the absence of distinct film peaks in some cases could indicate nearly amorphous structure [101]. Notably, a minimum level of crystallinity seems to be needed to achieve resistive switching, as the films deposited on Si wafers with native oxide or non-epitaxial STO resulted in poorly crystalline or partially amorphous GCMO, which exhibited weak or inconsistent switching behavior in the present device structures [III]. However, additional factors such as buffer-layer

Table 4. Correlation between substrate-induced GCMO film structure and resistive switching behavior, summarized from Publications [III] and [IV]. It should be emphasized that the HRS/LRS ratios, as well as the state retention and endurance characteristics, are all strongly dependent on the specific operating parameters and device fabrication.

Substrate	GCMO film structure	RS character	Working junctions	HRS/LRS ratio	Retention	Endurance
STO	Epitaxial/textured; uniform surface in [III]	Consistent bipolar RS; non-volatile in [III]	$4/4$ in [III]	Up to 10^2 in [III]	HRS/LRS distinguishable, up to 250 min in [III]	Clear cycling observed, up to 10^4 in [III]
NGO	Polycrystalline or partly textured; cracked surface in [III]	Partly reproducible bipolar RS in [III]	$2/4$ in [III]	Up to 10^1 in [III]	Poor HRS/LRS retention; clear state drift observed in [III]	Cycling up to 10^4 observed, only selected junctions in [III]
Si-STO epi	Epitaxial; two GCMO phases in [III]	Bipolar RS in most junctions; anomalous/reversed polarity in [III]	$3/4$ in [III]	Up to 10^1 in [III]	HRS/LRS can remain discrete, but response depends on read delay in [III]	Cycling up to 10^4 observed, but timing-dependent in [III]
Si-STO	Poorly ordered or structurally deteriorated in [III]	No clear RS with the used device design in [III]	–	–	–	–
Si/SiO_2	Poorly ordered or structurally deteriorated in [III]	Poorly reproducible RS-like response in [III]	–	–	–	–
MgO	Polycrystalline; cracked surface in [III]	Consistent bipolar RS; volatile LRS; leaky-integrate behavior in [III, IV]	$4/4$ in [III]	Up to 10^2 in [III, IV]	LRS relaxation within 10 s in [IV]	Clear cycling up to 10^4 observed in [III]
MgO-buffered STO	GCMO structurally similar to MgO-grown in [IV]	Consistent bipolar RS; volatile LRS; leaky-integrate behavior in [IV]	Demo in [IV]	Up to 10^2 in [IV]	LRS relaxation, > 60 s in [IV]	Clear cycling observed, up to 10^4 in [IV]

conductivity, device architecture, or possible leakage paths to the substrate may also influence the observed electrical characteristics, and these effects are not investigated further here.

The films deposited on substrates or buffer layers with larger lattice mismatch, such as MgO, display diffraction patterns containing multiple crystallographic orientations, characteristic of polycrystalline films [III, IV] [101, 104]. The GCMO films grown on both MgO substrates and MgO-buffered STO are predominantly polycrystalline [III, IV]. The presence of grain boundaries and structural disorder introduces high-diffusivity pathways for oxygen ions, which facilitate rapid ionic relaxation once the external electric field is removed. As a result, these devices exhibit volatile resistive switching behavior [III, IV].

While the applied electric field drives oxygen ions across the metal-oxide interface to modulate the Schottky barrier height, the crystalline quality of the manganite film determines the stability of this modulation [28, 37, 106]. Polycrystalline growth introduces grain boundaries that may enable rapid back-diffusion of oxygen vacancies once the electric field is removed [28, 109, 110]. In such films, the concentration gradient overcomes the trapping potential of the lattice, leading to spontaneous relaxation and volatile switching behavior.

Looking at the RS performance metrics across these materials, the substrate-induced structure affects more than only the volatile or non-volatile character of

the switching. The clearest influence is observed in retention: STO-based textured films maintain distinguishable HRS and LRS states within the measured time frames, whereas polycrystalline or poorly crystalline films show stronger LRS relaxation, state drift, or inadequate reproducibility. The substrate also influences switching regularity and device-to-device variability, as seen from the poorer consistency of NGO, Si-STO, and Si devices. Endurance is less directly comparable between the different substrate sets because the device geometries and measurement protocols differ, but the available data suggest that clear cycling can be obtained both in STO-based non-volatile devices and in MgO/MgO-buffered volatile devices. These trends are summarized in Table 4.

These results demonstrate that the observed neuronal-like volatile dynamics are not governed solely by the electrode interface chemistry but are also influenced by the microstructure of the oxide film, including its crystallinity, texture, and possible grain-boundary-mediated diffusion pathways [III, IV]. By controlling substrate-induced strain and crystallinity through substrate selection and buffering, the device functionality can be tuned between synaptic (non-volatile) and neuronal (volatile) operating regimes [III, IV].

4.3.3 Leaky-Integrate Functionality

The intrinsic volatility observed in polycrystalline GCMO films, discussed in the previous section, enables the emulation of temporal signal integration, a fundamental computational primitive in spiking neural networks (SNNs) [140–143]. Unlike synaptic devices that store weights statically, neuronal elements must integrate incoming stimuli over time while relaxing towards a resting state in the absence of input [9, 83, 94]. This competition between excitation and spontaneous decay constitutes the leaky-integrate component of the leaky integrate-and-fire (LIF) neuron model.

To characterize this behavior within the constraints of the measurement setup, pulsed sequences are applied to MgO-substrate GCMO crosspoint devices with an active area of $40 \times 40\,\mu\mathrm{m}^2$, fabricated and electrically characterized by I. Angervo and L. Miettinen [IV], to probe the competition between field-driven excitation and intrinsic relaxation. The applied measurement sequences are presented in Fig. 24a and b. Unlike the standard pulsed IV protocol discussed earlier, these measurements do not sweep the device through a complete voltage loop during each cycle, but instead separate the SET-pulse integration step from the subsequent read/probe monitoring of relaxation. In the full reset protocol, each SET sequence is preceded by an IV RESET to establish the HRS baseline, followed by a train of SET pulses to modify conductance and read/probe pulses to monitor the state after each SET pulse; additional auxiliary pulses at V_{read} are included only to satisfy the pulse-program requirements of the measurement setup. In the cumulative protocol, the full IV RE-

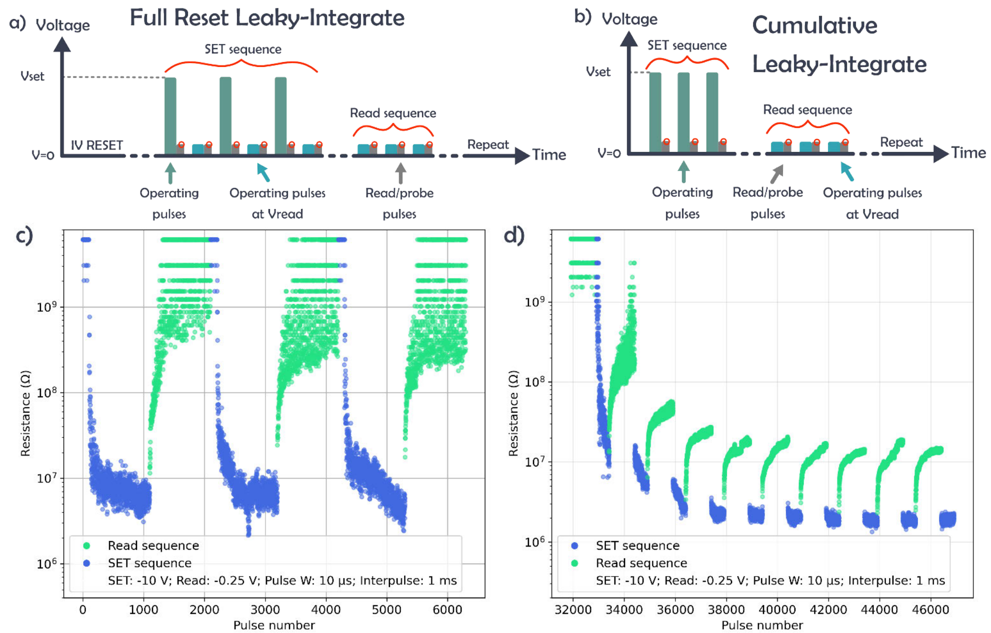

Figure 24. Pulse protocols and corresponding device-level leaky-integration dynamics in representative volatile GCMO memristors on an MgO substrate: an approximately 70 nm thick GCMO film contacted by 150 nm Al and 50 nm Au electrodes, with an active Al/GCMO interface area of $40 \times 40\,\mu\text{m}^2$. (a) Full-reset leaky-integration protocol. Each SET sequence is preceded by an IV RESET step to establish the HRS baseline. After an intermediate delay, each SET pulse is followed by a low-amplitude read/probe pulse. Additional auxiliary pulses at V_{read} included only to satisfy the pulse-program requirements of the measurement setup. The subsequent read sequence monitors relaxation of the programmed low-resistance state. (b) Cumulative leaky-integration protocol. The IV RESET step and the intermediate auxiliary pulses are omitted. The device is first driven by consecutive SET pulses, after which relaxation is monitored using read/probe pulses. (c, d) Corresponding resistance evolution measured using the protocols shown in panels (a, b), respectively. Measurements done with ArC ONE using negative SET pulses and low-amplitude read/probe pulses with a 2 ms read/probe pulse width. Repeated SET pulses decrease the resistance, corresponding to temporal integration, whereas the subsequent increase in resistance under read/probe conditions reflects spontaneous relaxation of the volatile low-resistance state. Panels (a, b) are redrawn schematics of the measurement protocols and panels (c, d) are redrawn measurement data from this work [IV].

SET and the intermediate auxiliary pulses between SET pulses are omitted, allowing the conductance to evolve cumulatively. As illustrated in Figure 24c and d, resistance evolution follows a characteristic pattern [IV]: the first SET pulse induces the largest drop, while subsequent pulses produce progressively smaller changes as the device approaches conductance saturation. This nonlinear saturation resembles membrane response dynamics, where stimulus impact depends on the instantaneous neuronal state. The two operation modes correspond to controlled baseline integration and cumulative temporal integration with memory of prior stimuli, both relevant for rate- and temporal-coding neuromorphic schemes. During the subsequent read sequences, resistance gradually increases towards the HRS baseline as oxygen vacancies back-diffuse under the concentration gradient [IV][31, 80].

The two operational modes demonstrate functional versatility: full reset baseline integration (Fig. 24a and c) and successive, cumulative state accumulation (Fig. 24b and d) [IV]. In the full reset mode, each pulse sequence is preceded by an IV RESET, ensuring a defined starting point and allowing systematic analysis of how SET parameters govern resistance change magnitude and leakage rate. In state-accumulation mode, the IV RESET is omitted, so each cycle begins from the residual conductance of the previous one, producing a temporal memory effect where device state reflects stimulus history balanced against continuous decay. Although a full circuit-level LIF neuron, including threshold-triggered spiking and autonomous reset, is beyond this work, the observed dynamics indicate the essential device-level temporal integration required for such architectures [IV][97].

The gradual drift of the low-resistance state towards a stable high-resistance state is commonly observed in volatile memristive devices and, in GCMO films, has been linked to crystallinity-dependent diffusion [III]. Similar findings in related oxides show that grain boundaries act as preferential oxygen diffusion pathways, accelerating relaxation [109, 133–135, 144]. This mechanism resembles ion-channel-mediated membrane potential decay in biological neurons, where ionic flux drives relaxation towards the resting state [145]. Memristive devices have therefore been widely investigated as compact artificial neuron components [98, 99, 140, 141, 146, 147]. Neuron spiking is often implemented by combining memristive switching with external circuit elements such as capacitive discharge in RC circuits [145] or by exploiting intrinsic memristor battery effects [146]. While complete neuron architectures require such circuit elements, this work documents the essential device-level temporal integration dynamics.

The same volatile relaxation dynamics may also be relevant for short-term synaptic memory. In this interpretation, the SET pulses temporarily potentiate the device conductance, while the subsequent spontaneous relaxation corresponds to forgetting or short-term plasticity rather than the leaky term of a neuronal element. Similar volatile memristive dynamics have been used to emulate short-term synaptic behavior, where conductance changes persist only over a limited time window before re-

laxing back towards the initial state [148, 149]. In the present GCMO devices, the same physical relaxation process can therefore be viewed either as the leaky term of a neuronal element or as short-term synaptic memory, depending on the circuit role assigned to the device.

These results indicate that polycrystalline GCMO films could provide a hardware platform for device-level temporal integration [IV][95, 96]. By leveraging grain-boundary-mediated relaxation, the device transitions from static memory to dynamic processing where the state depends on stimulus frequency [III, IV][150]. Thus, the transition between long-term synaptic memory, short-term synaptic memory, and neuronal-like dynamics is a tunable property governed by the oxide film's structural landscape, as well as the pulsing sequence. Importantly, this neuronal-like behavior emerges from the film's structural properties: grain-boundary diffusion pathways responsible for volatility originate from the polycrystalline growth mode induced by lattice mismatch, meaning substrate engineering provides a direct route for tuning device functionality between stable synaptic memory and dynamic neuronal processing [III, IV].

4.4 Neuromorphic Processors

The results presented in this chapter suggest that the oxidized Al/GCMO interface is not limited to a single mode of operation [II, IV]. By controlling the structural landscape of the GCMO film through substrate selection, we have realized a unified material system capable of emulating the two fundamental components of the biological brain: the synapse and the neuron [8, 83].

For synaptic applications, epitaxial GCMO films provide the non-volatile stability required for weight storage [I, II]. These devices have successfully emulated spike-timing-dependent plasticity [50] utilized in pulse-based learning rules. Beyond plasticity, these epitaxial films aim to satisfy the core requirements for high-density memory: multi-state conductance tuning, adequate retention, and high endurance [39, 84, 103]. These properties, combined with successful integration into crossbar arrays [I], provide a scalable foundation for networks that learn and retain information over time [15, 89].

Conversely, by introducing structural disorder via polycrystalline growth on MgO, the same interface transitions towards a neuronal element [IV]. These devices implement the leaky-integration discussed in the previous section, providing the temporal processing necessary for dynamic data handling [93, 95, 96]. The ability to sum incoming signals and spontaneously return to a resting state allows these artificial neuronal-like elements to process information in the time domain, mirroring the energy-efficient operation of biological spiking neurons [83, 151].

This dual functionality could significantly simplify the fabrication of neuromorphic processors [17]. By utilizing selective MgO buffering on STO substrates, or

conversely STO buffering on MgO, GCMO growth can be locally modified to exhibit volatile behavior within an otherwise non-volatile matrix [IV]. The polycrystalline, neuronal elements could be fabricated simultaneously with the epitaxial, synaptic-weight storing crossbar arrays [I, IV]. This spatial control of device kinetics is promising for the use in more complex neural circuits, combining memory and integration, without the need for heterogeneous material stacks [142, 152].

5 Conclusions

This thesis demonstrates that the resistive switching behavior in Al/$Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO)/Au devices is governed by a redox-active interfacial region located at the Al/GCMO interface. The chemical state and thickness of the oxidized Al-containing interfacial layer modulate the effective injection barrier, thereby controlling the observable resistance states. The XPS depth-profile comparison between HRS and LRS devices, together with the area-dependent resistance scaling, supports an interface-controlled mechanism rather than a purely localized filamentary model [II]. This is significant as many oxide-based memristors rely on the formation and rupture of stochastic conductive filaments, which can lead to variability in switching voltage, resistance state, and device-to-device behavior [10, 27, 29]. In contrast, the GCMO devices studied here follow the broader behavior of interface-type perovskite manganite memristors, where oxygen redistributes near the metal/oxide interface [28, 37, 41].

One main contribution of this work is the demonstration that the active interface and the crystalline microstructure of the GCMO film both affect the RS properties. Publications [I] and [II] establish the non-volatile, multistate, synaptic-like interface-controlled switching behavior of GCMO-based devices, when GCMO is grown epitaxially on $SrTiO_3$ (STO) substrates. These studies present crossbar-compatible operation, forming-free switching, area-dependent resistance states, and chemical evidence for the active interfacial AlO_x region. Publication [III] shows that substrate-induced differences in crystallinity affect the reproducibility, memory window, and stability of the switching response by exploring samples grown on varied substrates: $NdGaO_3$, STO-buffered Si, Si with native oxide, and MgO. Publication [IV] extends this structure–property relationship by confirming that polycrystalline GCMO films grown on MgO or MgO-buffered STO can exhibit volatile relaxation of the low-resistance state and device-level leaky-integrate behavior. Together, the publications included in this thesis illustrate that GCMO is not only a resistive switching material, but a structurally tunable platform whose dominant functionality can be shifted between synaptic-like memory and neuronal-like dynamics.

In common filamentary oxide memristors, large resistance windows are often achieved through localized conductive paths, but the stochastic nature of filament formation can complicate analog tuning and device uniformity [10, 29]. Interface-type perovskite manganite systems offer a more spatially distributed alternative,

Table 5. Comparison of representative manganite-based memristive devices reported in the literature with the GCMO devices studied in this thesis.

Manganite oxide	Electrodes	Geometry	HRS/ LRS	Endurance (cycles)	Volatility	Ref.
$Pr_{0.7}Ca_{0.3}MnO_3$; crystallinity not reported	W/Pt	Capacitor	10^2	$> 10^4$	Non-volatile	[153]
$Pr_{0.6}Ca_{0.4}MnO_3$; epitaxial/ highly textured	Al/Ag	Planar	10^3	$> 10^5$	Non-volatile	[154]
$La_{0.7}Ca_{0.3}MnO_3$; polycrystalline	2AgAl/Pt	Capacitor	2	$> 10^4$	Not reported	[155]
$La_{1/3}Ca_{2/3}MnO_3$; polycrystalline	Ag/Pt	Capacitor	300	$> 10^4$	Non-volatile	[156]
$Gd_{1-x}Ca_xMnO_3$; epitaxial/ highly textured	Al/Au	Planar	10^2	$> 10^5$	Non-volatile	[43]
$Gd_{0.2}Ca_{0.8}MnO_3$ on STO; epitaxial/ highly textured, this thesis	Al/Au	Lateral crosspoint	10^3	$> 10^5$	Non-volatile	[I, II, III, IV]
$Gd_{0.2}Ca_{0.8}MnO_3$ on MgO; polycrystalline, this thesis	Al/Au	Lateral crosspoint	10^2	$> 10^4$	Volatile	[III, IV]
$Gd_{0.2}Ca_{0.8}MnO_3$ on 7 nm MgO-buffered STO; polycrystalline, this thesis	Al/Au	Lateral crosspoint	10^2	$> 10^4$	Volatile	[IV]

where resistance is controlled by oxygen migration and interfacial barrier modulation [27, 37, 41]. Short-term plasticity and neuronal-like leakage have also been shown for oxide-based devices [141, 148]. To place the results of this thesis in the context of related manganite-based memristive devices, Table 5 compares representative literature examples with the GCMO devices studied in this thesis. Non-volatile STO-based GCMO devices reach HRS/LRS ratios and endurance values comparable to representative PCMO- and LCMO-based manganite memristors. In addition, the MgO-based and MgO-buffered GCMO devices provide volatile resistance dynamics, showing that substrate-controlled crystallinity can extend GCMO from non-volatile synaptic memory towards neuronal-like and short-term-memory functionality.

Several limitations remain. The long-term retention of the full set of intermediate resistance states has not yet been systematically measured, and accelerated retention testing has not been performed. Similarly, the coexistence of volatile and non-volatile regimes within a single device has not been fully mapped as a function of pulse amplitude, pulse width, pulse number, and read delay. Direct comparison of endurance and retention between all substrate types is also limited by differences in device geometry and measurement protocol. Future work should therefore focus on systematic pulse-parameter mapping, long-term and accelerated retention studies, improved device scaling, and integration strategies where epitaxial and polycrystalline GCMO regions could be deliberately combined on the same platform.

Overall, this thesis clarifies how structural quality, substrate-induced defects, and interfacial oxygen exchange jointly determine whether GCMO-based devices behave

as stable synaptic elements, short-term synaptic elements, or volatile neuronal elements. The work contributes new knowledge on the relationship between oxide film crystallinity and resistive switching dynamics, demonstrating that GCMO could function as a single-material platform for multiple neuromorphic device roles, depending on its structural form. This work lays the foundation for structurally engineered GCMO memristor architectures for future neuromorphic processors, in which synaptic memory arrays, short-term plasticity, and neuronal-like temporal integration can be designed through substrate selection, buffer-layer engineering, and programming protocols.

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