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Zahra Jahanshah Rad

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ABSTRACT

Semiconductors play an important role in our today's lives. Our societies could not operate normally without semiconductors. They are used in devices that form new infrastructures in our societies. Decades ago, a power outage was considered catastrophic while it had mainly local consequences. Today we are living in a world where a problem in a server could instantly affect the lives of people living on another continent. This is the motivation behind numerous research on semiconductors in academia and the industry. Due to the strategic role of the semiconductor industry, governments started to pour funding into this section and to pass legislation related to it such as European Chips Act. Many different areas are involved in the semiconductor industry, from mining and recycling raw materials to designing chips and circuits, building equipment used in production lines for making semiconductor device components, etc.

After the very first transistor made of Ge was built in 1947, the size of electronic and photovoltaic components made of semiconductors are constantly getting smaller following Moore's law, resulting in faster and more efficient devices, which are smaller, light weighted, and widely accessible and affordable. On the other hand, size reduction makes us facing what is called the "devil's invention" by Wolfgang Pauli: **surfaces**. By reducing the size of components, the role of the surface becomes more effective and important on the performance and properties of the devices. The surface part of a crystalline semiconductor compared to the bulk material beneath it naturally contains more defects, which cause electrical and optical losses in devices made of semiconductors.

This PhD thesis was dedicated to make possible improvements on the defect-rich surface of Si and GaAs semiconductors by using ultra-high vacuum (UHV) and chemical treatments. One target has been that the treatments studied are scalable and therefore could be utilized on an industrial scale. Further investigation was done by testing the effect of the above treatments on selected devices. The presented experimental results suggest that by applying UHV pre- and post-treatments on Si, defect density could be reduced and the minority carrier life-time could be increased. Also, reduction in leakage current in the devices made of Si after these surface treatments are reported. A simple wet chemical method for growing gallium oxide nanocrystals on the surface of GaAs was developed which could reduce surface losses in optoelectronics devices made of GaAs.

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TIIVISTELMÄ

Käytämme puolijohteita päivittäin moninaisissa sovelluksissa. Kasvava riippuvuus puolijohdelaitteista on motivoinut tutkijoita niin yliopistoissa kuin teollisuudessa kehittämään ratkaisuja erilaisiin tehtäviin lähtien raaka-aineiden louhinnasta ja kierrättämisestä, mikropiirien suunniteluun ja puolijohdelaitteiden valmistukseen sekä valmistuksessa tarvittavien prosessointilaitteiden valmistukseen esimerkiksi.

Sen jälkeen, kun ensimmäinen transistori oli demonstroitu laboratoriossa vuonna 1947, niiden ja monien muidenkin puolijohdekomponenttien kokoa on pyritty pienentämään, jotta ne saadaan pakattua pienempään tilaan, laitteista saadaan energiatehokkaampia, ja materiaalien kulutuksen kasvua pystytään hillitsemään. Tämä on johtanut erilaiseen haasteeseen: ongelmallisiin puolijohdepintoihin, joita Wolfgang Pauli kuvaili paholaisen keksinnöksi. Puolijohteiden pintakerroksien ominaisuudet poikkeavat merkittävästi verrattuna syvemmällä kiteessä olevaan ns. bulk-materiaaliin. Pinnat sisältävät suuren määrän kidevirheitä, jotka heikentävät puolijohdelaitteiden sähköistä ja optista toimintakykyä. Toisin sanoen puolijohdepinnat vaikuttavat sirujen energiatehokkuuteen ja käyttöikään sekä sirujen valmistusprosessin saantoon. Tämän väitöskirjan tavoite oli tutkia ja kehittää menetelmiä, joiden avulla puolijohdepintojen ongelmia pystytään korjaamaan. Puolijohteiksi valittiin pii (Si) ja galliumarsenidi (GaAs), joita molempia käytetään teollisuudessa. Eli Si- ja GaAs pinnat aiheuttavat ongelmia päivittäin käyttämissämme laitteissa. Tavoitteena oli myös se, että tutkittavat menetelmät olisivat skaalautuvia teollisuuteen ja pystyttäisiin liittämään nykyisiin valmistusprosesseihin.

Menetelmät perustuvat erittäin pienen taustakaasun eli avaruuden olosuhteita muistuttavan UHV-tekniikan (ultrahigh vacuum) hyödyntämiseen kemiallisissa liuoksissa tapahtuvien käsittelyiden kanssa. UHV:n yhdistämisen perinteisten käsittelyiden kanssa havaittiin pienentävän kidevirheiden tiheyttä pinnoilla, kuten varaustenkuljettajien elinikämittaukset ja kondensaattorien vuotovirtamittaukset osoittivat. Lisäksi GaAs-puolijohteen pinnan löydettiin muuttuvan mustaksi eli hyvin vähän valoa heijastavaksi, kun pinta käsiteltiin sopivasti vetyperoksidissa ja vedessä, mikä on erittäin yksinkertainen menetelmä GaAs-pintojen optisten häviöiden hallintaan. Materiaalien kemiallisten, rakenteellisten ja sähköisten ominaisuuksien mittauksissa hyödynnettiin Turun yliopiston moninaisia materiaalien karakterisointivälineitä sekä yhteistyökumppaneiden laitteita.

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I specifically appreciate the role of my supervisors Prof. Kalevi Kokko and Docent Pekka Laukkanen. My supervisor and research director, Prof. Kalevi Kokko was always available for discussions and providing me with insightful views. Docent Pekka Laukkanen was always supportive and above all, optimistic. His up-to-date and wide knowledge in the field was very helpful. I learned a lot from both of them, not only on science-related topics, but also on how to create a supportive, inclusive, and positive work environment by being respectful, patient, and open to criticism.

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During my PhD journey, I experienced difficulties resulting from different crises. COVID pandemic and lockdown, Russia's attack on Ukraine, and the Woman-Life-Freedom movement in Iran. They all impacted me as many others. I was lucky to have Goopi, Fetch and Atefeh by my side during the difficult times.

Goopi was my best friend and the source of infinite emotional support for me for more than 17 years, but I lost him and I feel this loss every day. His memory will stay with me for the rest of my life. I am grateful for the support of Zoe and Roshanak during the difficult days I had after Goopi. I would like to thank my mother as an empowered woman, my sister Roya, and last but not least my brother Pooria, with whom I had the best memories of my childhood and joy and happiness in adulthood.

During the Woman-Life-Freedom movement in Iran, the moments of viral videos showing brutal suppression of a peaceful movement aimed at human rights were shocking and affected my life. I would like to dedicate my thesis to all the brave women and men who suffered during the Woman-Life Freedom movement, and specifically to Mahsa Jina Amini, Kian Pirfalak, and Sepideh Rashnu. Mahsa Jina Amini was murdered under arrest of the morality police. Kian Pirfalak, and Sepideh Rashno were both interested in learning, but the former was shot dead when passing by a demonstration and the latter was banned from her education at the university and was sentenced to prison for resisting against compulsory Hijab.

31.05.2025
Zahra Jahanshah Rad

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Abbreviations

AI	artificial intelligence
ALD	atomic layer deposition
ARC	anti-reflection coating
BSE	back-scattered electron
BSF	back surface field
CIGS	$CuInGaSe_2$
CIS	$CuInSe_2$
CMOS	complementary metal–oxide–semiconductor
COCOS	corona-oxide characterization of semiconductors
CVD	chemical vapor deposition
CZ	Czochralski
EDS	energy-dispersive x-ray spectroscopy
EQE	external quantum efficiency
ESCA	electron spectroscopy for chemical analysis
ETD	Everhart-Thornley detector
FF	fill factor
GI-SXRD	grazing incidence synchrotron X-ray diffraction
GI-XRD	grazing incidence X-Ray diffraction
HEMT	high electron mobility transistor
HF	hydrofluoric acid
HHP	hot hydrogen peroxide
HV	high vacuum
HW	hot water
IBS	ion beam sputtering
IC	integrated circuit
LED	light-emitting diode
LEED	low-energy electron diffraction

LT-UHV	low temperature ultrahigh vacuum
MBE	molecular-beam-epitaxy
MEMS	microelectromechanical systems
MOS	metal-oxide-semiconductor
MOSCap	metal oxide semiconductor capacitor
MOSFET	metal oxide semiconductor capacitor
PC	personal computer
PECVD	plasma enhanced chemical vapor deposition
PL	photoluminescence
PV	photovoltaic
QW	quantum-well
R2B	Research to Business
RCA	Radio Corporation of America
RGA	residual gas analyser
RTA	rapid thermal annealing
SC	standard clean
SE	secondary electron
SEM	scanning electron microscopy
SI	semi-insulating
STM	scanning tunneling microscopy
STS	scanning tunneling spectroscopy
TDMAH	tetrakis-dimethylamido hafnium
TEM	transmission electron microscopy
TMA	trimethylaluminum
UHV	ultra-high vacuum
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

List of Original Publications

The following publications are included into this thesis and they will be referred to with Roman numbers within this thesis. The original publications have been reproduced with the permission of the copyright holders.

I Z. Jahanshah Rad, J.-P. Lehtiö, I. Mack, K.Rosta, K. Chen, V. Vähänissi, M. Punkkinen, R. Punkkinen, H-P. Hedman, A. Pavlov, M. Kuzmin, H. Savin, P. Laukkanen, K. Kokko.
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1 Introduction

1.1 Semiconductors

Semiconductors play a vital role in our today's life. They could be considered as the raw material for the new infrastructures of our societies (Fig.1). It is not exaggeration to claim that semiconductors in our today's life play the same role as crude oil in the previous century. Without semiconductors, we would not have efficient communication, personal computer (PC) s, smart phones, the internet, solar cells, data centers, artificial intelligence (AI), etc.

Materials could be categorized into three groups based on their band diagrams of electron levels: metals, insulators, and semiconductors. As the name suggests, semiconductors are not conductors or insulators. They are in between. An intrinsic semiconductor does not have free charge carriers at 0 K, but when the condition is changed (e.g. temperature, doping), they can behave as a conductor. A semiconductor has a band gap that is smaller than that of insulators ($5 - 10\ eV$) [8], yet they are not insulator since they have a band gap between valence band maximum and conduction band minimum smaller than that of insulators (Fig. 2).

As mentioned above, by changing the temperature of a semiconductor or by doping it with donor or acceptor elements, the conductivity of a semiconductor could be changed. In an intrinsic (i.e. non-doped) semiconductor, the carrier concentration is:

$$n_i(T) = 2(\frac{2\pi kT}{h^2})^{3/2}(m_n^* m_p^*)^{3/4} e^{\frac{-(E_g)}{2kT}}, \tag{1}$$

where , k is the Boltzmann constant, T is the absolute temperature, h is the Planck constant, m_n^* and m_p^* are density of states effective mass of electrons and holes respectively, and E_g is the band gap energy of the semiconductor. This equation shows the dependence of the intrinsic carrier concentration on the temperature and the band gap.

The electron and hole concentration at equilibrium, n_0 and p_0, respectively, are obtained by:

$$\begin{aligned} n_0 &= n_i e^{(E_F - E_i)/kT}, \\ p_0 &= n_i e^{(E_i - E_F)/kT}, \end{aligned} \tag{2}$$

Figure 1. Infrastructures of our today's life. On top, bridges, damns, roads, power plants and below new infrastructures including data centers, smart-phones, solar power plants. (Figures taken from [1; 2; 3; 4; 5; 6; 7])

where n_i is the intrinsic concentration of electron-hole pairs, which is calculated from equation 1 at a given temperature, E_F is the Fermi level of the doped semiconductor, E_i is the Fermi level of the intrinsic semiconductor, k is the Boltzmann constant, and T is the absolute temperature.

All the magical properties of semiconductors lie into the nature of electronic band structures. They can amplify signals or work as a switch, either between an on-off state or as a converter between electricity and light. A transistor could be considered as a switch, a solar cell as a light to electricity converter, and a light-emitting diode (LED) as an electricity to light converter, respectively.

Switching between an on-off state is a key feature in semiconductor structures which is the same key element in computing as well. When there is current flowing in the device, it is considered as 1 and when not as 0. The one and zero are the units of computation. This similarity is not a coincidence, in fact semiconductors were used in computers because of this feature they have.

In 2024, for the first time pictures of the computer used in the second world war by the UK to break the codes of Nazi messages were published [9], however, the first transistor made of a semiconductor was built in Bell Laboratories in 1947. Before semiconductor transistors, vacuum tubes were used as switches for computing. They were expensive, large, and used a lot of power to provide small computing capacity

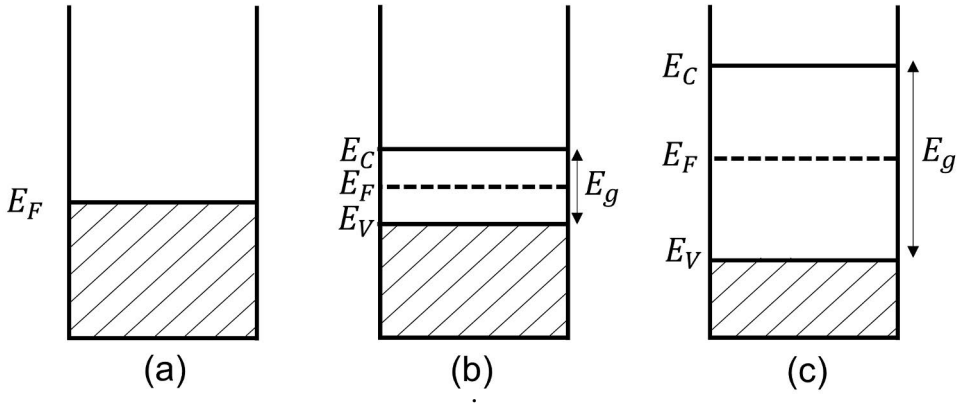

Figure 2. Difference between band diagrams of electron energy in (a) Metals, (b) semiconductors, and (c) insulators.

in return. On the other hand, semiconductors consume less power and could provide much more computation power with a smaller size and lower power consumption.

In another categorization, materials could be considered as amorphous, polycrystalline, and crystalline. Except in some exceptions, high-quality crystals are required in semiconductor device manufacturing [10; 11; 12; 13]. It is worth mentioning that polycrystalline materials are finding their application in the semiconductor industry, for example in communication) [14; 15]. Most semiconductors used in device fabrication are crystalline. Semiconductors could be categorized as elemental and compound depending on whether they are formed of only one element or more than one element, respectively.

In this thesis, two semiconductors were investigated: Si (elemental) and GaAs (III-V compound). In this thesis different devices including metal oxide semiconductor capacitor (MOSCap) s, solar cells, and Schottky detectors were investigated. In this chapter, the properties of the studied semiconductors and the structure of MOSCaps and solar cells are explained. At the end of this chapter the possibility of utilizing UHV processes in semiconductor production lines is discussed.

1.1.1 Silicon

Silicon is an elemental semiconductor and is the most widely used semiconductor in the industry. Although the first semiconductor device was a transistor made of Ge in 1947 [16], after that devices were mainly made of Si, like the first planar integrated circuit (IC) built in 1959 which was made of Si [17]. One of the main reasons for Si being the main material in semiconductor industry is its cheap price and wide availability, and that the rust of silicon: SiO_2 works surprisingly well as a natural insulating layer in applications.

Si has an indirect band gap of 1.12 eV and has a diamond crystal structure (Fig. 3) with the cubic lattice constant of 5.43 Å[18]. One of the main methods used to grow single crystalline Si is the Czochralski (CZ) method [19; 20]. It is worth mentioning that the silicon used in solar cells is solar grade silicon which is produced by a modified CZ method that produces a Si sheet rather than a Si ingot which must be cut and polished to make Si wafers [21]. By this method a thinner silicon wafer could be produced and there is less material waste because there is no need for cutting the ingot. Solar grade silicon is different from prime grade silicon and Si wafers that are used in e.g. chips.

Si is used in many different devices such as solar cells, transistors, processing and memory chips, photodetectors, particle detectors, microelectromechanical systems (MEMS), etc. In most of these applications, the Si surface is covered with a thin layer of amorphous silicon oxide because the cleaned and oxide-free Si surface is difficult to retain during device manufacturing. The interface between the amorphous silicon oxide layer with the crystalline Si beneath introduces interface defect states (see. Fig. 4) that will affect the performance of the device, for example, in MOSCaps, as discussed in Sec.1.2.1.

1.1.2 Gallium arsenide

Gallium arsenide is a III-V compound semiconductor with direct band gap of 1.42 eV and has a zincblende crystal structure (Fig. 5) with a cubic lattice constant of 5.65 Å [18]. GaAs has higher electron mobility (almost six times higher than Si [8]) and a band gap larger than that of Si making it a suitable material for high-speed and high-frequency devices such as high electron mobility transistor (HEMT)s [23]. In addition, unlike silicon, GaAs has a direct band gap, facilitating its use in photonics.

GaAs is used in e.g. semiconductor lasers, LEDs, solar cells, Schottky detectors, [20; 8].

1.2 Semiconductor devices

Different devices were made and measured in house or in collaboration of which the results are included in this thesis.These devices are investigated here.

1.2.1 MOS capacitors

Fig. 6 shows MOSCap and metal oxide semiconductor field effect transistor (MOSFET) structures schematically. In this figure, it can be seen that the interface between silicon surface and the insulator exists in both structures. Thus, methods that result in the reduction of the defect density in this interface and the leakage current of a MOSCap structure could be considered to be applicable to MOSFET and comple-

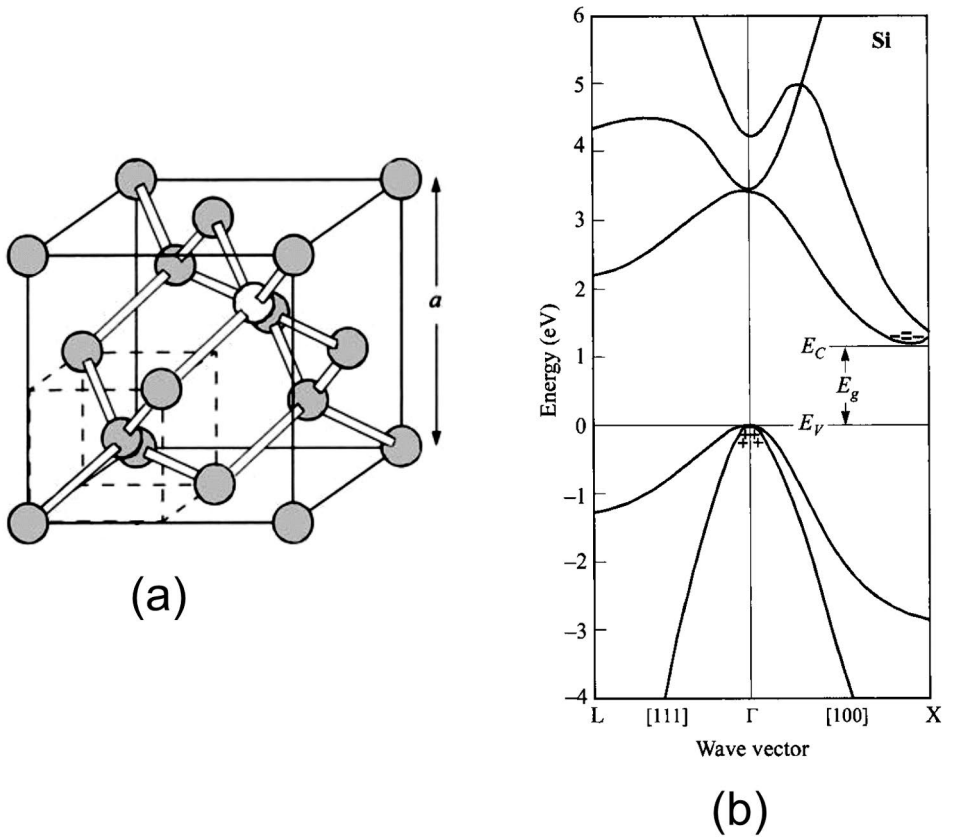

Figure 3. (a) Diamond structure of crystalline Si and (b) energy band structure of Si showing an indirect band gap [22].

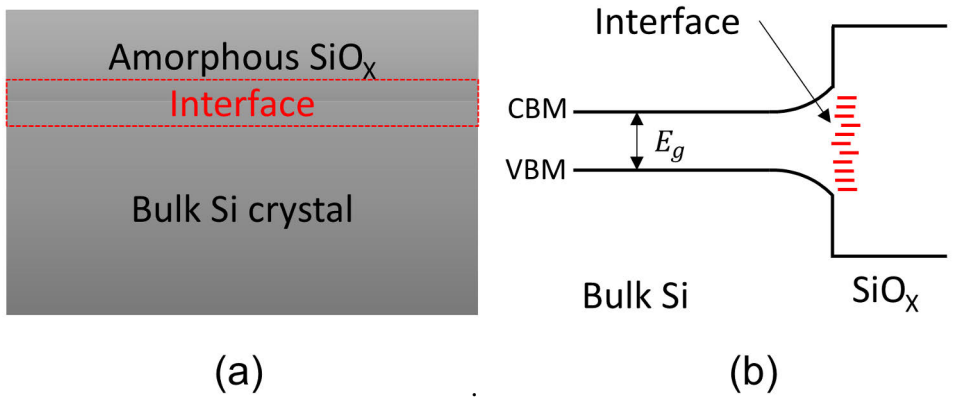

Figure 4. (a) Schematic interface between bulk Si and amorphous SiO_x and (b) band diagram of the structure. CBM and CVM are conduction band minimum and valence band maximum respectively. [22].

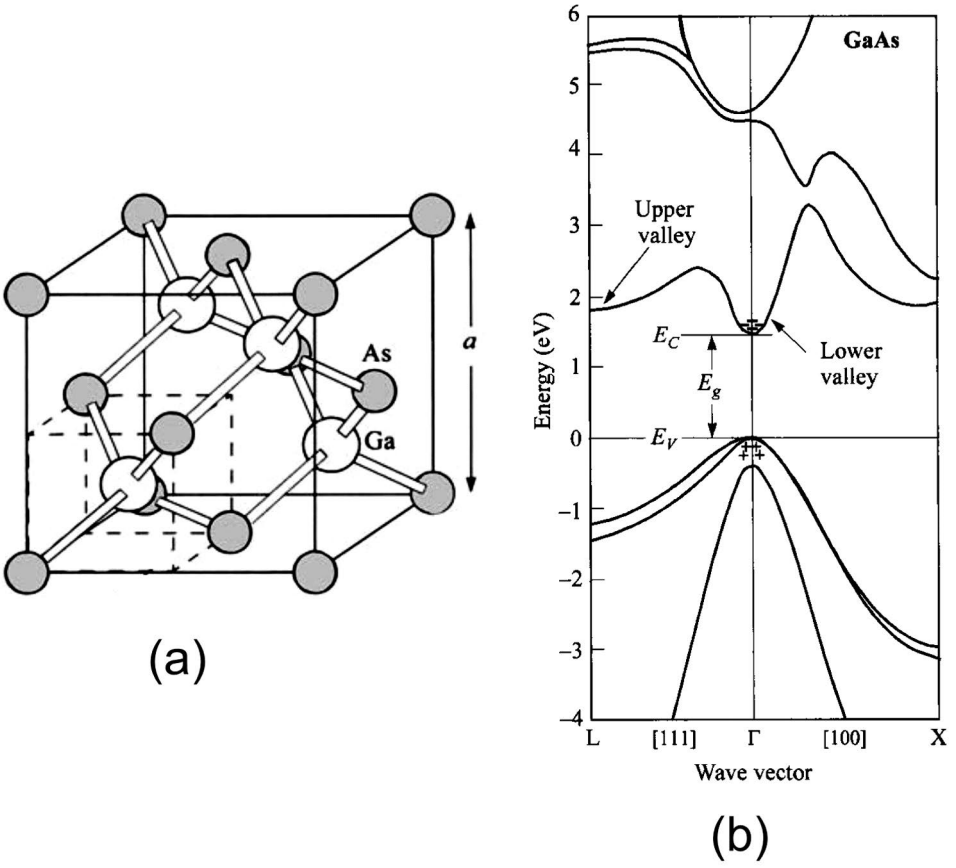

Figure 5. (a) Zincblende structure of crystalline GaAs and (b) energy band structure of GaAs showing a direct band gap [22].

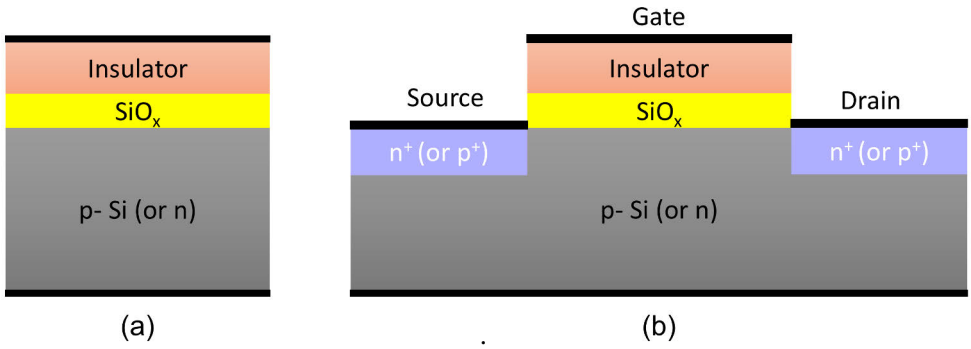

Figure 6. Schematic structure of (a) MOSCap and (b) n (or p) MOSFET.In both structures the interface between Si-Si oxide could be seen in yellow (not in scale). Black lines indicate metal contacts.

mentary metal–oxide–semiconductor (CMOS) structures as well. Power consumption in these structures could be categorized as on- and off-state power consumption, referring to power consumption when the device is in on or off state, respectively. The off-state or static power consumption originates from leakage current, which increases total power consumption. The off-state power consumption originates partially from the interface defects between silicon surface and the insulating layer [24; 25; 26]. These defects have a greater effect on the leakage current when the size of the devices containing these structures shrinks. Given the fact that MOSFET and CMOS are used in memory and logic chips [27], which are widely used in many devices, and the fact that the size of these structures is becoming smaller down to *nm* scale, the off-state or static power consumption role becomes more important [28; 29; 30; 31]. For this reason, MOSCaps were fabricated by the methods explained in Sec.s 2.4 and 2.5.4 to investigate possible methods for decreasing defect density and leakage current in them. Fig. 7 shows energy band diagram of a p-type MOSCap showing accumulation, depletion, and inversion conditions. The leakage current can increase through the oxide because of defect levels in the interface and insulator side shown in this figure. Also, these interface defects increase leakage via the so-called gate-induced drain leakage, which means that electrons from silicon valence band can move more easily to the conduction band via thermal excitation, after which the moved electrons increase in fact off-state leakage between drain and source. Different methods have been used to improve Si-Silicon oxide interface by reducing the amount of carbon contamination, interface defect density and leakage current for example by annealing these interfaces at different temperatures and different gases [32; 33; 34; 35; 26; 36]. In this thesis, the interface between Si and Si oxide in MOSCap structure was investigated. The motivation behind the study was to reduce the amount of interface defect density induced by silicon sub-oxides (SiO_x) to reduce the off-state leakage current. In this study two methods were in-

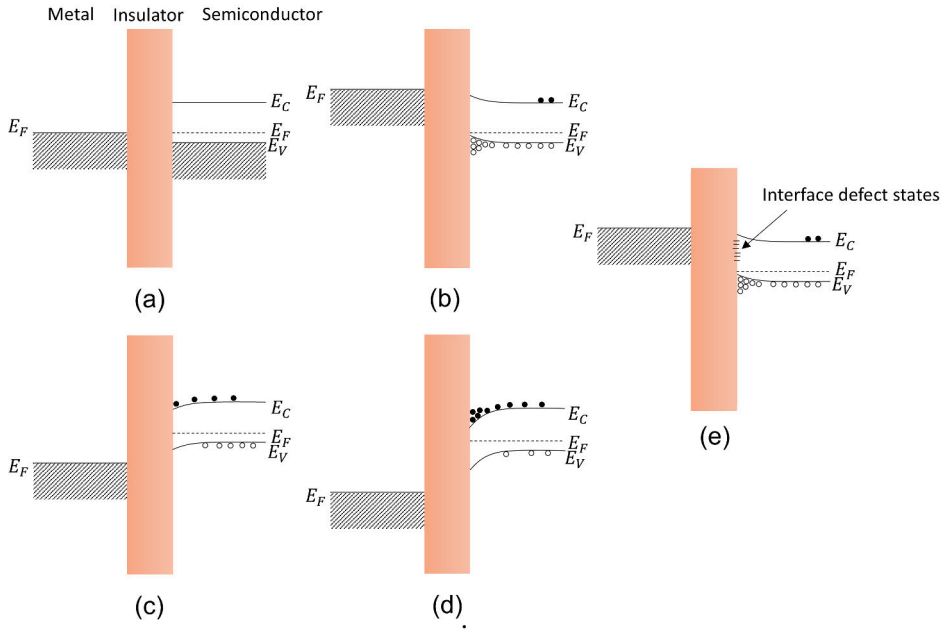

Figure 7. Energy band diagram of a p-type MOSCap under (a) zero bias ($V = 0$), (b) $V < 0$ and accumulation, (c) $V > 0$ and depletion, and (d) $V > 0$ and inversion, (e) interface defect states.

vestigated: growing a crystalline silicon oxide layer on top of clean silicon surface by UHV heating and controlled oxidation or by modifying chemically grown silicon oxide layer on silicon by UHV heating and oxidation prior to atomic layer deposition (ALD) (see Fig. 23).

1.2.2 Solar cells

Solar cells are photovoltaic devices that convert light to electricity. Different types of solar cells have been developed that could be categorized based on the used material in fabricating the cell or the cell structure.

A solar cell could be considered as a simple p-n junction When incident photon interacts with a semiconductor, electron-hole is created in the semiconductor and by collecting these carriers, electricity could be produced. For solar cells, wide spectral response over a broad solar wavelength is required. For an incident photon to contribute to photo-current, the energy $h\nu$ of photon must be higher than the semiconductor band gap (E_g). In this case, the energy of photon which is equal to E_g creates electron-hole and the rest of its energy is wasted as heat.

Challenges related to solar cells to improve their efficiency are related to collecting as many photons as possible (by reducing reflection), converting as many absorbed photons to electron-holes as possible (using multi-junction solar cells for example), and eventually collecting as many created electric carries as possible (for example solar cells with back surface field (BSF) layer). Semiconductor surface plays a key role in these challenges, where the oxide-semiconductor interface in anti-reflection coating (ARC) area affects guiding light to the solar cell efficiently and guiding electric carriers toward metal contacts, and where the metal-semiconductor interface affects the transfer of carriers to an external circuit.

In addition to efficiency, low production cost, reliability, and sustainable production methods and materials are important in manufacturing solar cells. The most important parameter in a solar cell is efficiency, which is calculated from:

$$\eta = \frac{P_m}{P_{in}}, \tag{3}$$

where P_m is the maximum output power and P_{in} is the incident power. P_{in} is known in the experiment setup for measuring current-voltage behaviour of a solar cell under illumination. Maximum power (P_m) could be calculated from the I-V curve of a solar cell under illumination.

Another parameter which is important in solar cells is Fill Factor (FF), which shows the sharpness of the I-V curve under illumination and is defined by:

$$FF = \frac{I_m V_m}{I_{sc} V_{oc}}, \tag{4}$$

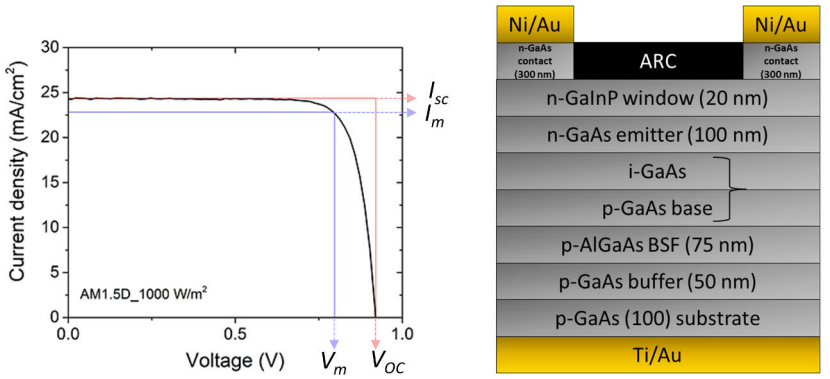

Figure 8. (a) I-V curve of a solar cell under illumination with IBS grown ARC, (b) the structure of the measured solar cell.

where I_m and V_m are current and voltage at maximum power, respectively, I_{sc} is the short circuit current, and V_{oc} is the open circuit voltage. Fig. 8 shows a typical I-V curve of a solar cell under illumination where I_{sc}, V_{oc}, FF, and P_m are shown in it. The structure of this cell is shown in the same figure. This cell had ARC grown on it using ion beam sputtering (IBS) method. The good FF for a solar cell is around 80% [37]. The efficiency of this solar cell is 18. 2% and its FF is 81%. Other methods have been utilized in this thesis to create ARC on the solar cell structure shown in Fig. 8 including plasma enhanced chemical vapor deposition (PECVD), IBS, and making black GaAs layer on top of the structure by wet chemical treatments.

Different materials have been utilized, and different device structures have been designed for solar cells mainly to increase the efficiency of cells. Silicon is the mostly used material in solar cells industry, however, other materials have been studied and developed, e.g., CdTe, CdS, $CuInSe_2$ (CIS), $CuInGaSe_2$ (CIGS), and perovskite. [38; 21; 37; 39; 40; 41]

These materials provide new possibilities to make cheaper solar cells but have instability problems. Solar cells are used in terrestrial and space applications (e.g. satellites). Fig. 9 shows the projected market for solar cells based on the material. It could be seen that Si will have the largest market share even though its efficiency is lower compared to that of GaAs solar cells. The reason is cheaper, faster, and more scalable production and lower raw material cost compared to GaAs. In specific applications where efficiency is vital (such as space applications), toxic and more expensive materials such as GaAs are utilized.

ARCs have been utilized to reduce reflection on the surface of the solar cell. Different methods are used to make broad band ARC layers on solar cells [43] like PECVD and IBS [44; 45; 46; 47]. Also, texturizing the surface causes the reflected

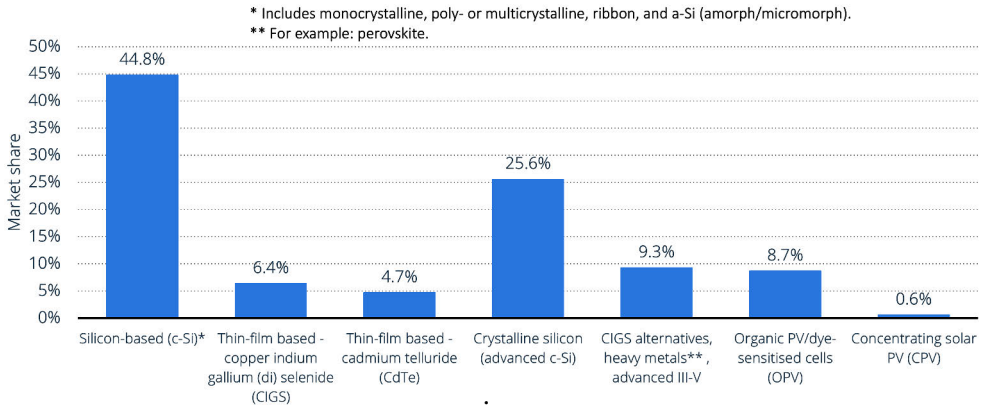

Figure 9. Projected market share of solar photovoltaic (PV) panels worldwide in 2030 by technology. [42]

light being reflected back to the cell by texturized structure [47; 48; 49] In the last article included in this thesis, a patented method is utilized to reduce the reflection on the surface of GaAs by a two step wet chemical method.

1.3 Utilization of ultra-high vacuum processes in surface science and silicon industry

Defects and contaminants are big problems in semiconductor industry affecting the production yield, device reliability and durability, electrical, and optical properties of the produced devices [50; 51; 33; 52; 53]. Interestingly, the source, effect, and acceptable level of contaminants and defects have changed over time. In the early days of the semiconductor industry, the devices were larger (compared to today), and so the effective contamination source was particles in the air, which affected the chips made on Si wafers. An effective solution to the high particle level was to take the fabrication process to clean rooms.

Since then, different solutions have been established and developed to fulfill the industry demands for reducing the amount of defects and contaminants and consequently increasing the production yield. Examples of these methods are wet chemical cleaning procedures such as Radio Corporation of America (RCA), gettering, using different high purity chemicals and gases, and different annealing steps [54; 55; 56; 57; 58; 59; 8]. These methods are used in production lines as they are considered scalable and provide low enough level of contamination and defects required by industry demands.

As components made of semiconductors are getting smaller, the source of effective contamination is shifted from particles to atomic scale defects which are affecting the production yield, and devices quality [60; 61; 53; 62]. For this reason,

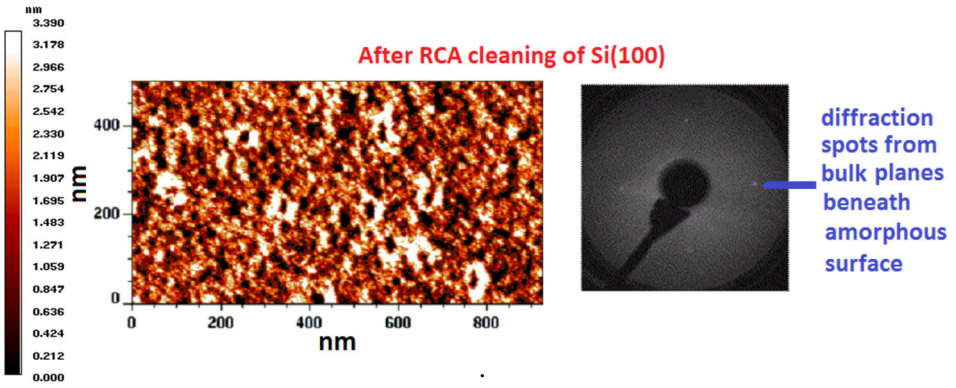

Figure 10. STM image and LEED pattern of a Si surface cleaned by RCA method with last step HF dip showing that the surface is not smooth or crystalline. The height variation in this image is 3.39 nm. [64]

different methods in the industry are utilized to reduce the amount of defects such as annealing in different gas environments with different pressures and temperatures, plasma cleaning, etc. [63].

When the device size shrinks, the role of the surface becomes more important in device operation, while the surface of a crystalline semiconductor is problematic in its nature. When a surface is created on a bulk crystal, it means that the bonds between atoms are broken on the surface. These broken (dangling) bonds have high energy that should be minimized. When the fresh cut semiconductor surface is in air, different molecules are available in air to help the semiconductor reducing its surface energy, including oxygen and carbon. This process results in carbon contamination and defect rich amorphous silicon oxide layer on top of crystalline bulk Si. These contaminants and defects will be buried under any next layer grown on the semiconductor which could be an insulator or metallic layer. This is expected to happen in Si device manufacturing lines, where processing steps are done in ambient conditions. It is worth mentioning that a defect-rich and contaminated Si surface is created on the side walls of Si when devices/chips are diced from a processed wafer.

These contaminants and atomic-level defects are present on the surface of Si when it is processed within the device fabrication steps while the surface is considered "clean" after different cleaning steps. Fig. 10 shows low-energy electron diffraction (LEED), and scanning tunneling microscopy (STM) of a Si surface after it is cleaned by the RCA wet chemical cleaning method followed by hydrofluoric acid (HF) dip. This surface is considered clean enough to be further processed in the fabrication line, while it could be seen from these figures that the surface is not crystalline or atomically smooth, which imposes defects on the surface because a disordered material naturally includes many point defects.

These atomic scale defects on the surface are well known, investigated, and re-

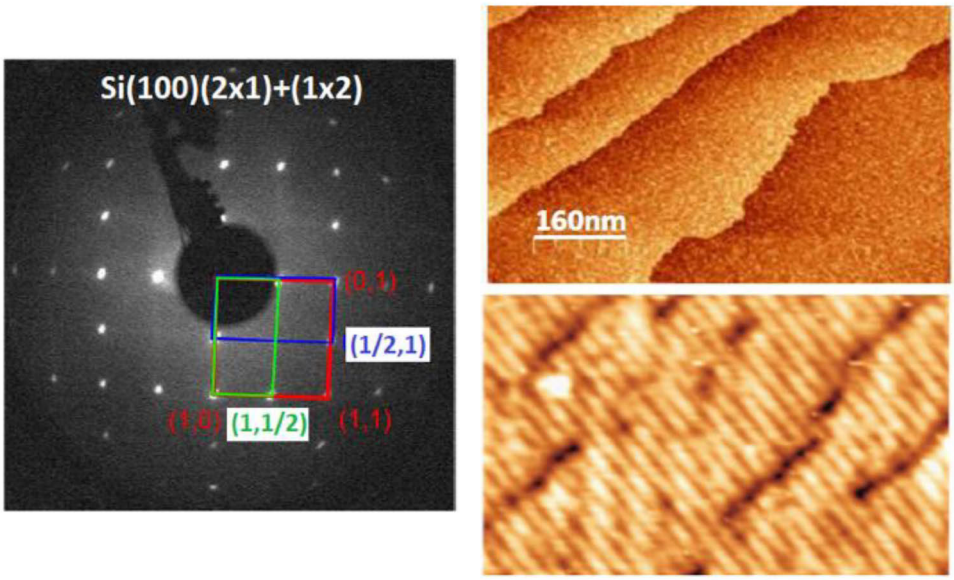

Figure 11. STM image and LEED pattern of a Si surface cleaned by UHV flash heating method. The surface is atomically smooth and crystalline. Reprinted with permission from paper I, ACS Appl. Mater. Interfaces 2020, 12, 46933-46941. Copyright 2020 American Chemical Society.

duced in surface science laboratories where the Si surface is cleaned by the so-called UHV flash heating. In this method, a small piece of Si is heated up to 1200-1300 °C multiple times and kept at that temperature for a very short time [65; 64; 66], resulting in a contamination-free, crystalline and atomically smooth Si surface. Fig. 11 shows LEED, and STM of a UHV flash heated Si surface where the surface is atomically smooth and crystalline. The key element in this method is that it is done under UHV condition, which prevents oxidation and contamination of the surface and results in a crystalline surface reconstruction.

By comparing Figs. 10 and 11 one can see the difference between a crystalline and smooth silicon surface with less surface defects and a wet chemically cleaned surface lacking atomic-level smoothness and crystalline structure.

Based on the above discussion, it seems that the "cleanliness" of the silicon surface needs to be clarified and even redefined. For example should cleanliness include also a crystalline degree? Furthermore, it is clear that most of surface oxides can be removed in simple way by a proper wet chemical immersion, but what is a maximum allowed oxygen or carbon density, e.g. $10^{10}\ cm^{-2}$ or $10^{12}\ cm^{-2}$. As the size of devices made of Si are getting smaller, reducing the atomic scale defects on silicon surface by having crystalline and smooth surface becomes more important. Decades ago, clean was defined based on the requirements related to the size of devices, now,

this requirement demands Si surface cleaning on atomic scale when the device size is reduced to below 20 *nm* [67].

Since vacuum and high vacuum (HV) processes have been used in silicon industry in different processing steps, e.g. ALD, chemical vapor deposition (CVD), and rapid thermal annealing (RTA), one could argue that these processing steps already provide a clean environment to prevent Si surface from being contaminated and oxidized in an uncontrolled way during processing steps. However, according to the basic vacuum technology result,

$$F = \frac{2.635 \times P}{\sqrt{MT}}, \tag{5}$$

where F is the number of molecules striking the surface $[cm^{-2}.s^{-1}]$, P is pressure $[mbar]$, M is molar mass $[g.mol^{-1}]$, and T is temperature $[K]$, Si surface will be covered with a monolayer of contamination within seconds in HV condition. Even under UHV condition the surface will not remain intact for a long time, as it takes hours for the Si surface to be covered with oxygen and contaminants. Therefore, the methods mentioned above, which are utilized in the current Si industry, cannot provide a clean enough environment that provides more time to keep a surface clean and control the atomic structure of the surface, although an inert background gas would be used.

Given the Si industry requirement to reduce the amount of defects on atomic scale, it could be perfect timing for Si industry to integrate UHV process and environment into production lines to improve yield and device quality.

In this thesis, the use of UHV heating and oxidation is shown to reduce the interface defect density and leakage current in Si-Si oxide interface. Other reports also show the benefits of utilizing UHV in Si device fabrication processes [68**?**]. Furthermore, it is shown in this thesis that applying UHV heating and oxidation could be done not only on small pieces of silicon, but also on silicon wafers. This paves the way to utilize this method on industrial scale and to bridge between methods used in surface science laboratories and industrial processes.

2 Experiments

2.1 Summary of experiments

In total more than 300 samples were prepared for experiments related to the results presented in this thesis. Among the samples, 30 were full and half wafers, and 200 were small surface science samples. A UHV system for processing silicon wafers with 100 mm diameter was designed, assembled, and calibrated in this work.

Collaborations with different research groups within the University of Turku (Department of Computing and Department of Chemistry), Aalto University (Department of Electronics and Nanoengineering), Tampere University of Technology (Optoelectronics Research Center), University of Oulu (Nano and Molecular Systems Research Unit), Raja Ramanna Center for Advanced Technology (Synchrotrons Utilization Section), and University of Tartu (Institute of Physics) were established for preparing and characterization of samples. In addition, device tests were performed on ready devices from different companies.

Considering the size, the samples used within this thesis could be categorized into three different groups:

- Surface science samples with size of $6 \times 12\ mm^2$, which are compatible with Omicron sample holders used in the systems explained in the Sec. 2.2.
- Full and half wafers of Si with diameter of 100 mm, which were processed in the system explained in Sec.2.3.
- Small devices with miscellaneous size, which could not be mounted on the Omicron sample holders were processed in the system explained in Sec. 2.3 using a buffer Si wafer.

2.2 Ultra-high vacuum (UHV) system

UHV systems are widely utilized in surface science as they provide an environment with less amount of contamination compared to ambient condition, possibility to do controlled processes such as oxidation, gas exposure, and deposition in addition to long mean free path for particles used in the surface analysis.

In the experiments of this thesis, a UHV multichamber system was used to process $6 \times 12\ mm^2$ samples which are compatible with the Omicron sample holders used in the system. A sample is mounted on this sample holder using clamps, which

makes the sample transfer possible inside the UHV chamber. The system and its schematic are shown in Fig. 12. The system has three chambers with independent pumping systems, and each chamber is separated from the rest of the system with a gate valve. This system is connected to an ALD (see Sec.2.4) unit through a gate valve, which enables the in-situ ALD growth on the samples after being processed in the UHV system. The three chambers of this system are:

- **Load-lock chamber**: used for inserting samples into and taking them out from the system while the rest of the system is still under pumping and within UHV pressure range.
- **Preparation chamber**: used for preparing the samples. This chamber is equipped with different thermal evaporation sources used for depositing thin layers on the surface of samples. Different gas lines (oxygen, hydrogen, and ammonia) are connected to this chamber that could be used for gas exposure in preparation chamber or analysis chamber when the gate valve between these two chambers is closed and opened respectively. Indirect current heating of the sample is possible in this chamber. The pressure within this chamber is in the range of 10^{-10} mbar.
- **Analysis chamber**: used for characterization of the surface of samples. It has the same pumps and pressure gauge as the preparation chamber. This chamber is equipped with X-ray photoelectron spectroscopy (XPS), LEED, and STM/scanning tunneling spectroscopy (STS) characterization systems. Direct and indirect current heating, and Ar ion sputtering could be performed within this chamber. Gas exposure could be performed within this chamber by opening the gate valve between this chamber and preparation chamber and using gas inlet lines connected to the preparation chamber. The pressure within this chamber is in the range of 10^{-12} mbar

Each of these chambers are connected to an independent compression pumping system which is a Turbomolecular pump connected to a Rotary vane backing pump. In addition, each of the preparation and analysis chambers are connected to an entrapment pump which is an ion pump. The load-lock chamber has no vacuum gauge, while the preparation and analysis chambers have their own hot cathode ionization gauges and independent controllers for these gauges.

2.3 Scaling up ultra-high vacuum (UHV) system for processing Si wafers

Utilization of HV systems are well established in the semiconductor industry. For example in metal deposition to form metal contacts, ALD systems for depositing insulating layers on semiconductors, RTA, and CVD systems. Also, UHV systems are in some specific applications such as molecular-beam-epitaxy (MBE), however, utilizing UHV systems for silicon is not established in the semiconductor industry as

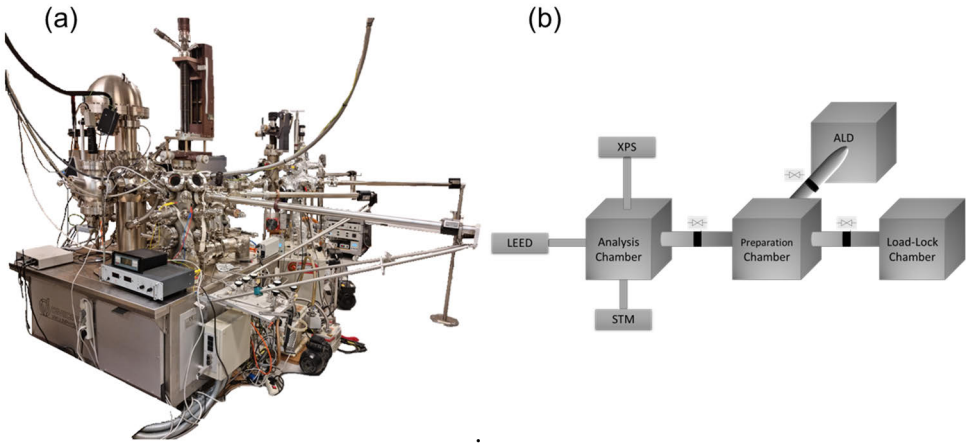

Figure 12. (a) UHV system used in the experiments and (b) schematic of the system.

pre- and post- treatments studied within this thesis.

As described in Sec. 2.2, the size of the samples used in the surface science experiments is $6 \times 12\ mm^2$, while in the silicon industry, samples are wafers with minimum size of 100 mm diameter. Silicon industry is shifting towards larger size of wafers with diameter of 150 mm, 200 mm, 250 mm, and 300 mm to increase production yield. Therefore, to fill the gap between the laboratory scale and industrial scale, a UHV system (henceforth wafer system) was designed, assembled, and calibrated for processing silicon wafers with 100 mm diameter. It is worth to mention that the system could be designed and assembled for processing larger wafers up to 300 mm diameter, as the components required for building such a system are available in the market.

Another benefit of this system is that very small samples could be processed in it. As explained in Sec. 2.2, only $6 \times 12\ mm^2$ samples which are compatible with Omicron sample holders could be processed in the laboratory scale surface science system. However, for processing smaller samples like ready devices such as detectors, the Omicron sample holders cannot be used. These samples with miscellaneous dimensions were processed in the wafer system by using a buffer silicon wafer with diameter of 100 mm. The samples with miscellaneous dimensions were placed on top of the buffer silicon wafer and were processed under UHV condition (See Fig. 13). Fig. 14 shows the wafer system in the clean room. The specifications of this system is explained in SubSec.s 2.3.1 to 2.3.6. The pressure within this chamber could reach to lower than 1×10^{-9} mbar.

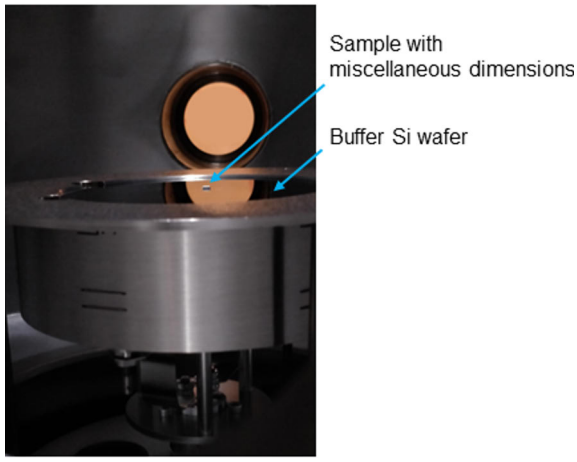

Figure 13. Samples with miscellaneous dimensions could be heated and oxidized in the wafer system using a buffer Si wafer put on top of the heater element.

2.3.1 Ultrahigh vacuum chamber

The UHV chamber used in the wafer system is a cylindrical stainless steel (304) chamber with 406 mm diameter and height of 254 mm. The bottom plate of the chamber is extended by using a port with the height of 189 mm, which is welded to the main body. This long port is required for inserting the heater element stage into the chamber. To avoid overheating of the chamber at high heater element temperatures, the chamber is equipped with embedded water cooling system. During the heating, water at 17 °C temperature flow into the walls of the chamber with 4 l/min flow rate and keeps the chamber walls cooled during the heating. The chamber is equipped with 15 different ports. Fig. 15 shows top view drawing of the chamber and the details of the ports are presented in Table 1.

2.3.2 Pumping

The wafer system is connected to a compression pumping system consist of a Turbomolecular pump, which is connected to the main chamber through a DN100CF port. This pump is connected to a rotary vane backing pump. The system is vented each time a sample is inserted in or taken out from the chamber. To protect the Turbomolecular pump from working under strain due to viscous flow nature of the gas in the beginning of the pumping when the chamber pressure is at atmosphere level, the pumping is started by rotary vane pump until the pressure of the chamber reaches below 10^{-2} mbar [69], and then the Turbomolecular pump is switched on.

2.3.3 Pressure gauges

A variety of pressure gauges could be used in vacuum systems. Choosing the suitable pressure gauge for a system depends mainly on the pressure range that should

be measured within the system. When it comes to UHV pressure range, two main pressure gauges are available: hot and cold cathode ionization gauges. The working principle of both gauges is based on measuring the pressure based on the number of detected ionized gas molecules within the gauge head that is inserted into the UHV system.

Considering the fact that the wafer system is vented to air pressure for inserting in and taking out the samples, cold cathode gauges was utilized for this system to avoid accidental burn out of the filament in the hot cathode ionization gauge. The gauge is connected to the main chamber through port D2 (see Fig. 15) which is DN40CF compatible. To exclude the effect of the location of the gauge on the measurement, another cold cathode gauge was installed to the port B3 (see Fig. 15). Measuring the pressure at the same time with these two gauges installed on different ports did not show noticeable difference in pressure measurement, therefore, the effect of the gauge location on measured pressure could be excluded. The cold cathode pressure gauge was used to measure the pressure in the wafer system and to measure the partial pressure of oxygen during the oxidation process. The gauge could be used to measure the pressure within the range of 10^{-9} to 10^{-2} mbar.

Figure 14. Picture of the wafer system in clean room.

2.3.4 Heater element

A heater element was required to enable heating semiconductor wafers with diameter of 100 mm. Different materials were available for the heater element e.g. Pyrolytic Graphite coated Graphite, Pyrolytic Boron Nitride coated Graphite, Solid Silicon Carbide, and Solid Silicon Carbide coated Graphite. Among these heater element materials, solid silicon carbide fulfills the requirements of the wafer system as it could be used under UHV condition, it is resistant against oxidation,and its ultimate achievable temperature is 1000 °C. The only disadvantage of this heater element is its high price compared to other possible materials. The solid SiC heater element with diameter of 125 mm is mounted on a manipulator equipped with an Inconel cradle with 25 mm height adjustment to facilitate the mounting and unmounting of the wafer. The manipulator operating height could be adjusted within 150 mm range by a manually actuated insertion/retraction belows-sealed linear shift mechanism.

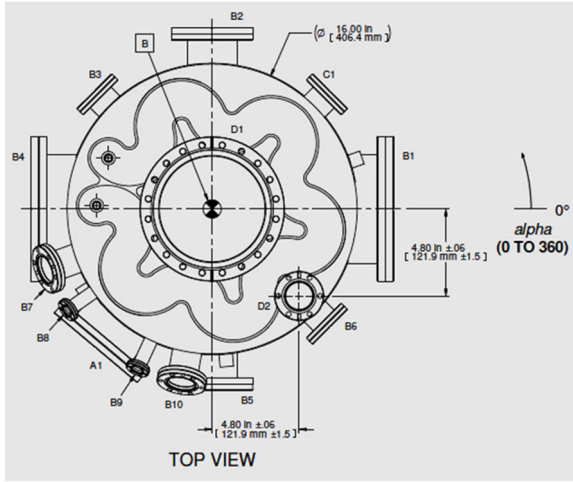

Figure 15. Drawing of the chamber used in the wafer system. Figure modified from the approved drawing provided by Kurt J. Lesker Company.

The manipulator could be fully retracted and inserted for transferring and mounting/unmounting of the sample.

The heater element and the manipulator are mounted on a DN200CF flange and the flange is connected to the compatible port located at the bottom plate of the chamber. This way, the heater element is installed in the facing-up position. Fig. 16 shows the drawing of the heater element, and its manipulator. The heater element is connected to a combined temperature controller (suitable for K-type thermocouple) and DC power supply (96 V, 31 A) through a feed-through DN40CF flange.

Port	Function
A1	Turbomolecular pump
B1	Sample insertion
B2	View port
B3	RGA/extra pressure gauge
B4	Sample insertion
B5	View port
B6	Spare port
B7	Evaporation source
B8	Shutter
B9	Shutter
B10	Evaporation source
C1	Oxygen leak valve
D1	View port
D2	Pressure gauge
E1	Heater element

Table 1. Port identification details of the chamber used in the wafer system

2.3.5 Other parts

All the ports of the chamber are ConFlat® compatible and the flanges are sealed with copper gaskets. The chamber has three DN150CF/DN160CF ports that could be used for inserting in and taking out the samples. One of these ports is connected to a pneumatic gate valve to facilitate sample inserting in/taking out. Three view ports are connected to the system through DN63CF compatible ports to enable monitor-

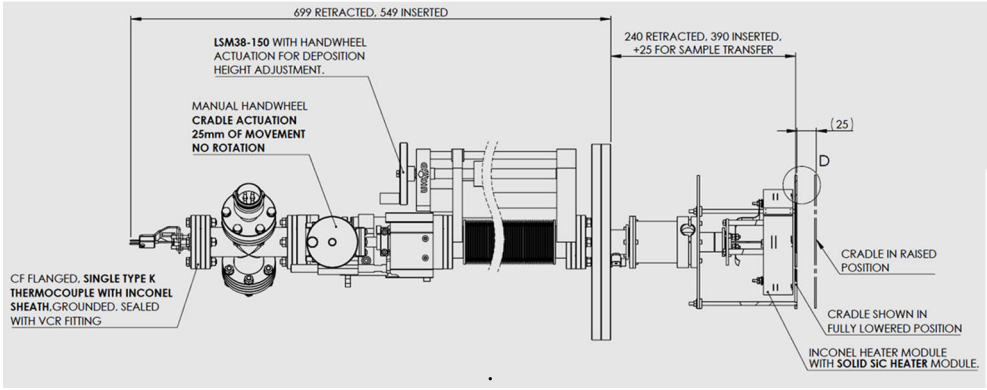

Figure 16. Drawing of the heater used in the wafer system. Figure modified from the approved drawing provided by UHV Design Ltd.

ing the heating and oxidation process and calibrating the temperature. The glass material of these view ports is UV sapphire which enables using them at temperatures up to 450 °C. An all-metal regulating leak valve is connected to the system through a DN40CF compatible port. This leak valve is used to increase the oxygen partial pressure during the oxidation process and is connected to a regulator and high purity oxygen bottle. Two additional DN40CF compatible ports were designed for the system for other purposes e.g connecting residual gas analysis (RGA) unit to the system. Two more DN40CF compatible ports were designed for the system that could be used for installing possible thermal evaporation sources. These ports have neighboring DN16CF compatible ports that could be used to install shutters for the evaporation sources.

2.3.6 Calibration

The temperature of the wafer during heating must be calibrated. The heater manipulator is equipped with a K-type thermocouple. The wafer temperature is also measured using two different pyrometers (high and low temperature ranges) while the emissivity is set on 0.6. The heat transfer within UHV happens mainly through radiation. Although the heater element is equipped with heat shields, still the position of the heater element within the chamber affects the heat transfer. If the heater element is retracted so that the heater element is near to the bottom plate of the chamber, the bottom plate and the long port on the bottom of the chamber become warmer than the rest of the chamber. Regarding the fact that the long port has no water-cooling, then the temperature of the bottom part of the chamber and consequently the temperature of the wafer on top of the heater element will increase for a given voltage and current of the power supply compared to the positions of the element near the middle of the chamber. To overcome this problem, an optimized position of the heater within the

chamber was chosen during the heating and oxidation process and the temperature was calibrated for this position.

2.4 Atomic layer deposition (ALD)

In 2018, Millennium Technology Prize was awarded to Dr.Tuomo Suntola for his innovation entitled atomic layer deposition ALD[1] developed by him in 1970s [70; 71]. In early 2000s, the semiconductor industry realized the importance of ALD and since then this method is used for producing thin isolating or conducting atomic layers. Regarding the reduction of the size of electronic components, ALD is being utilized in semiconductor industry as it provides mono layer growth control and uniformity of the grown layer on high aspect ratio structures [72].

To grow a mono layer of metal oxide by ALD, two half cycles are required. In the first half cycle a precursor pulse is inserted into the reactor at elevated temperature. This precursor reacts with the surface and then the reactor is flushed by an inert gas. Then the second pulse is inserted into the reactor and molecules of the second precursor react with the existing layer on the substrate deposited during the first pulse and form the final mono layer on the surface. After this pulse the chamber is flushed again with the inert gas. The cycles could be repeated until the desired thickness of the oxide is reached. Fig. 17 shows the ALD mechanism schematically. In this thesis two types of ALD machines were used: home-built and commercial. The home-built ALD is suitable for processing small samples and the commercial one was used for wafers. Precursors used for depositing Al_2O_3 and HfO_2 were water and trimethylaluminum (TMA) and tetrakis-dimethylamido hafnium (TDMAH) respectively.

2.5 Silicon experiments

2.5.1 Chemical pre-treatment

Si samples were treated with wet-chemical methods prior to any processing steps such as UHV heating and oxidation, ALD, or metal deposition. The chemical pre-treatment was based on the RCA recipe which is widely used as chemical cleaning method for Si. RCA contains two main steps of standard clean (SC)-1 and SC-2, which could be combined with immersion in Piranha solution. For experiments of this thesis, the samples were first cleaned in an ultrasonic bath while immersed in acetone and methanol. In the next steps, the sample is immersed in Piranha solution and SC-1 to remove organic contaminants and SC-2 solutions to remove metallic contaminants from the surface [73; 52]. In SC-1 and SC-2, Si is immersed into a solution of NH_4OH: H_2O_2:H_2O (1:1:5) and HCl:H_2O_2:H_2O (1:1:6) respectively.

[1] https://millenniumprize.org/news-articles/news/

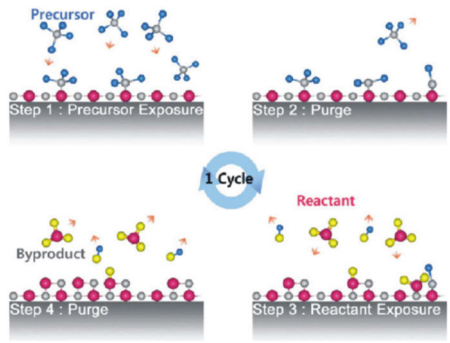

Figure 17. ALD growth process shown schematically, after [76]

In both steps the duration of immersion is 10 minutes and the temperature of the solution is 80 °C. After SC-2 an oxide layer is formed on the surface of silicon. In some experiments, an additional step of immersing silicon into HF was followed after RCA to remove the oxide. The surface after HF dip is hydrogen passivated [74; 75].

2.5.2 Ultra-high vacuum pre-treatment

Silicon wafers with diameter of 100 *mm* and 6×12 mm^2 silicon samples were heated and oxidized in UHV systems explained in Sec.s 2.3 and 2.2 respectively after chemical pre-treatment.

2.5.3 Ultra-high vacuum post-treatment

In addition to silicon samples, ready devices were heated and oxidized under UHV condition as well. These samples were treated in the wafer system explained in Sec. 2.3, as they were not compatible with Omicron sample holders used in the UHV system explained in Sec. 2.2. These samples were put on a Si buffer wafer mounted on the cradle.

2.5.4 Fabricating MOS capacitors

To fabricate MOS capacitors, an insulator layer of HfO_2 was grown on the surface of Si using a prototype home-made ALD. Afterwards, front metal contacts were grown on the insulating layer using shadow mask and sputtering. The back contact was made using silver paste.

2.6 Gallium arsenide experiments

2.6.1 GaOOH nanocrystals on GaAs

To grow GaOOH nanocrystals on GaAs surface, GaAs surface was first cleaned in ultrasonic bath while immersed in IPA and then it was cleaned with IPA:HCl solution for three minutes which removes carbon contamination and provides an oxide free surface for next steps [77; 78]. Samples were then immersed into IPA for one minute. After cleaning the surface, the sample is immersed into deionized hot water (HW) kept at 80 °C. This simple treatment results in the growth of GaOOH nanocrystals on GaAs surface. Immersion time and water temperature are effective parameters on the growth of nanocrystals.

2.6.2 Black GaAs

To prepare black GaAs, the same treatment as explained in the previous section (2.6.1) is done with an additional step of immersing the sample into hot hydrogen peroxide (HHP) kept at 80 °C. This step is after chemical cleaning and before immersing the sample into HW. After this treatment, surface color is changed to black and reflectance is reduced down to $\frac{1}{10}$ of the reflectance of the reference sample, which is GaAs with native oxide on its surface.

3 Characterization methods

Surface sensitive characterization methods were utilized in this thesis as the surface of investigated semiconductors must have been characterized. In addition to surface sensitive characterization methods, electrical and optical characterizations were performed on the samples and devices to investigate the studied surfaces and interfaces. Other characterization methods were used for some samples when the above mentioned methods were not suitable. It is important to use different characterization methods to make more accurate conclusion about the surface. For this reason, different characterization methods are used in this thesis, of which some of them are used through collaboration.

3.1 Low energy electron diffraction

LEED is a surface sensitive method that is widely used in surface science to investigate the surface structure. By using LEED it is possible to investigate the crystalline order of the surface. In fact electrons diffraction from crystals was one of the observations that supported modern physics theories. Fig. 18 shows schematically a LEED apparatus. An electron gun produces electrons which reach the sample surface in UHV and interact with the surface. Diffraction pattern of elastically scattered electrons are detected on a fluorescent screen connected to high voltage. When incident electrons interact with the surface, back scattered electrons are scattered elastically and in-elastically. Elastically scattered electrons have the same energy as incident electrons and they make the diffraction pattern on the screen. In-elastically scattered electrons could be prevented from reaching the screen by applying variable negative voltage on a set of grids. The electron energy in LEED is $20 - 200\ eV$, so electrons interact with the surface. In LEED electrons behave like waves and then the de Broglie equation could be used for explaining the electrons behaviour;

$$\lambda = \frac{h}{p} = \frac{h}{\sqrt{2mE}}, \tag{6}$$

where λ is wavelength, h is Plank constant, m is the electron mass, E is the electron kinetic energy.

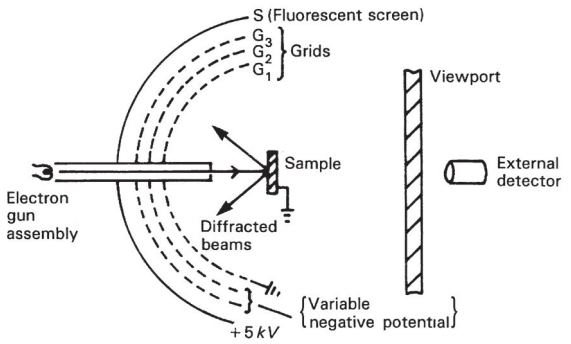

Figure 18. Schematic figure of LEED. The figure is taken from [79].

3.2 X-ray photoelectron spectroscopy

XPS which is also known as electron spectroscopy for chemical analysis (ESCA) is a surface sensitive characterization method that is widely used in surface science labs and could provide information on the elemental composition and theier relative concentration in specimen and the chemical state of atoms. Fig. 19 shows a typical XPS instrument used in laboratories.

As shown in Fig. 20, X-ray photon with energy of $h\nu$ emitted from an x-ray source interacts with core level electrons of an atom, if the energy transferred to electron is enough, the core-level electron with binding energy of E_B will be ejected from the atom. The ejected electron will have the kinetic energy of E_K. The binding energy of the ejected electron is calculated from equation

$$E_B = h\nu \ - E_K - W, \tag{7}$$

where E_B is the binding energy of core-level electron, $h\nu$ is the photon energy, E_K is the kinetic energy of the ejected core-level electron, and W is the work function of the spectrometer.

The photon energy $h\nu$ is a known value as typical laboratory XPS systems use $Al\ K_\alpha$ or $Mg\ K_\alpha$ as x-ray source with emission photon energy of 1486.6 and 1253.6 eV respectively[80]. Also, in synchrotron centers, it is possible to use x-ray with different and tunable energies which provides more freedom for depth profiling and having more detailed spectrum of a sample. Work function of the spectrometer is a known value as well. So, by measuring the kinetic energy of electrons that reach the analyzer, it is possible to have binding energy of them.

If ejected electrons reach the analyzer without losing kinetic energy due to further interactions, they represent binding energy of electrons in the spectrum as peaks and those electrons scattered inelastically contribute to the spectrum as background.

Since the binding energy of a core-level electrons is a fingerprint of each element, it is possible to identify the elements present in a specimen. In addition, the intensity of a peak is proportional to the concentration of an element in a specimen.

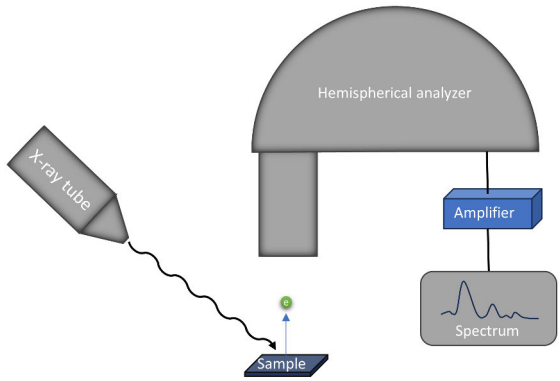

Figure 19. Schematics of a typical x-ray instrument.

In addition to qualitative analysis, more information can be obtained from the surface by quantitative analysis of XPS spectra or peak fitting. For obtaining this information, the background of the spectrum which is due to the inelastically scattered electrons should be removed first. Shirley Background is commonly used as background of the spectrum. The XPS peaks have Voigt shape resulting from the convolution of Gaussian and Lorentzian profiles. The Gaussian profile of the peak is due to the instrument while the Lorentzian profile is related to the photoemission from the sample. After peak fitting, it is possible to calculate the concentration of each peak by calculation the area below the peak.

3.3 Scanning electron microscopy

Scanning electron microscopy (SEM) is used to investigate the morphology and chemical composition of surfaces of different materials. It is widely used in materials science and semiconductor industry for different purposes, for example in doping concentration profiling [81; 82; 83] and grain size distribution [84].

Different computational methods, software, and recently AI have been developed to assist in analyzing SEM images [85; 86; 84].

As the name suggests, SEM is a microscope that provides better resolution compared to optical microscope since it uses electrons rather than light which equips SEM with shorter wavelengths compared to light. The wavelength of electrons in SEM could be calculated by De Broglie equation (6) and substituting the velocity of electron from:

$$eV = \frac{1}{2}mv^2, \tag{8}$$

Where e is electron charge, V is the accelerating voltage, m is the electron rest mass, and v is the electron velocity. The wavelength of electron in nm will be[87]:

$$\lambda_e = \frac{h}{\sqrt{2emV}} = \frac{1.22}{\sqrt{V}}, \tag{9}$$

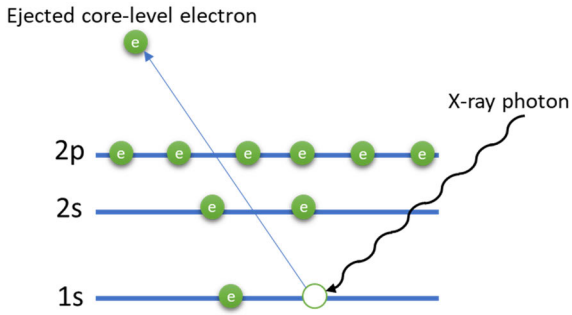

Figure 20. Interaction of x-ray with core-level 1s electron. Phton with energy of $h\nu$ ejects an electron and the electron leaves the atom.

Where h is Plank constant. Considering the accelerating voltage in SEM, being $1-30$ kV [88], the electron wavelength will be $0.007-0.038$ nm. It should be noted that one need to consider the relativistic mass of electron at higher accelerating voltages e.g. for transmission electron microscopy (TEM).

In SEM a beam of electrons produced by an electron filament passes through electromagnetic lenses and interacts with the sample surface as shown schematically in Fig. 21 . Depending on the interaction between incident electrons and the sample, back-scattered electrons (BSE), secondary electrons (SE), and characteristic x-ray are produced and could be detected by suitable detectors.

BSEs are the elastically scattered electrons by the nucleus and have strong correlation with atomic number. SEs are in-elastically scattered electrons which interacted with core or valence level electrons in the atom. These electrons are collected to a positively biased detector. Characteristic x-ray is resulted if the incident electron ejects a core-shell electron and an outer shell electron fills the created vacancy and x-ray is emitted. Fig. 22 shows schematically a SEM instrument and the

Different detectors can be utilized to detect BSE and SEs and characteristic x-ray leaving the specimen following the interaction between incident electron beam and the specimen surface.

The most common detector used in SEM to detect SEs is Everhart-Thornley detector (ETD). This detector is mainly used to have information on morphology of the surface. BSE detectors are used to detect BSEs and provide information on the composition contrast of the specimen [89]. To detect characteristic x-ray, energy-dispersive x-ray spectroscopy (EDS) detector is used. Position of these detectors in SEM are shown schematically in Fig. 21.

3.4 Electrical characterization

As mentioned in Sec. 2.5.4, MOS capacitors were fabricated on Si and their current-voltage and capacitance-voltage characteristics were measured. As discussed in Sec. 1.2.1, leakage current in MOS capacitors is an indication of smaller amount of interface defects and it reduced the off-state leakage current which eventually reduced

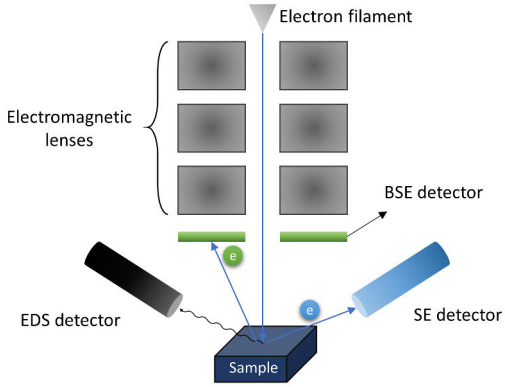

Figure 21. Simple schematic of a SEM instrument. Electrons leave the filament and are accelerated towards the specimen. The electron beam passes through different electromagnetic lenses. The products of the interaction between incident electron beam and the specimen are BSEs, SEs, and characteristic x-ray that are detected by suitable detectors.

the power consumption of a chip. In addition to MOS capacitors, current-voltage was measured for solar cells and fabricated Schottky detectors on n-type and semi-insulating (SI) GaAs in dark and under illumination.

3.5 Other characterization methods

Other characterization methods have been utilized through collaboration to obtain results included within this thesis. These methods are photoluminescence (PL), reflectance, TEM, X-ray diffraction (XRD), STM, STS, and corona-oxide characterization of semiconductors (COCOS).

PL measurements provide information about passivation properties of a studied surface. PL is a non-destructive method that could be used to evaluate qualitatively the amount of surface and interface defects mainly in direct band gap semiconductors. In PL, photons with energy higher than the material band gap energy ($h\nu > E_g$) interact with the studied semiconductor and produce electron-hole pairs. Optically generated electron-hole pairs will be relaxed in the conduction band minimum and valence band maximum. Then they will recombine radiatively and emit photons which will be detected by a photodetector. When there are defects present in the band gap, non-radiative recombination happens. Therefore, increased PL intensity could be a sign of reduced non-radiative recombination which is caused by point defects on the surface [90; 91].

Reflectance of a surface is measured within a wavelength range. Reduced reflectance over wide wavelength range is preferred and ARCs that provide reflectance over a wide wavelength are required e.g. in III-V semiconductor multi-junction solar cells [92]. Growing nanocrystals and multiple thin layers as anti-reflection coating are used to reduce reflectance [48; 93; 49]. When reflectance is reduced, it increased the number of absorbed photons and reduces the number of reflected photons from the surface.

Increased PL and reduced reflectance show reduction in optical losses in a device.

The working principle of TEM device is like SEM, with some differences. The energy of electrons is higher in TEM and electrons pass through a very thin layer of the specimen (around 100 *nm*) [94]. Sample preparation is more complicated and time consuming in TEM. Also smaller area of a sample is investigated compared to SEM. Better resolution of TEM makes it possible to investigate the crystal orientation of a specimen.

XRD is a widely used method to identify the crystal structure of powders, single and multi-crystalline materials, thin films, and nanostructures [95; 96; 97; 98]. It is also possible to monitor phase transition of a material via in-situ XRD measurement [99]. When crystal structure of a surface is of interest in XRD like thin films or nanocrystals grown on a substrate, grazing incidence X-Ray diffraction (GI-XRD) is used where x-ray reaches the sample surface in a grazing incident angle making XRD surface sensitive [100; 101].

STM and STS are surface science techniques that provide small scale topography and localized electronic states around the Fermi level of a conductive surface respectively. STM works based on the tunneling effect and provides information in real space. In STM, a small voltage is applied between a very sharp tip and the surface which enables a tunneling current flow between top surface of the sample and the tip. STM could be used in two modes, constant current or constant distance mode having slower and faster scan speed respectively. In constant current mode, which is the most used mode of STM the current between the tip and surface is kept constant by a feedback loop where voltage is applied on the pizoelectric driver to keep the current constant. The feedback loop variation is due to the distance change between surface and the tip, so by measuring the voltage of the feedback loop, it is possible to have topographical image of the surface. In constant distance mode, the distance between the tip and the surface is kept constant which enables imaging faster. Disadvantage of the constant distance mode is that the tip might crash into the surface if the surface being studied is not atomically flat [102; 103]. STM could be used to investigate defects on the surface [43; 104].

COCOS is used to measure defect density in the interface between silicon and the oxide on top of it. Benefits of COCOS include fast measurement, measurement without making a contact, and possibility to be used for different wafer sizes (up to 300 mm) [105; 106; 107; 108; 109].

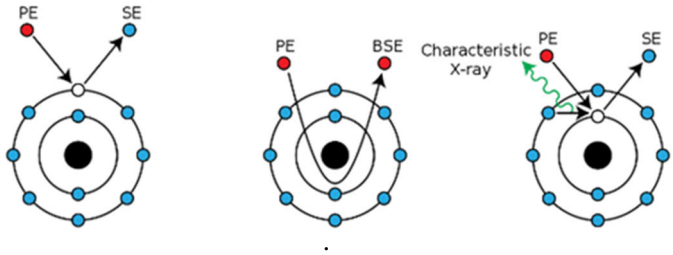

Figure 22. Different products are produced when the incident electron beam interacts with the specimen: SE, BSE, characteristic x-ray [110]

4 Summary of the results and conclusions

The results of this thesis have been published in two patent families granted in Finland ([111; 112]). The results related to these patent families are presented in the first and second articles included in this thesis. Two priority patent applications are filed related to the results presented in the third publication included into this thesis. A Research to Business (R2B) project entitled "Growing nanostructures on III-V semiconductors by a cost efficient and simple method" (RONASEC) is funded by Business Finland for commercialization of the patent families related to the last publication included in this thesis.

In this chapter, possible future steps and the summary of the publications included into this thesis are presented.

4.1 Possible scaling up of the UHV system for treating wafers

As discussed in Sec. 2.3, silicon industry is moving towards using larger silicon wafers (up to 300 mm in diameter) to increase the production yield, while in this thesis, a UHV system for processing wafers with diameter of 100 mm was designed and built. However, it is possible to scale up the the system to process larger silicon wafers as the heater element for heating up to 300 mm silicon wafers are available in the market. Also, other possible heater elements could be utilized in the system to reduce the investment cost.

A load-lock chamber could be added to the current system to speed up the heating and oxidation process. It is also possible to integrate the UHV heating and oxidation of silicon wafers into other HV and UHV systems that are utilized in the semiconductor industry. For example, it is possible to integrate this UHV heating and oxidation step into industrial ALD units available in the market.

4.2 Summary of the results for silicon (papers I and II)

In the first and second paper, low temperature ultrahigh vacuum (LT-UHV) is used to improve the silicon surface by heating and controlled oxidation at temperatures below 450 °C in UHV condition. Fig 23 shows how LT-UHV was utilized on Si

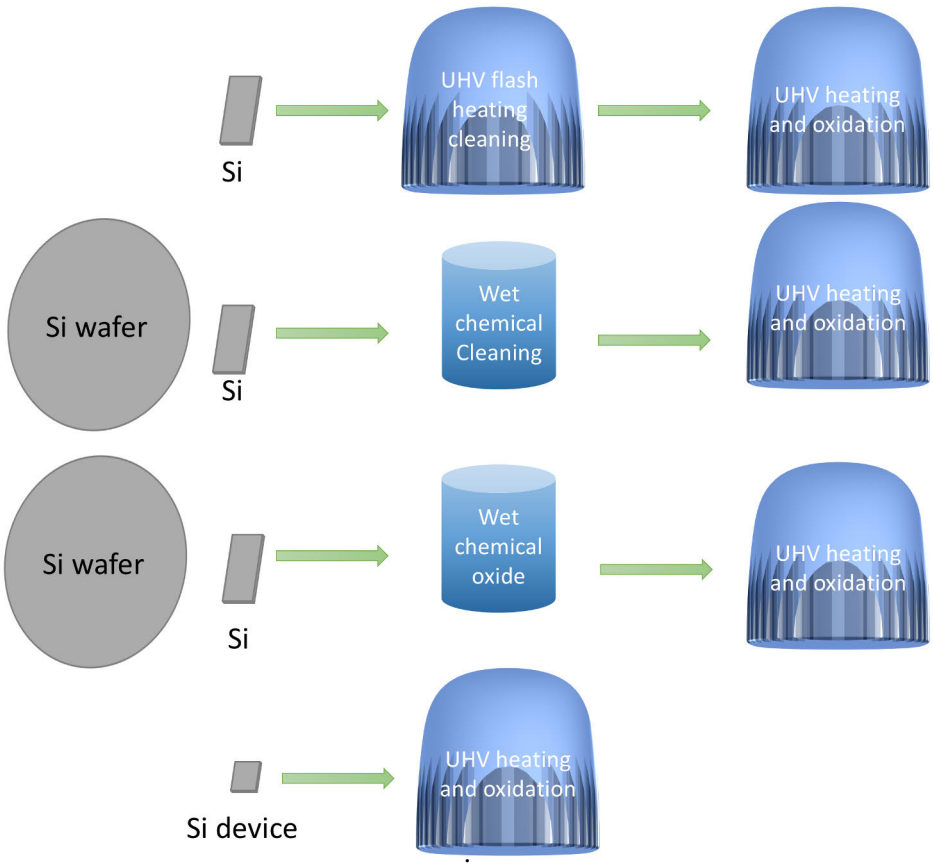

Figure 23. Schematic summary of applying UHV heating and oxidation on Si small pieces, wafers, and device structures.

pieces, wafers, and devices schematically.

In the first article, the concentration of studies is on heating and controlled oxidation of clean Si surface. The surface is cleaned by UHV flash heating at 1200 °C or by RCA.

In the second article the concentration is on applying LT-UHV heating and oxidation on Si surface with silicon oxide layer on it grown by wet-chemical methods [113; 114].

In both articles, the LT-UHV treatment was applied on commercial devices. The controlled heating and oxidation under UHV condition at temperatures lower than 450 °C reduces the leakage current in commercial silicon detectors and diodes. The reduced leakage current could be linked to the improved sidewall passivation and reduced defect density.

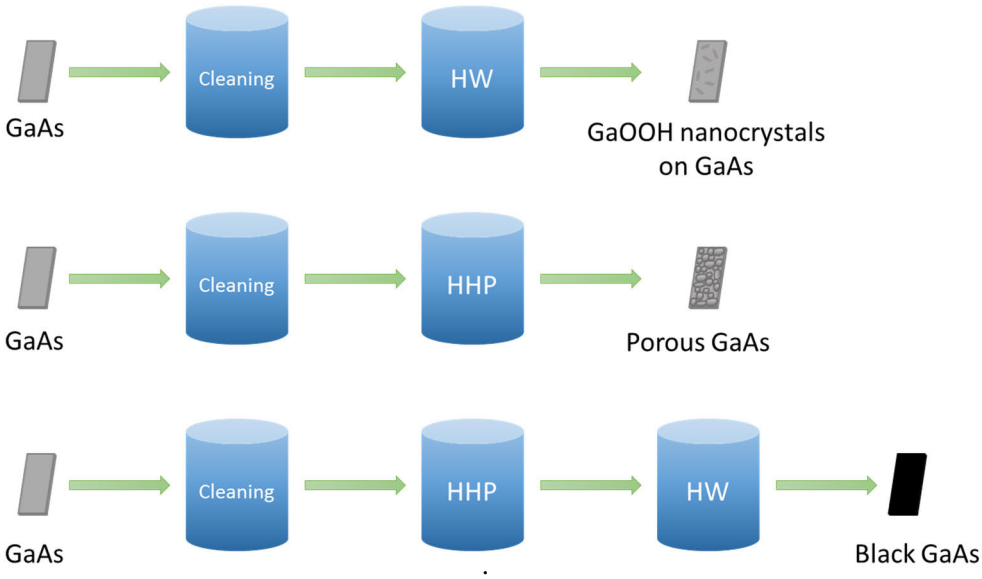

Figure 24. Schematic summary of the chemical treatments presented in the third article included in this thesis.

4.3 Summary of the results for GaOOH nanocrystals and black GaAs (paper III)

In the third article the summary of results on reducing optical losses on GaAs surface by HW and HHP treatments on GaAs are presented. To investigated whether the treatment could be useful in device structures, the treatment was applied on quantum-well (QW) structures, where the results show increased PL intensity of QWs after HW treatment.

Fig. 24 shows schematically the summary of chemical treatment done on GaAs.

The immersion of GaAs into HW results in the growth of GaOOH nanocrystals on the surface. According to EDS results, the substrate is mainly composed of Ga and As, while nanocrystals are formed of gallium and oxygen. As the hydrogen could not be detected by EDS, grazing incidence synchrotron X-ray diffraction (GI-SXRD) was used to identify the elemental composition and crystal structure of nanocrystals. GI-SXRD results suggest that nanocrystals are GaOOH.

Immersion in HHP results in porous structure on the surface. The thickness of the porous layer depends on the immersion time. EDS results show that the surface is mainly composed of gallium and arsenic.

The immersion of GaAs into HHP followed by a HW immersion results in reduced reflectance of the surface by factor of 10. The surface color of GaAs which is normally gray, changes to black after this treatment. In addition, when the black-GaAs is used in metal-semiconductor-metal photodetectors, the external quantum

efficiency (EQE) increases. The EQE values are higher than 100% at 5 *V* bias. The exact mechanism behind the increased EQE above 100% is not known yet, but since this increase is happening under bias, it may arise from an imbalance between electron and hole drift components in the current transport.

The effect of cleaning, HW immersion time and temperature on nanocrystals are investigated as well.

4.4 Conclusions

In this thesis, different passivation methods were applied on two semiconductors: silicon and gallium arsenide.

For Si, a UHV step was introduced after wet chemical cleaning of Si surface where the surface was covered by a chemically grown silicon oxide layer or it was hydrogen passivated. The results suggest that additional low temperature heating and oxidation after wet chemical step could improve the surface passivation of Si. In addition to typical size of a surface science sample, this UHV step was applied on Si wafers with 100 *mm* diameter. This could pave the way to utilize this method on larger wafers and possibly in production lines.

A wet chemical treatment method was applied on GaAs surface. In this method, a HW immersion results in the growth of GaOOH nano and micro crystals on the surface. When a HHP step is applied on the surface prior to HW, the surface color of GaAs changes from gray to black. The HHP immersion alone results in a porous GaAs structure. The results suggest that by applying this wet chemical treatment on the surface of GaAs, optical losses could be reduced. The fact that this method is a simple wet chemical method makes scaling up possible.

The main results of publications included in this thesis are:

- **paper 1**:
  new crystalline surface structure was observed on Si after low-T oxidation
- **paper 2**:
  chemical oxide of Si was modified by low temperature oxidation in UHV such that defect density decreases and recombination time increases.
  wafer scale instrument for UHV treatments was constructed.
- **paper 3**:
  Novel HW immersion was done for making GaOOH nano and microstructures on GaAs.
  Black GaAs with reflectance below 1% was formed on GaAs by a novel HHP immersion followed by a HW immersion step.

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