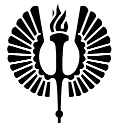


# Studying Nickel Contamination on Silicon Surfaces using XPS and Ultrahigh Vacuum Heating

Materials Physics/Department of Physics and Astronomy

Master's thesis

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## Abstract

Nickel and Silicon systems hold a key value in modern semiconductor devices. Owing to their conductive properties, thermal stability, and ability to form nickel silicides, they are used in nanoscale contacts, Schottky junctions, and low-resistance interconnect technologies. Nickel silicides ($Ni_2Si$, NiSi, and $NiSi_2$) can be used to create thermally stable contact layers essential for MEMS, CMOS, and photovoltaic devices. Same material that delivers technologically valuable silicides can also produce challenges during improper Si wafer handling, leading to unintended Ni contamination.

Ni impurities can host deep-level traps, elevate leakage currents, and degrade carrier lifetime in Si wafers, which can lead to significant electrical defects, resulting in lower device performance and manufacturing yield. So it is important to understand Si surface chemistry and how Ni interacts with silicon based surfaces.

This thesis studies Si surface chemistry, Ni's interaction with Si, cons and pros of Nickel Silicides, and behaviour of Ni contamination on different Si surfaces at high temperature treatments (range from 600°C to 1200°C) under ultra-high vacuum ($10^{-8}$ and $10^{-9}$ mbar). Samples were analysed using high-resolution XPS to get more insights, including chemical states of Ni and other possible contaminations.

Ni contamination appeared at 1000°C when first sample was heated from 600°C (30mins), 800°C (30mins), 1000°C (5mins), 1200°C (5secs). Later on experiment was repeated for a new and the same Si surface but this time, temperature was increased to 900°C after 600°C. XPS spectrum showed appearance of Ni contamination at 900°C along with elimination of Si oxide state. Another sample, which already had Ni contamination and was cleaned by HF solution demonstrated elevation in Ni concentration at higher temperatures (same range above). The identified nickel exhibited Nickel oxide states towards higher binding energies along with $Ni_2O_32p_{1/2}$ and $Ni2p_{1/2}$ towards lower binding energy. However, appearance of Ni at higher temperatures is discussed in results and discussion chapter.

Through literature and experimental studies, this thesis facilitates a comprehensive understanding of Ni/Si contact behaviour, formation of nickel silicide, and the analytical methods most capable of detecting nanoscale impurities. The findings aim to support reliable device fabrication and contamination free processing within advanced semiconductor technologies, especially at higher temperatures and clean room facilities.

# 1 Introduction

In current chapter, importance and unique properties of silicon (Si) as a semiconductor will be discussed along with different types of nickel (Ni) contaminations as well as their mechanisms that occur during the fabrication process, impacting the quality of Si semiconductors used in a variety of devices including micro-electro-mechanical system, integrated circuits, and photovoltaic-cells, etc.

## 1.1 Evolution in Semiconductor Materials; from Germanium to Silicon

In 1958, first ever integrated circuit came into existence when Jack Kelby, after the invention of the transistor, electronically installed transistors, resistor, and capacitor on Germanium (Ge) chips. An interesting fact about these inventions were they all were based on Ge instead of Si due to the fact that electron mobility of Ge is higher as compared to Si, resulting in better processing speed of the Ge-based computers. However, the only drawback application of Ge is that its efficiency when temperature increases is not the same as compared to Si, which delivered promising results even at 170 degrees Celsius. Also, this characteristic can be attributed to having different energy band gaps which highly impacts how a semiconductor reacts under different circumstances. So, Si, as a result of possessing higher band gap ~1.1 eV, is better resistant towards heat in comparison to Ge with a lower band gap ~ 0.7eV.

Till now, we have observed both Si and Ge possessing their own cons and pros but in future as rise of using semiconductor was observed in many electrical devices as a result of a novelty in Si manufacturing. Before this, Si-based transistors were sold at 14 dollars and Ge transistor were priced at around 2 dollars in 1956. One more reason of transition towards more usage Si is its abundancy in the earth's core. So with better manufacturing and extraction practices, price of the Si dropped and that resulted of it being more used in the modern electronics for a variety of applications including in energy, communication, and more. In addition, second-generation-semiconductors composed on indium phosphide and gallium-arsenide were introduced that offered direct band gap, electron mobility, and other desirable semiconducting properties that are useful in photonics and devices that undergo high temperature, frequency, and power applications. All of these led to successful transition from Ge. Some of the newly developed semiconductors were toxic and cannot be used widely as compared to Si, so Si remained undefeated when it came to usage in the electronic devices [1].

## 1.2 Silicon's significance in electronics

Si possesses an overall advantage over other semiconductor materials based on its availability and highly developed manufacturing practices. Here we will discuss cost-efficiency and properties of elemental Si based on physical, electronic, and chemical characteristics including crystal structure and band gap. In addition, some Si-based devices are going to be presented as well.

### 1.2.1 Silicon's electric, mechanical and chemical properties

Silicon is 28% percent of the earth's crust, making it one of the most abundant elements. Crystalline Si exists in diamond structure (face-centered cubic) where each Si atom is bonded with four other Si atoms via covalent bonds as show in figure 1 below. Furthermore, thermal conductivity at 300 K for elemental Si is 150 W/m k, which is quite significant [2] .

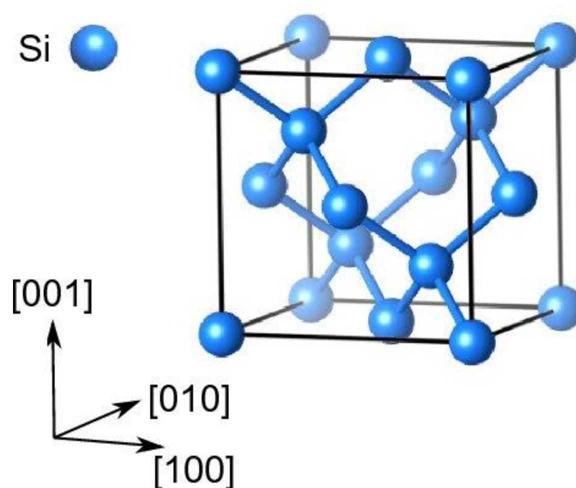



Figure 1: Cubic crystal structure of Silicon [3]

Cubic lattice constant for Si is ~ 5.431 Å, which can be influenced along with other mechanical properties like elastic constant and overall strength if Si is doped with dopants containing excess of holes and electrons. For example, researchers reported a 7.5% decrease in elastic modulus of crystalline Si when impurity B with concentration ($1.0 \times 10^{21}$ $cm^{-3}$) was introduced in pure silicon [3] .

Some of the electrical and optical properties of elemental Si are provided below in the table [4]:

Table 1: Elemental silicon's electrical properties

| Property | Value |
|---|---|
| Breakdown field | $3*10^5$ V/cm |
| Refraction Index | 3.42 |
| Mobility electrons | 1400 $cm^2$ / (V*s) |
| Mobility holes | 450 $cm^2$ / (V*s) |
| Diffusion-coefficient electrons | 36 $cm^2/s$ |
| Diffusion-coefficient holes | 12 $cm^2/s$ |
| Electron thermal velocity | $2.3*10^5$ m/s |
| Electronegativity | 1.8 Pauling Scale |
| Hole thermal velocity | $1.65*10^5$ m/s |
| Optical phonon energy | 0.063 eV |
| Surface-atoms density | (100) 6.78 (units: $10^{14}/cm^2$)<br>(110) 9.59 (units: $10^{14}/cm^2$)<br>(111) 7.83 (units: $10^{14}/cm^2$) |

As it has been established earlier that Si despite presence of all other alternatives holds the major share when it comes to semiconductor applications. From table 1, we can deduce that it is due to better compatibility with industrial practices and balanced electrical characteristics. For instance, breakdown field of circa $3*10^5$ V/cm makes it capable of facilitating applications across low voltage to medium voltage. Additionally, mobility of electrons is higher than holes, which makes Si a more favourable material for n-type material applications. Formation of junction stably and seamless doping can be facilitated by Si due to low-electronegativity and 4.15 eV of intrinsic work-function. Si has refractive index of 3.42 and is not ideal for optoelectronic applications due to indirect bandgap. Also, atomic density gets impacted significantly on crystal orientation of Si ultimately affecting etching and oxidation. Although, (100) plane is preferred during IC fabrication as it enables smooth

etching, better oxidation, and less surface-state-density, leading to fewer surface defects for better charge-carrier-mobility [5].

Regarding physical properties, Si is a tough/brittle material and at room temperature when stress is introduced, Si can show signs of fracture or shatter after undergoing elastic deformation, which can be attributed to presence of mechanical defects including scratches or dents as well. That is why even and polished Si wafers have more chances of survival under stress as compared to Si wafers retain roughness as a result of cutting or grinding during production process. Multiple studies in the past have been conducted where researchers conducted different tests on Si surfaces to get valuable data on how surface conditioning and temperature can have an impact on fracture-strength. Two scientists Roberts and Samuels [6] carried out fourpoint bending test using rugged silicon surface in the form of a bar under ambient pressure and reported brittle-to-ductile transformation (BDT) at approx. 545 °C. Also, fracture stress of 270 MPa was reported at room temperature. Interestingly Demenet and Rabier [6], they discovered that the temperature at which BDT can be lowered to 275 °C if confining pressure of 1.5 GPa is applied. Fracture tendency of the subject material is highly dependent upon overall wafer quality and how manufacturing practices were followed and post-treatment was carried out.

Furthermore, plasticity behaviour at high temperatures is also presented where the researchers reported that slip systems are activated and dislocations come into existence when limit for upper-yield stress is reached, and also dislocation travels along the plane once they are formed, leading to plastic-deformation and hardening of the lattice. Also presence of O impacts the slip process, for instance in CZ silicon that contains O, after a certain amount of dislocation further dislocations are restricted as more yield strength is required due to O blocking the formation of further dislocation. However, for FZ Si, material under stress is more likely to slip due to lack of O. Also, upper-yield-strength, around 800 to 900 °C elevates if oxygen levels are sufficient enough but if density of dislocations are high then regardless of O levels, there is a reduction in upper-yield strength. So Si wafers can come with different specifications as per requirement and applications; for instance, Epitaxial wafers come with some thick epitaxial layers slipped already meanwhile there are zero to minimal defects or dislocations in the standard Si wafers. For example, during MEMs application, low amount O based Si wafers are used to ensure density of bulk-microdefects are minimized [6].

For chemical properties, Si is an inert material in general but under specific conditions including very high temperatures and extreme chemically active/aggressive mediums, Si can have demonstrated selective chemical reactivity. One of the prominent chemical properties is its ability to form oxidation layer when placed in open air, leading to formation of a barrier/oxidation layer ($SiO_2$) that further protects the material form oxidation, hence making it a suitable material for applications or device fabrication requiring controlled oxidation. Although elemental Si poses no health risks and is non-toxic but on nanoscale level. However, if silica nanoparticles are inhaled; powdered form can lead to some pathological injuries (as per studies [7]). In addition, Si is does not catch flames, but Silane which is one of Si's compounds may demonstrate such behaviour. Corrosion resistance is one of the exceptional benefits of oxidized Si being resistant towards many chemical reactions. But that may change if it is exposed to strong basic- and acidic-media like HF acid, which is used in the oxide-etching process during the microfabrication procedure [8].

Mentioned physical, mechanical, electrical, thermal, and chemical properties bring elemental Si and its compounds as a strong choice for diverse applications across photonics, electronics, energy, and microsystems technology in future as well.

## 1.3 Silicon's application in MEMS, microelectronics, and photovoltaics (PV)

### 1.3.1 Si in MEMS and microelectronics

Micro-electromechanical systems (MEMS) are unique devices that are a combination of electrical and mechanical components in micro dimensions on a chip. MEMS are used widely as key components across different devices based on consumer electronics, aerospace, the automobile industry, pressure sensors, and medical devices. Si's common use in microelectronics since last century has made it a suitable material in MEMS fabrication due to Si's properties like thermal stability, cost-effectiveness, availability, and manufacturing practices. Also, Si being rigid and lightweight at the same time has always been widely used material in microelectronics. Also, Si is chemically stable and can be used for selective-etching to fabricate microstructures as per requirements. Since MEMS require actuation and sensing capabilities, so Si whose conductivity can be tuned via doping facilitates such capabilities in MEMS devices. Chemical vapour deposition on low pressure, deep-reactive ion-etching, and photolithography are amongst the microfabrication methods which are

currently being used to produce MEMS. A few examples regarding MEMS fabrication on Si using etching are presented below in the figure:

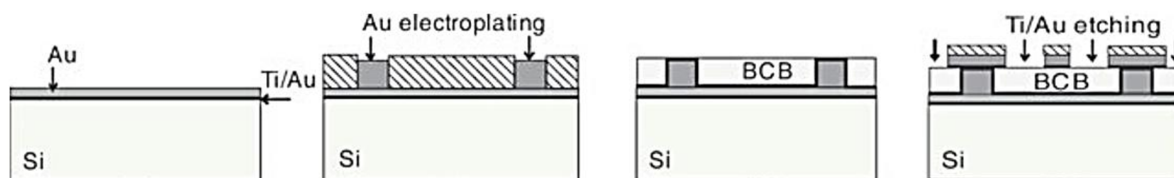



Figure 2: MEMS-fabrication using etching on Si wafer. [9]

Regarding market growth, it has been reported that evaluated forecasts estimated MEMS industry to reach $20B in 2020. However, there is a limitation that hinders its usage in applications requiring flexible materials and optical transparency within smart watches and health technology sensors. Regardless of the limitation and Si has remained most widely used material for MEMS fabrication as a result of novel applications discovered by interdisciplinary scientists and engineers [10].

As for BCB or benzocyclobutene in figure 2, it is a thermosetting polymer and applied to facilitate seamless bonding and sealing of MEMS devices [11]. MEMS have applications in appliances and robotics as sensors and actuators to deliver daily life and industrial scale uses. [12]

### 1.3.2 Silicon's application in PV

Mono- and multi-crystal Si wafers used as a main-base material makes up to 90% of all created solar cells in the whole world due to Si's easier availability as well as physical, electrical, and chemical properties including stability and non-toxic nature. Recently, Si usage in PV fabrication has achieved share of more than 80% of the world's Si supply. The trend has brought PV industry as world's highest consumer of Si wafers even surpassing microelectronics where Moore's law is followed. Since PV sector improves by decreasing overall cost of electricity generated, as in cost-per-watt, more Si wafers are used for that purpose, leading to higher market share of PV industry. Current efforts to slash overall Si wafer costs includes reduction of Si wafer thickness from 150 - 200 µm to 100 µm. However, it poses risk to durability of the PV panels during production, handling, and installation PV panels. However, researchers have introduced a solution to overcome such problem by facilitating a novel Si wafer growth method such as epitaxial growth; that includes growth of

thin Si layers over a base that can be reused and slicing thin wafer from bulk Si block. These methods have proven to decrease overall Si consumption while retaining the required efficiency for PV panels. Also, decreasing PV panel width enhances ratio between diffusion length and cell thickness as seen from figure 3 which presents a trend between efficiency and Si wafer thickness, and that solar cell efficiency maximizes between 20 to 50 μm.

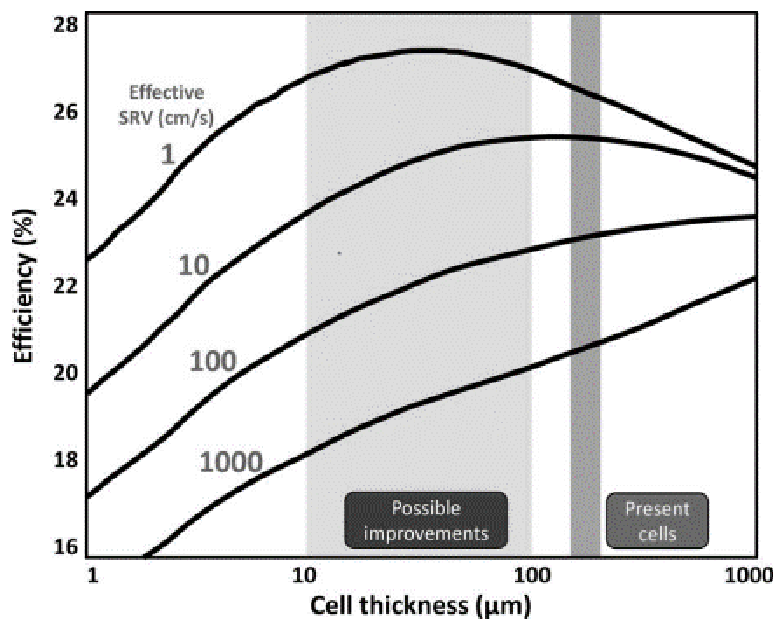



Figure 3: Solar Efficiency as a function of cell thickness [13]

Commercially available monocrystalline Si based solar cells hold efficiency from 18 to 24%, whereas, multi-crystalline Si solar cells have demonstrated up to 18% efficiency. However, efforts are being made to improve solar cell efficiencies by experimenting with new materials, which are integrated with Si to make heterojunction solar cells, as well as improving Si wafer quality via different technologies and methods like Continuous Czochralski (CCZ) for crystal growth and directional solidification technology to mold mc-Si ingots to elevate throughput and eventually aid mass production efforts. Overall, it can be predicted that Si will be the main material in solar cell production for long still, and ongoing research efforts are aimed at bringing solar power to grid parity (a factor where solar power costs the same as other electricity generation sources) [13]

# 2 Literature Review

The semiconductor industry relies heavily on Si and semiconducting properties. Si's surface and its chemistry have been the most studied since last century. Generally, Si is a stable element but when its surface is reformed and dangling bonds come to existence, then a native-oxide layer is formed reaching up to 2 nm in thickness. The layer can significantly impact the Si's electronic properties by inducing interface traps and altering charge states across the surface. One of the most important applications of these oxide is in creation of MOSFETs, although these oxides are not created at room temperature and in uncontrolled media but in specifically control thermal media because native oxide can distort functioning of junctions in semiconducting devices. Surface orientation of Si (100 and 111) plays a key role in its properties as well. The specific crystal orientation can decide how metal contaminants like Nickel can have surface interaction. As mentioned earlier, dangling bonds and surface reconstructions on etched Si and newly cleaned Si can augment metal diffusion and metal adsorption. XPS helps to study surface chemistry of Si and meanwhile ultrahigh vacuum (UHV) reduces contamination and keeps the surface integrity. In the chapter, we will cover all about surface chemistry, important Si crystal orientations, Nickel as a crucial contaminant, and how XPS in combination with UHV is a better approach to study surface chemistry.

## 2.1 Si surface chemistry

Si surface is a widely studied surface and researchers have come up with different methods to gain surface control of Si due to its importance and versatile applications across electronic devices. Other than configuring surface chemistry of film deposition, doping, and etching, its crucial to attain required mesotrophic structures for devices built on single-crystal substrate of Si and properties on atomic levels play a crucial role in this regard. With technological advancements in semiconductors and electronics industry, device size is getting smaller and understanding surface chemistry would result in a greater advantage for efficient semiconductor devices, as quantum properties rely on size.

As it has been discussed earlier that Si possesses diamond-like structure with sp3 hybridization where each Si atom is chemically bonded with 4 others, making a tetrahedral form with lattice constant of 2.35 angstrom and 225kj/mol strength is required to break that bond. Dangling bonds comes to existence when Si is cut and reformed for certain

applications, however magnitude of these dangling bond relies on surface normal's direction on macroscopic level as shown in figure below:

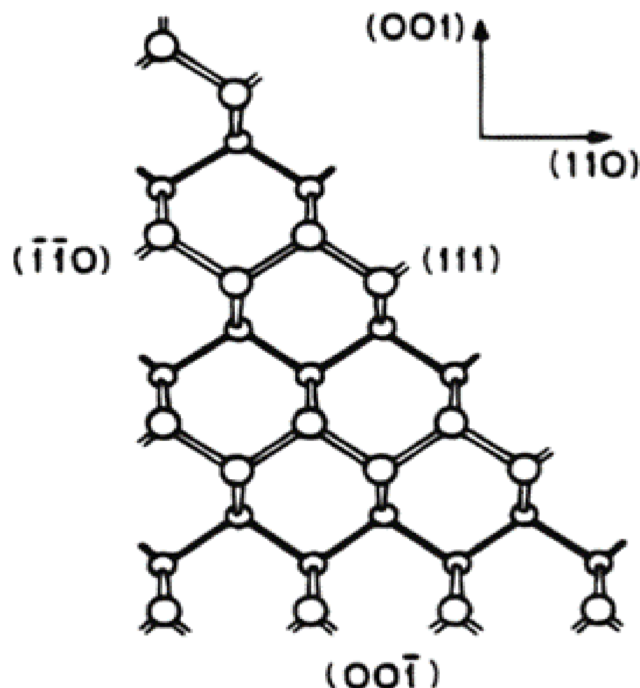



Figure 4: Dangling bonds formation on unreconstructed Si surfaces [14]

Dangling bonds can be observed in figure 4, also number of dangling bonds can be decreased if Si atoms can make bonds again and this will result in lowering the overall surface energy as well as surface reconstructions, since dangling bonds are the main cause of Si reactivity and increased surface-induced energy. However, another way of reducing surface reactivity is to if hydrogen is introduced as a capping agent to Si dangling bonds, leaving no space for further bonding.

### 2.1.1 Si (100)

Unit cell of (100) Si planes retain square geometry, where each Si atom under surface is chemically bonded to four other atoms, 2 above and 2 below the plane. In below figure, surface and bulk atoms are presented, where it is shown that bulk atoms get size reduction as they move away from the surface and reaches more crystal depth.

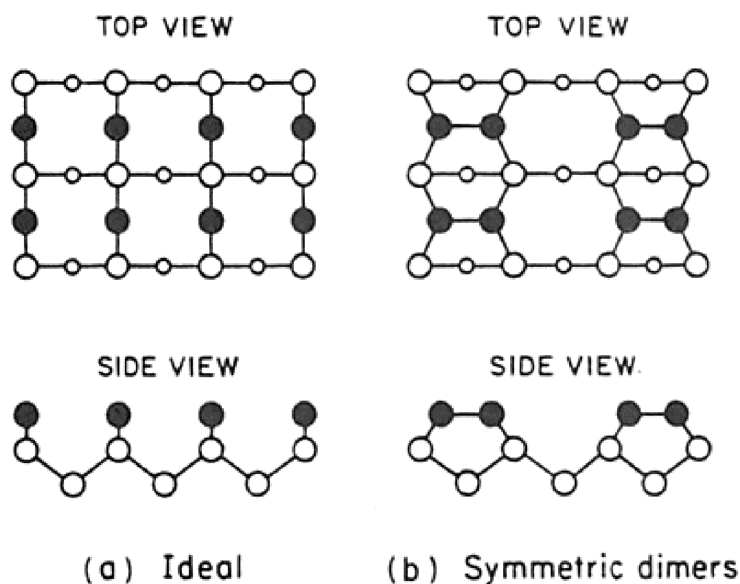
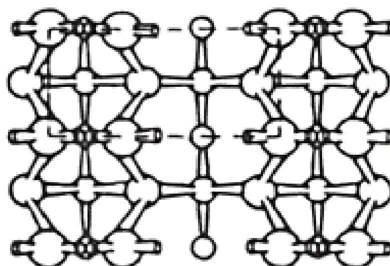



Figure 5: Restructured Si [100] surface with views from side and top [14]

We are also going to discuss briefly on Si (100), which is nominally flat. For flat Si (100), the dimmer model by two scientists Schlier and Farnsworth [14] is the most accepted model, where observation regarding 2 by 1 LEED pattern was reported. In the suggested model rows of dimmers come to existence and results in 50% reduction in dangling bonds. In the reported observation, Si atoms chemically bonds with neighbouring Si atoms within [110] by utilizing one of the dangling bonds (figure 5b).

Further modification in the original model was carried out by Levine and afterwards by Chadi [14]; proposing asymmetric nature of the dimmers, meanwhile asymmetric dimmers can be obtained by positioning two ends of the dimmers in opposite directions, one on the top and other downwards. A variety of dimers (buckled) can be obtained based on their placement order. For instance, symmetric dimers exhibit (2x1) structures in figure 6a, meanwhile figure 6b represents the dimmers, buckled across the same direction.

(a) Symmetric Dimers-(2×1)



(b) Buckled Dimers-(2×1)

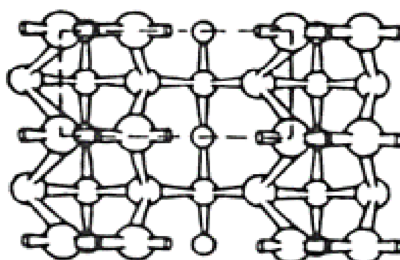
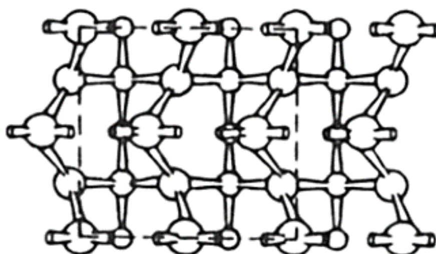


Figure 6: Surface dimmer (2x1) configurations for surface of restructured Si (100) [14]

Furthermore, (2x2) configuration structure can be attained (figure 6c) when bonding of close dimer-rows takes place in uniform/same direction; and (4x2) configuration comes to existence if the bonding direction of nearby-dimer-rows is opposite (figure 6d).

(c) Buckled Dimers-(2×2)



(d) Buckled Dimers-C(4×2)

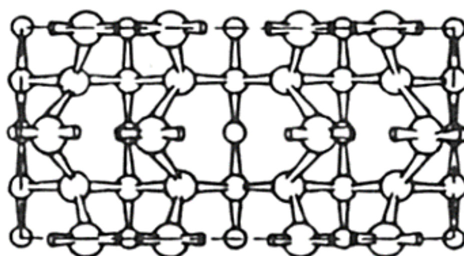
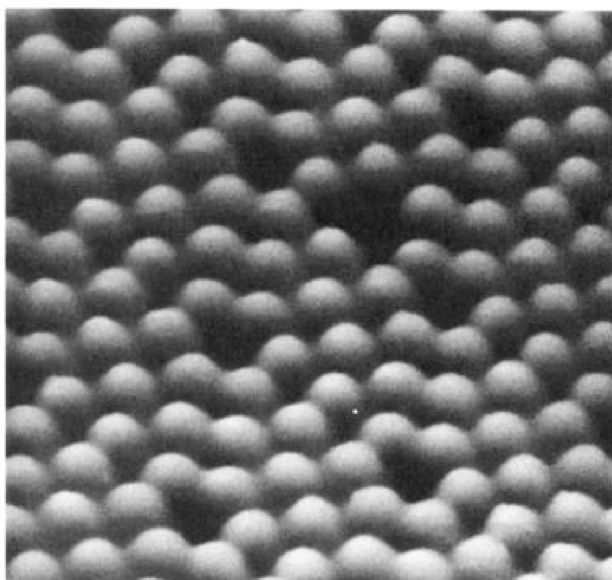


Figure 7: Surface dimmer (2x2) and (4x2) configurations for surface of restructured Si (100) [14]

### 2.1.2 Si (111)

In Si (111) formation, Si atoms are stacked in layers, where one out of the four atoms is bonded in a different layer. Meanwhile, 3 Si atoms form bonds within the same atomic layer and during restructuring there are chances of either formation of one or three dangling bonds. So, formation where there are 3 dangling bonds, the Si surface is more reactive and vice versa for the formation with only one dangling bond. Other than how material is cut, Si (111) surface also exhibits two different reconstructions one after annealing process and second after cleaving, which includes surface-cutting. In Figure 8 (a & b), two 7x7 configuration structures of Si (111) are presented.



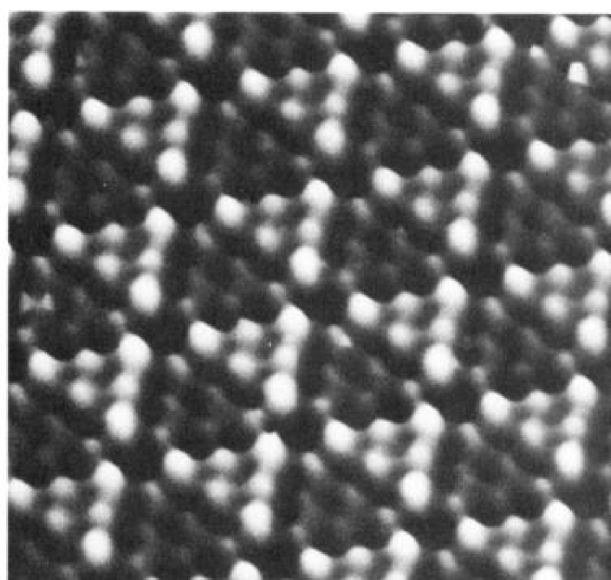




Figure 8: STM scans of Si (111) clean surface with (7x7) structure [14]

Figure 8a shows the unoccupied states for electron when +2V was applied on the crystal, meanwhile figure 8b with -2v bias on the crystal and occupied states of electrons. Adatoms in both of the scans can be observed, also there is a stacking-fault in figure 8b along with a change in center- and corner-adatoms; resulting in a surface with twenty-one dangling-bonds that are normal to the two sub-unit's surface, and saturating all of these dangling bonds is a difficult task with the standard Si unit cells. However, a configuration where six adatoms are present in each of the subunits that occupy sites across a local two by two structure [14] .

## 2.2 Native oxide layer formation

A thin oxide layer is formed on Si when it is exposed to air or water, resulting in a more stable compound of $SiO_x$ of which formation decreases the total (inner) energy and this layer formation depends on multiple factors including doping content, orientation of crystal, and the growth-environment. This layer can grow up to 2 to 3 nm in air (several angstroms within just 10 hours) and meanwhile in purified water, the native-oxide layer forms growth takes place layer by layer. Attaining a better understanding and control over the layer-formation is of great importance as fabrication of many devices relies on it. The layer formation can cause hindrance towards growth of Epitaxial-Si-layers when temperatures are low, resulting in elevation of electrical-resistance as well as losing control over insulating-layer. Growth mechanism for native oxide layer formation is different than thermal based oxide formation. Researchers discovered that surface cleaning high impact the layer generation, so surface conditioning matters and affects how semiconducting takes place and can influence thermal-oxidation kinetics. It has been reported where iron ions in $HNO_3$ has interacted with the oxidized layers and formed Fe(III)-O complex without reacting with Si itself, resulting in more iron impurities. So, it can be implied that intrinsic Si can be a source of Fe impurities that can further produce defects during processes with high temperatures. Similar phenomenon has been observed with Ni and chromium as well; hence, reducing the overall control, the efficiency, and impacting the fabrication process of complex electronic devices.

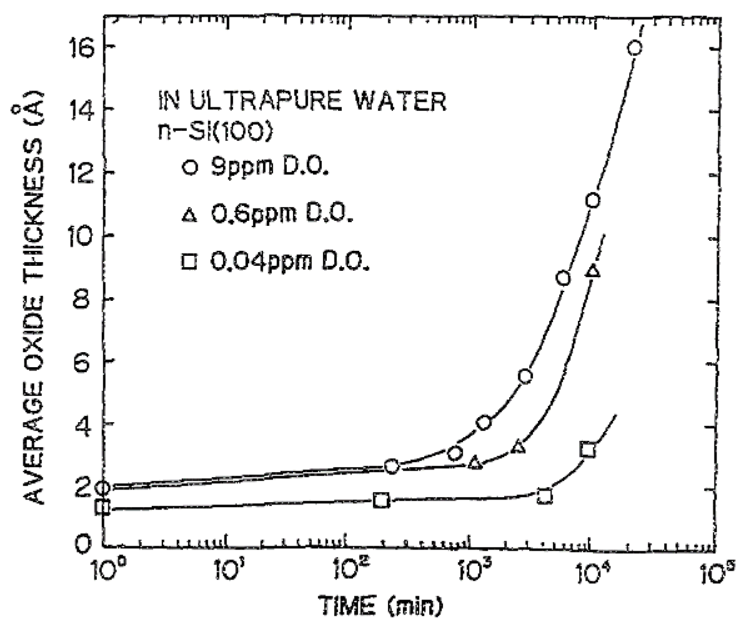



Figure 9: Formation of native oxide layer (thickness vs time) [15]

Figure above has n types Si samples with (100) configuration immersed in distinct dissolved O levels in purified-water and the results demonstrated that layer formation mechanism follows a parabolic path. So, the trend is simple, oxide layer thickness is directly proportional to amount of oxygen and the time passed where sample remained in the water [15].

## 2.3 Si surface contaminations and visual analysis

Si wafer quality, including purity and surface characteristics lay a huge impact devices fabrication; for instance, researchers are still trying to improve efficiency of Si-based solar cells and purity of Si matters alot in this regard. As discussed earlier, oxide layer forms on intrinsic Si and during wafer cutting process, Si surface is prone to coming into contact with some metal contaminations as metal wire is employed during the sawing process. In addition, organic impurities can also occur due to several reasons associated with washing liquids, packaging materials, and environmental factors like air quality and more.
So controlling both inorganic and organic impurities can play a huge role in material purity, which ultimately can result in better semiconducting devices efficiency. Regarding inorganic impurities that occur during Si wafer cutting, how it is cleaned and what material is used also matters. For example, two Si wafers of the same dimensions are cut but one is pre-cleaned with water and other by NaOH/IPA. Then samples were observed by high-resolution mass spectrometer. Sample pre-cleaned with water demonstrates visible stains, meanwhile no stains were observed NaOH/IPA pre-cleaned sample, as shown in figure 10 below. The ultimate result for all the pre-cleaning process may result in better Si wafer performance due to absence of organic/inorganic impurities [16].

Figure 10: Batch 1 pre-cleaned by water and batch#2 by NaOH/IPA [16]

## 2.4 Si wafer contaminations during etching, deposition, and diffusion

Si wafer manufacturing followed by device fabrication is an extensive process and contaminations during processes like etching, deposition, and diffusion can occur at any stage; affecting the overall efficiency of the electronic device.

### 2.4.1 Impurities during chemical vapour deposition

For example, in one of the studies, chemical vapour deposition technique (CVD) is used to transfer graphene on Si/$SiO_2$ surfaces for the resulting product, but residual impurities from metal catalysts like Cu and Ni was also found. The contaminations directly affect on device's performance, for example, Ni, Cu, and Fe, even at low concentrations (~1011 atoms/cm^2) can cause junction-leakage current increase and gradual decrease in dielectric strength. The following XPS spectra in Figure 11 demonstrates the presence of Cu impurity when CVD-deposited Graphene was transferred using metal catalysts Cu and Fe.

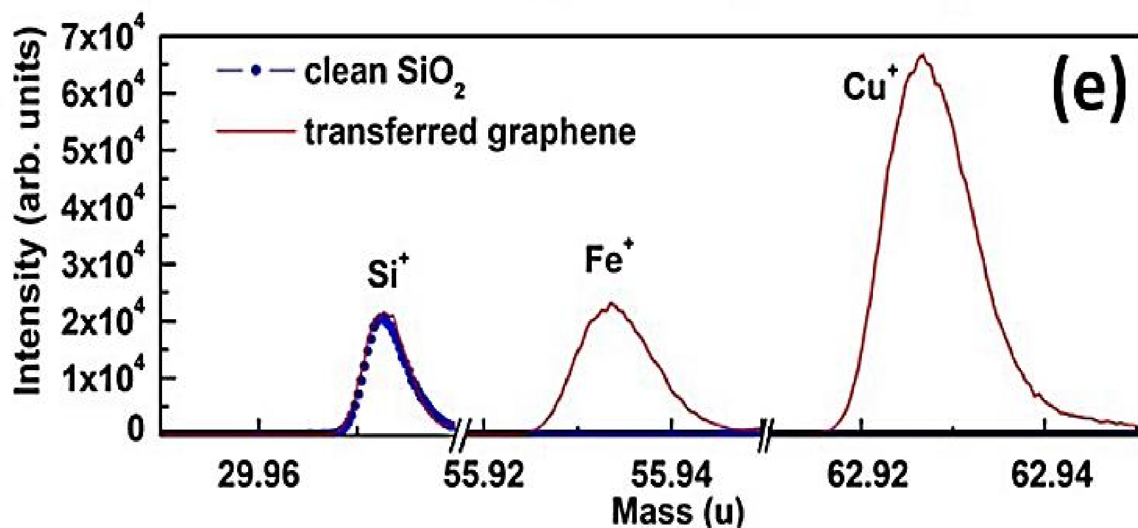



Figure 11: XPS spectra of $SiO_2$ during Graphene transfer via CVD [17]

### 2.4.2 Impurities during etching

Chemical or ion etching process can also cause contaminations via ion-migration across surface of silicon dioxide or depositing the materials that are ejected back to the surface during chemical etching. It is crucial to manage impurities during etching and etching area. Also mobile contamination can be regulated via temperature control. In the following study, Ion etching and contamination is the subject, where layer of $SiO_2$ is the impurity and gets redeposited on Si surface during ion etching process. In the studies, McCaughen et. al [18] uses ion implantation equipment to bombard $SiO_2$ and figured out that $SiO_2$ surface density

can be decreased after ion etching, if annealing is carried out afterwards. Also, he reported that, certain ions like Na, K, and Ar become mobile ions after getting trapped within the layer during $SiO_2$ ion etching with ions possessing high-ionization-potential. In addition, redisposition can occur during the ion-etching process along with sputtering, which is also the main cause of contamination [18].

### 2.4.3 Contamination during diffusion

During metallic diffusion process of dopants like P in n-type Si to enhance their electrical properties, some metal impurities can also find their way on surface or inside specific layers. Also, addition of P can remove impurities like Cr and Fe via process called gettering. During the $P_2O_5$ and $P_4O_{10}$ diffusion process, some residues were observed in XPS spectra, which are elemental P, diffused phosphorous as interstitial/substitutional impurity $P^-$ these are all the residues after the diffusion process has taken place. Also, during the phosphorus diffusion process with Si, silicon dioxide layer (1.3 to 1.4 nm) forms and noticeable elemental phosphorus was present on Si surface, this presence was more notable for wafers contaminated with Fe as compared those Si wafers that had chromium as contamination. The accumulation of P can be attributed to reduction in diffusion length. The study reported the diffusion length of all three phosphorous ions in which $P^+$ had the least diffusion length and elemental phosphorous had the highest diffusion length. In the following figure, we can observe how the P oxidation state varies within Si surface depth with both Cr and Fe doping.

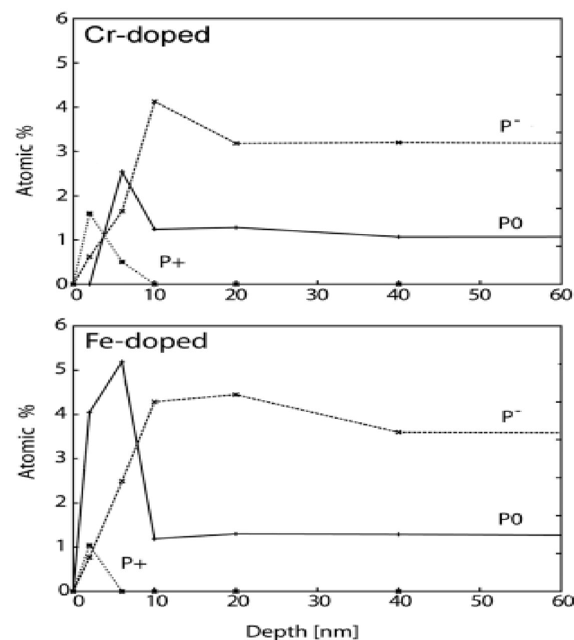



Figure 12: Plot demonstrating trend of P states atomic percentage with depth [19]

## 2.5 Nickel as contaminant and Si semiconductor

Studies on multiple metal impurities when it comes to Si have been conducted; for example, effect of iron, along with its complexes (FeB, for instance) is well known in p-type Si. But studies for n-type Si wafers, which are used in solar cells and some other metallic contaminants have an impact on minority-lifetime are not sufficient. Nickel can be regarded as major impurity as well that can occur in manufacturing of solar cell. Ni can generate participates on Si wafer surface owing to its high diffusion ability even when temperature is low, and it can also augment already present lattice-defects, leading to generations of recombination sites and reducing overall high-carrier lifetime of the solar cell [20][21].

Few of the cons and pros of having Ni as a contamination in Si can be discussed. Cons would include degradation in carrier lifetime, elevation in surface recombination, persistent contamination, diffusion that occurs during heat-treatment, and efficiency decline due to defects in structure. Meanwhile, some of the benefits of having Ni as an impurity can be having manageable growth of Ni-silicide which has potential applications in microelectrocnics like CMOS. Also, proper oxygen introduction can help address performance issues resulting from Ni in CZ silicon.

### 2.5.1 Nickel contamination sources

As mentioned earlier, Si manufacturing as well as Si-based device-fabrication consists of many processes and is prone to being intact with many impurities or getting defects via stress during sample handling, edge profiling, cutting, lapping, and grinding. Consistent acid or caustic-etching is a strong etching process that can be used to remove induced-surface-defects, and MEMS fabrication involves acid etching using KOH solution.

During caustic-etching, rate at which Si-etching takes place reflects highest dependence on doping level as well as crystal-orientation (100, 111). Hence, why caustic etching is being used a lot when it comes to Si manufacturing. Furthermore, the etch rate where KOH solution is used can rely not only on temperature, crystal-orientation, and dopant type but also on amount of KOH solution used. In addition, the researchers also presented a solution to restrict Ni adsorption on Si wafers, and it is achieved by incorporating KOH with less than 200ppm of Triethylenetetramine-hexaacetate along with diethylene-triamine-pentaacetate. Also, they

observed that Ni tends to diffuse more in Si wafer having high concentration of Br doping [22].

### 2.5.2 Nickel's influence on Silicon's electrical properties

Ni, as one of the metal impurity that hold rapid-diffusing characteristics when it comes to crystalline-Si, can occur in the time of high-temperature wafer processing as well as during fabrication of photovoltaic-based materials and in large concentration. As a result of it, during processing of the device, Ni contaminates the surface by creating $NiSi_2$ precipitates, penetrates deeply and impact lattice, and elevates leakage currents along with charge carrier recombination that negatively affect the device performance. Also, it has been reported that p-type Si have demonstrated more negative impact on their performance in the presence of Ni contaminations as compared to N-type Si. In addition, highly intrinsic Si wafers have demonstrated alteration in electrical behaviour (via change in minority-carrier-lifetime) with impurity as little as $<10^{-12}$ $cm^3$ [23][20].

In one of the studies, researchers probed into a p-type Si fused (110) - (100) boundary to analyse how Ni can change the electrical properties and compared it to an undoped (110) - (100) boundary of p-type Si. It was reported that during presence of Ni impurity, number of defect locations or state sites was elevated at the boundary and followed by number of holes being captured by the sites increased ten times. Also, after performing a simulation, Shockley-Read-Hall with recombination model, it was confirmed that the (110) - (100) boundaries defected by Ni under reverse biased configuration exhibit higher leakage currents in comparison to an undoped (110) - (100) interface [24].

Also, there has been a study where they presented impact that Nickel has on silicon's electrical characteristics when it is introduced in a controlled manner via cleaning solutions and later on Si samples with different Ni concentrations were thermally oxidized. Results reported a reduction in carrier lifetime and it was confirmed that even minute amount of Ni transferred via cleaning solutions can render Si wafer's ability to transport charge carriers. Figure 18 below demonstrates a correlation between increased Ni contamination in cleaning solutions and with reduction in the lifetime of minority-charge-carriers.

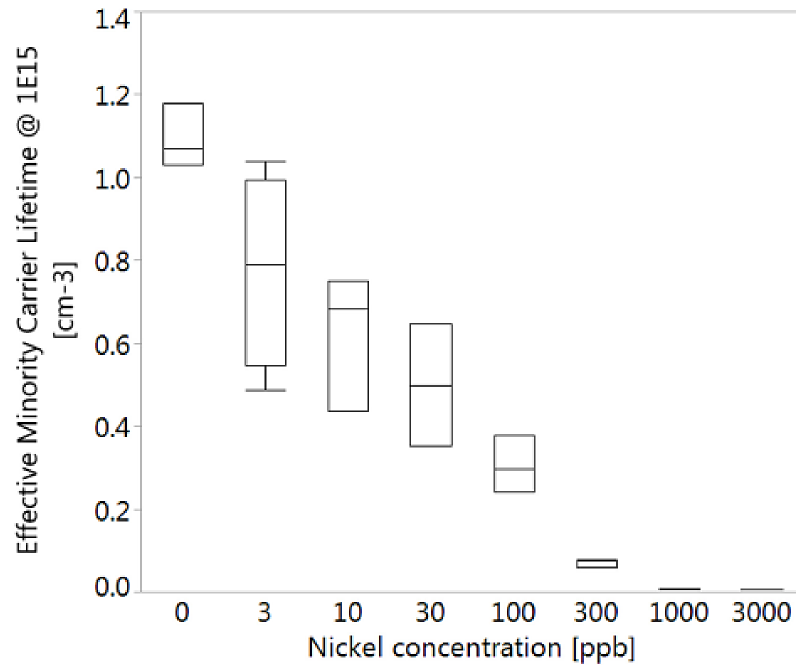



Figure 13: Observation presenting effect of Ni impurity in different concentrations against lifetime of the minority charge-carriers [22]

In addition, when contaminated samples were treated under heat to oxidize, the Ni interacts with the oxidation process in way that aggravates electrical-degradation and it is possible that Ni on surface level during the oxidation process can become electrically active, create traps, or interferes with interface between silicon and oxide layer. [25]

In conclusion, we can say that presence of nickel impurity in Si wafers can directly or indirectly impact electrical properties based on carrier lifetime, surface recombination, leakage current, and overall efficiency of semiconductor devices.

## 2.6 Nickel Silicide and Ni-Si Metal Contacts

By definition, silicide consists of silicon and another metal and mostly they are created at the Si-metal interface. So if the metal is Nickel, then it can be regarded as Nickel Silicide, and they possess desirable characteristics like low-resistance that can be used to make metal contacts for silicon semiconductor devices, as they improve interface connectivity between Si substrate and metal electrode.

There are different types of Ni Silicide and among them Ni-Si is the most outstanding one, as not only it offers low resistance but it can undergo phase transformation at different

temperature ranges to provide NiSi, $Ni_2Si$, and $NiSi_2$ that facilitate remarkable structural/electrical properties for metal contacts in CMOS devices as well as other electronic devices based on Si wafer. [26]

Common method to attain NiSi is via depositing Ni on Si substrate via sputtering or atomic layer deposition ([27]). The created sample is treated under different temperatures to attain different phases of NiSi. For instance, in one of the studies, researchers deposited Ni on Si wafers followed by heating the sample from 200 to 800°c in ranges, and discovered the formation of 3 phases of nickel silicide including $Ni_2Si$ at 200°c on nickel/silicon interface, NiSi develops at Si-$Ni_2Si$ interface at 350°c, and $NiSi_2$ comes into existence from NiSi when temperature reaches above 750°c. Furthermore, the disilicide was grown on (110), (111), (100) Si surfaces, in an epitaxial manner, and synthesis was observed via X-ray diffraction along with electron microscopy. [28]

Researchers also reported the final product of Ni on Si reaction relies heavily on Si nanowire (SiNW) orientation, proving that interface geometry and lattice are crucial when it comes to silicide growth and nucleation. For instance, with [112] SiNW, we get $Ni_2Si$ when treated with 350 - 700 °c range, 2mins and observed a distorted silicide structure probably due to generated stress in the nanowire. Later, NiSi was identified in [111] SiNW when exposed to 700°c for 2mins and before that $NiSi_2$ was obtained at 450°c for 2mins. [29]

From electrical engineering point of view, NiSi nanowires with <50nm fabricated via top-down method demonstrated no change in resistivity at room temperature when widh of nanowires was decreased to 23nm, but at cryogenic environment electrical resistivity did increase when nanowires width was reduced. Further studies revealed the limit of 22nm wire width for successful implementation as nanoscale nodes without facing any device performance degradation. [30]

Also, a research presents the overall impact of nickel-silicides on p-type Si doped with boron. In summary, researchers presented that resistance induced by bulk impurities enhanced by 3-4 factor during presence of $NiSi_2$ film (50 to100 Å) during to boron's transfer towards the Si surface and the newly developed $NiSi_2$ film. [31]

Metal contacts are crucial when it comes to bridging the gap between Si substrate and metal electrodes for successful transfer of charge carriers (holes or electrons) as well as to enable many current semiconductor applications along with fabrication of microelectronic devices. A reliable and low-resistance metal-to-Si contact is important to achieve high device performance, miniaturization, and efficiency. Currently, these contacts based on their characteristics are classified into 2 major types: Schottky and Ohmic contacts [32]

Since, metal contacts govern a device's performance in a long run so it is crucial to study and find way to regulate metal contacts' properties. One factor, Schottky barrier height ($\Phi_b$) which is required energy for seamless charge transfer over metal and semiconductor contact. Also, it is key element to evaluate Schottky and Ohmic contacts' electrical performance. It can be regarded as electron affinity of the semiconductor and work function of the metal. $\Phi_b$ in case of ohmic contacts impacts overall contact resistance whereas reverse leakage current and turn-on voltage along with other electrical characteristics as well as performances when it comes to Schottky contacts.

A lot of studies has been conducted on $\Phi_b$ for different contacts to figure out an optimized value and properties suitable for certain device applications. A brief explanation on how $\Phi_b$ forms can be understood by below figure 14a, which demonstrates energy figure of n-type semiconductor and a usual metal. Whereas, figure 14 b presents alignment of Femi levels for both semiconductor and metals when they come into contact with each other and electron transport takes place.

A relation, also known as The Schottky and Mott relationship, can be deduced from charge transport and is the difference between semiconductor's electron affinity ($\chi_s$) and metal work function $\Phi_m$ and is equivalent to $\Phi_b$. So one can conclude that Schottky barrier height can be tuned if we choose appropriate metal with specific $\Phi_m$. However, $\Phi_b$ seemed not relying completely on $\Phi_m$ due to many visible and hidden factors such as, Fermi-level pinning, surface states, and gap states induced by metal. [33]

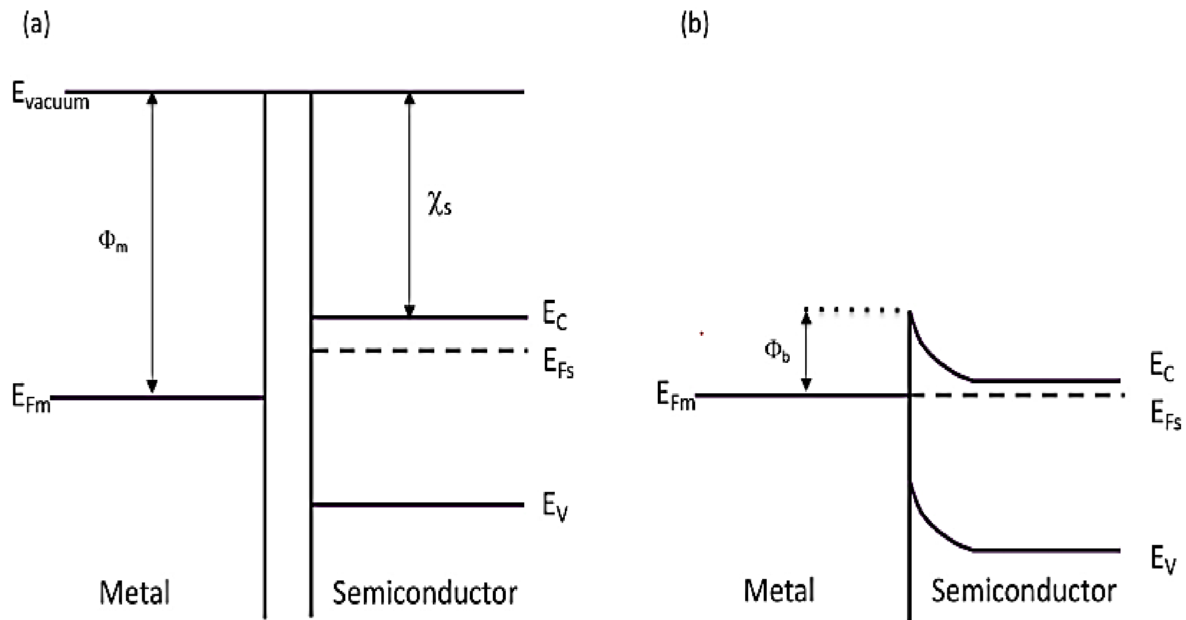



Figure 14 a and 14 b: Before and After contact $e^-$ energy band diagrams for n-type semiconductor and a metal [33]

A research investigated $\Phi_b$ for Ni-Si contacts for p-type (100) Si across a temperature range of 60 to 300K in a forward-biased setting. The results showed that Schottky barrier heights were between 0.205 and 0.513 eV. But on didoes that were annealed at low temperatures reported low barrier heights as well, for instance, NiSi/Si diodes exhibited 0.67 eV, and $Ni_2Si$/Si reported 0.67ev. [34]

In case of NiSi's application in CMOS, they have been used in them quite for a while now as well as in high-performing devices with node size 90nm. Few of the pros using NiSi on large scale CMOS devices can be that: 1) Ni possesses superior scalability as compared to $CoSi_2$ when it comes to thin polysilicon lines. 2) Tested for better electrical compatibility in case of SiGe. 3) NiSi requires less Si to meet sheet resistance requirement in contrast to $CoSi_2$. 4) Si to Si interface demonstrates better electrical compatibility for NiSi. 5) NiSi, when used as a self-aligned silicide, provides better dopant redistribution.

However, there are some challenges in using NiSi as a metal-semiconductor contact like narrow line effects also thermal stability issues and limited applications in higher temperatures due to Ni diffusion. [35]

## 2.7 Surface Analysis Techniques

Surface study and analysis in today's era are benefiting and enhancing ongoing manufacturing practices, research, and quality control across several industries. Industries are actively using surface analysis for biotechnologies, lightweight materials, energy storage, and characterization of nanomaterials. Over time, a variety of analysis techniques have been developed and implemented to investigate chemistry, physics, and biology of surfaces. Advancements in the field of applied surface analysis and surface science have benefited from the application of such techniques.

Ability to detect and characterize contaminant traces are of very importance for performance and stability of semiconductor devices. As discussed earlier, transition metals like Ni, Fe, and Cu even with a very small concentration can degrade performance and alter electrical performance of Si wafers and electronic devices by acting as recombination centres and altering minority-charge carrier lifetimes. In order to tackle the challenges, it is crucial to have information about elemental composition, chemical-states, and depth profile, and that is where we require bulk sensitive and surface sensitive techniques.

To probe surface reactivity and characteristics effectively we need information about surface like physical topography, chemical structure and composition, atomic structure, and bonding and electronic state of surface molecules. As it a lot of information not a single technique can cover all of this information and for applied surface analysis, we may require a combination of techniques/characterizations.

Some of the widely implemented techniques for surface studies and chemical analysis: Auger Electron-Spectroscopy, ESCA also known as X-ray photoelectron spectroscopy (XPS), Secondary Ion Mass-Spectrometry, Molecular Surface Mass Spectrometry by SIMS, Low-Energy Ion Scattering along with Rutherford Backscattering, Vibrational Spectroscopy from Surfaces (including EELS and Raman Spectroscopy), Low-Energy Electron Diffraction (LEED), Scanning Tunneling Microscopy (STM), Atomic force Microscopy, and currently more than 50 techniques are in execution to enable seamless surface studies.

We can classify surface study techniques based on radiation/signal source and the sort of information can be extraction:

- Electron analysis for chemical analysis (ESCA) or XPS:

Working principle of XPS is based photoelectric effect. X-ray photons with specific energy are bombarded on surface that ejects electrons from atoms' orbitals with specific kinetic energies and binding energies. Such electrons can provide information about electronic states and chemical composition because sample chemical composition is that a certain element's binding energy is closely dependent on its atomic environment (for example, Si 2p photoelectrons emitted from Si-Si and Si-O environments have different binding energies).

- Auger electron spectroscopy (AES):

Similar to XPS and instead of X-rays, surface is bombarded by keV electron beam. Also, AES provides higher spatial resolution for imaging and elemental mapping, but less detailed information when it comes to chemical states

- Secondary ion mass spectrometry (SIMS):

There are two modes to this technique, molecular and dynamic SIMS. Similar technique is used in both modes to extract information where the target surface is exposed to high energy beam of ions and ejected ions are analysed via mass spectrometer. The spectroscopy can be used to study elemental or molecular composition of thin films and other solid surfaces.

- Ion scattering spectrometry (ISS):

The technique is slightly different than SIMS but high energy ion beam is used here and results about element identification as well as surface structure are obtained by analyzing kinetic-energies and scattering angles of the primary ions from beam.

- Infrared Spectroscopy:

Currently Fourier Transform Infrared Spectroscopy is being used widely, with surface exposed to infrared light that generated vibrational frequencies within surface layers. The analysis results and information about functional groups are obtained via losses in photon energy used to make molecules vibrate.

- Electron energy loss spectroscopy (EELS):

The target surface is exposed to electrons having low energy of few electron volts and as a result electrons lose energy after interacting with the surface. The change in energy or energy distribution is then observed to deduce surface information.

- Low energy electron diffraction (LEED)

Effective for studying surfaces of a single crystal. Low energy electrons (in the range of tens of ev) are employed and diffracted from the target sample. Then the backscattered electron provides a diffraction pattern and surface information is deduced.

- Scanning tunnelling microscopy (STM)

Sharp metal tip is used in this spectroscopy for a conducting surface to obtain information about surface morphology at atomic scale. Electric current flows between tip and the surface, the tip does not touch the surface but hovers over it and then quantum tunnelling current is measured between the surface and the tip to attain plot surface topography at atomic level precision with high resolution

- Atomic force microscopy (AFM)

Functions in similar way to AFM but can be executed on non-conducting surfaces as well. Information about surface's topography is achieved by analyzing force generated between tip and the sample surface.

Some of the spectroscopies including electron spectroscopies which are sensitive and can be used to study semiconductor include AES, SIMS, STM, XPS, and LEED. So we can summarize their uses for semiconductors including the information that can be derived along with limitations:

**AES:** Can be used for elemental analysis and detection except for He and H, delivers 10-50% of precision based on peak shape oxidation shape. Detection limit during point analysis (0.1 to 1 % of monolayer similar to $10^{12}$ - $10^{13}$ particles/$cm^2$). Electron attenuation and escape depth for electrons with energies < 2kev is 1-3 nm, which is normal for auger transitions. Some modern instrument with electron sources of 30kev can achieve resolution limit between two points with 20nm distance (resolution limit).

**XPS:** XPS or ESCA comes under group of electron spectroscopy and can be used to study elemental composition for a variety of samples surfaces with depth profiles upto 10 nm into

the target sample. It is a non-destructive method and takes bonding orbitals and valence-band electron distribution around the core levels into account. In other words, core-level shifts can appear for example in Si 2p spectrum when Si atoms form bonds with oxygen. Because valence electrons are concentrated around O atoms, larger work (i.e. larger binding energy) is required to remove Si 2p core electrons due to the O bonds.

**STM:** Comes under class of Scanning Probe Microscopy and can provide details like topographic information and electronic structure on an atomic-scale. In addition, insights about surface reconstructions and dangling bond, band structure of semiconductors, and present defects can also be retrieved. Although, for STM, surface has to be conductive. [36][37][38]

# 3 Methods

In this chapter, experimental details including sample preparation and treatments, along with specifications of implemented XPS characterization, will be discussed.

## 3.1 Experimental Setup:

The experiments were conducted to investigate (100) n-type Si wafer with sample length (~ 10 × 3√5 × 0.3 mm) behaviour under high temperatures and UHV setting (pressure below 5× $10^{-8}$mbar) using Omicron XPS. Mg Kα x-ray source with 1253.6 eV photon energy was employed to record photoelectron spectra. Also, X-ray source is not monochromatized and have spot size around 3-4 mm. Samples were heated in UHV system under constant current mode and temperatures were assessed via infrared pyrometer. Additionally, specific regions on Omicron XPS machine were selected to detect Si2p, Ni2p, C1s, and O1. Three mirror-polished Si substrates were used in the experimental setup with following temperature details:

### 3.1.1 First Observation and Sample 1 (S1):

- Clean Si substrate with native oxide layer loaded on Mo sample holder prior to placement in UHV chamber
- Performed XPS scans at room temperature for after each heat treatment: Room Temperature, outgassing sample at 600°C (30mins), after annealing at 600 °C (30 min), 800 °C (30 min), 1000 °C (5 min), and 1200 °C (5 s) were performed.
- After the above sequence, the sample was again heated to 1000 °c for 20 min, and additional measurements were performed at varying sample stage positions (from L: 12 to 10 mm).

Following are the current and voltage values for S1 at specific temperature:

| Annealing Temperature °C | Current (A) | Voltage (V) |
|---|---|---|
| 600 | 1.2 | 0.7 |
| 800 | 3.5 | 6.7 |
| 1000 | 6.7 | 8.6 |
| 1200 | 13.6 | 13.1 |

### 3.1.2 Second Observation and Sample 2 (S2):

- To pinpoint closest temperature where Ni2p appears on XPS spectrum under thousand degrees, an additional heating experiment was conducted on same sample as S1 under similar UHV and XPS conditions
- First scan was performed at room temperature, followed by scans after annealing Si substrate at 600°C and 900°C for 30 minutes both.

Following are the current and voltage values for S2 at specific temperature:

| Annealing Temperature °C | Current (A) | Voltage (V) |
|---|---|---|
| 600 | 1.2 | 0.7 |
| 900 | 5.1 | 7.6 |

### 3.1.3 Third Observation and Sample 3 (S3):

- Si substrate was dipped into Hydrofluoric acid for 5 seconds to remove native silicon oxide layer followed by 30 mins dip in deionized water.
- Cleaned sample was dried with nitrogen air and plastic tweezers were used in sample handling and mounting. Sample was then placed in the same sample holder.
- Total air exposure time, where sample was exposed to air after cleaning and loading into UHV chamber was 12.5 minutes.
- To check Ni contamination behaviour HF cleaned Si substrate behaviour at room and high temperature setting, S3 was exposed to following annealing temperatures:

| Annealing Temperature °C | Current (A) | Voltage (V) |
|---|---|---|
| 600 (30 mins) | 1.2 | 0.7 |
| 800 (30mins) | 3.5 | 6.7 |
| 900 (30 mins) | 5.5 | 7.2 |
| 1000 (5 mins) | 7.2 | 8.7 |
| 1200 (5 sec) | 13.2 | 13.2 |

After all the heat treatments, samples S1, S2, and S3, where analysed further using Thermo Scientific Nexsa surface analysis system, which is equipped with monochromatized Al K-alpha X-ray source. Such high resolution system comes up with an option to select points and point sizes that one needs to analyse on a sample. In our analysis, point size used was around 300 μm and hence we were able to place So samples S1 and S3 before and after heat and HF treatment were selected to observe the changes in the sample. The following points were selected for scans:

Figure 15: Selected scan points for Sample 1

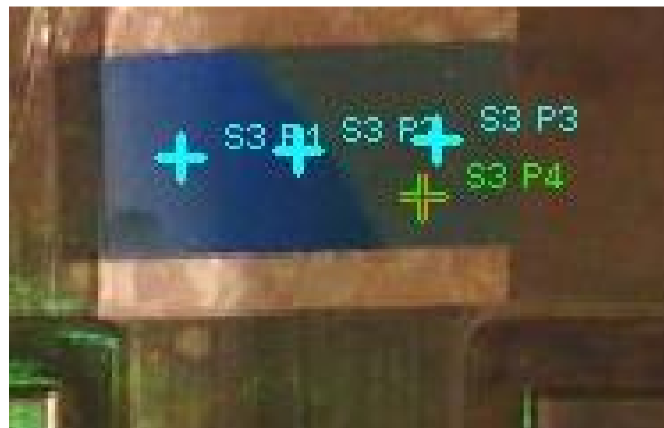



Figure 16: Selected scan points for Sample 3 before HF cleaning and Heat Treatment

Figure 17: Selected scan points for Sample 3 after HF cleaning and Heat Treatment

Also, in Omicron XPS, 5 scans were performed to detect each of the elements Si2p, Ni2p, C1s, and O1 in the specified regions. The selected regions in electron volts for scans were: 115 to 90 (Si2p), 300 to 280 (C1s), 550 to 525 (O1s), 890 to 850 (Ni2p), and 900 to 0 for XPS survey for all S1, S2, and S3 samples.

Additionally, data obtained from both XPS systems were converted, sorted, and quantified using CasaXPS software for analysis and curve fitting.

# 4 Results and Discussion

In this chapter, results obtained from three sets of experiments conducted in ultrahigh vacuum settings and designed to evaluate the evolution of treated Si surfaces under high temperatures, native oxide desorption on the samples at different temperatures, and the behaviour of nickel contamination. Performed analysis includes:

- Sample S1, a mirror-polished Si wafer containing native oxide layer, heated sequentially under UHV at progressively higher temperatures.
- Additional experiment on the same wafer as a Sample 1, heated specifically at 600 °C and 900 °C for 30mins each to analyse the onset of nickel surface contamination. The resultant sample is named S2
- A Si wafer chemically cleaned by HF etching, analysed over a similar temperature range as sample 1, but with an additional heating of 30mins at 900 °C for comparison with the native oxide sample S1

For each particular Si sample, XPS survey spectra and core-level spectra for Si 2p, O 1s, C 1s, and Ni 2p were obtained from using two different XPS systems. Additionally, measurements were performed at multiple spatial points to assess surface uniformity and distribution of Ni contaminant. The results provide insight into oxide desorption dynamics, impurity diffusion mechanisms, and the impact of pre-cleaning procedures.

Experimental setup for observation has been discussed in section 3.1.1. and figure 18 and 19 presents data gathered in 1$^{st}$ experiment containing Si wafer with oxide layer. Figure 18 a), b), and c) demonstrates expected peaks of C, Si, and O at room temperature. As Si sample was sequentially heated to 600 °C (30mins, for gassing out), 800 °C (30mins), 1000 °C (5mins), and 1200 °C (5 seconds), a consistent decrease in O 1s intensity was observed. This trend supports thermally activated desorption of the native $SiO_2$ layer. When temperature reached 1000 °C, the oxygen peak was significantly reduced and with lowest value upon reaching 1200 °C for 5 seconds. Same was observed in case of C1s peak. On the contrary more Si2p content was observed with the increase in temperature.

Figure 19 reveals clear presence of Ni contamination starting from 1000°C, normally Ni2p peaks appear around 856eV for $Ni2p_{3/2}$ but a slight shift towards higher binding energies can

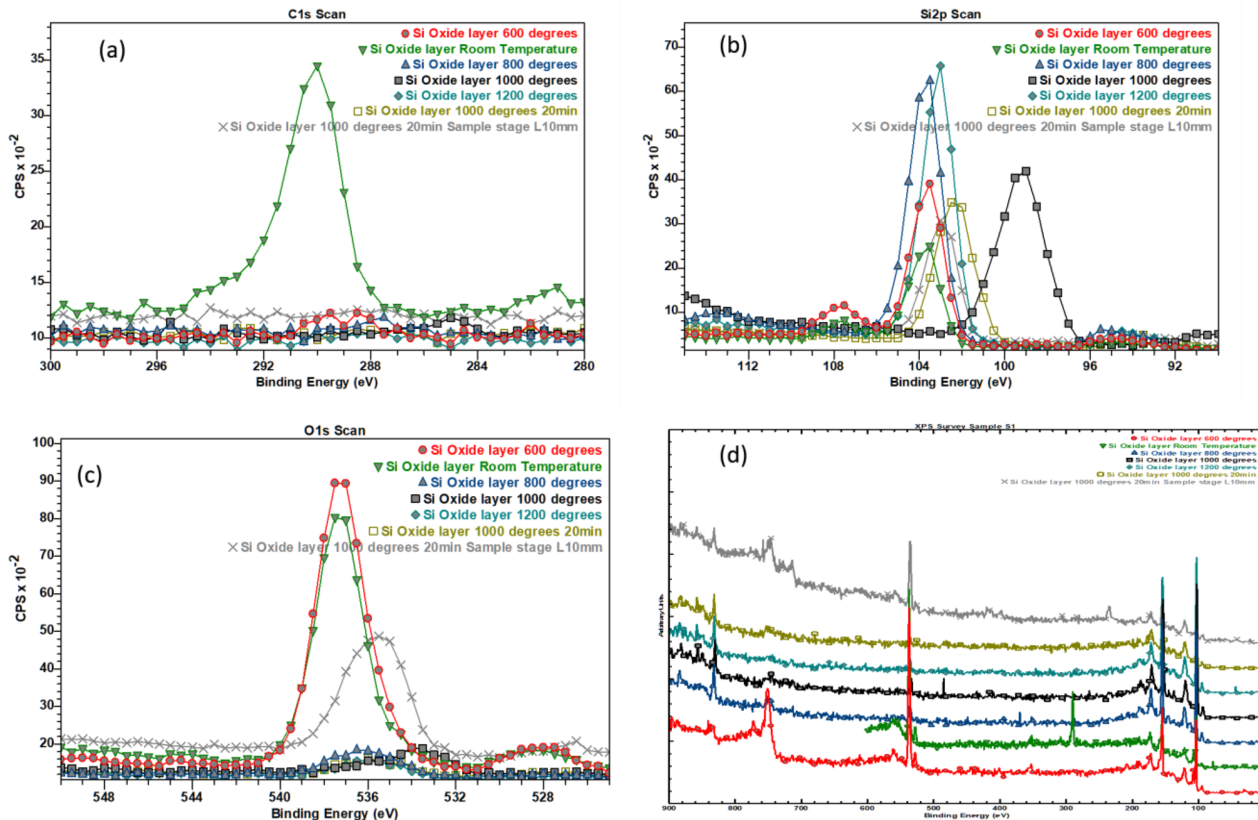



Figure 18: S1 XPS spectra represents a) C1s Scan b) S2p Scan c) O1s Scan d) XPS Survey

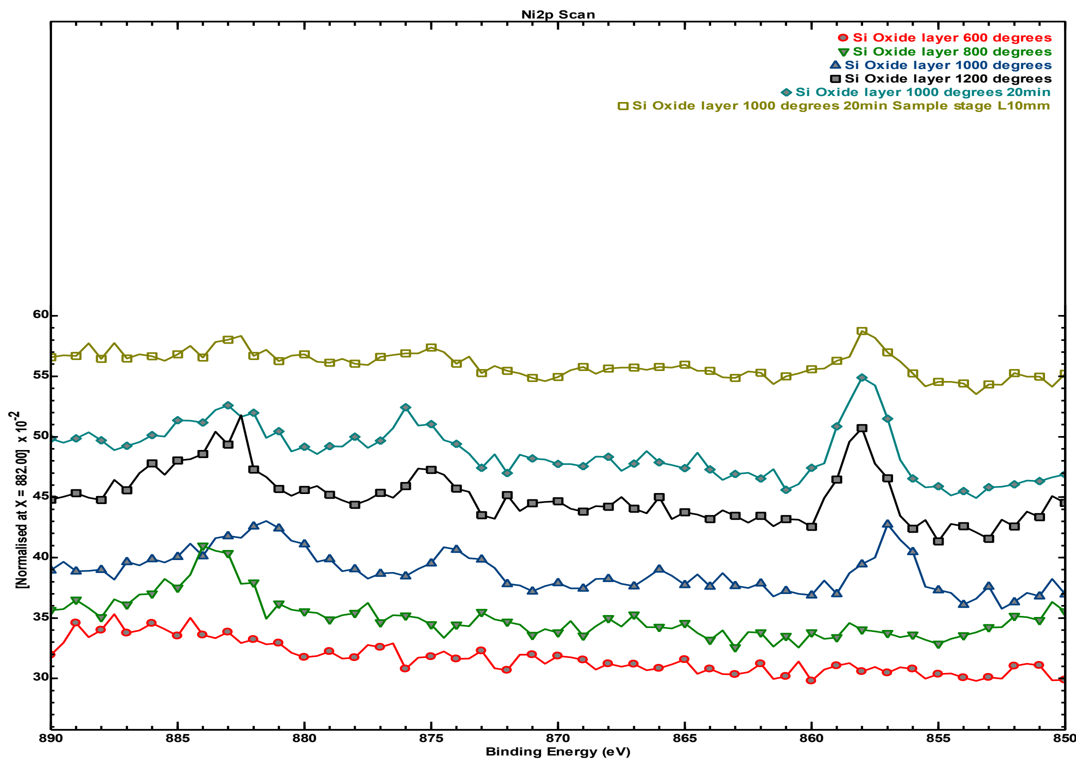



Figure 19: Ni2p contamination under different temperatures for S1

be attributed to charging build-up of the sample that creates a positive charge on Si surface especially in . But appearance of Ni2p contamination is evident in higher temperatures.

Starting from 1000°C, a significant rise in Ni intensity can be observed with increases in temperature. Such phenomenon can be caused by several factors. It is possible that Ni was already present in “as received” Si substrate and higher temperatures caused the enhanced mobility of Ni atoms that resulted in surface segregation and thermal diffusion.

Also, at high temperatures, Ni interstitials can diffuse rapidly through Si lattice and furthermore the removal of the native oxide layer (which otherwise reduces the signal) further reveals segregated Ni at Si surface. A study [39] has discussed the diffusion rates of Ni in Si substrates at higher temperatures.

To verify appearance of Ni at even lower temperature than 1000°C, another Si substrate with oxide layer was taken and given same heat treatments, except this time, going straight to sample was heated at 900°C after 600°C, and figure 20s confirms appearance of Ni contamination at 900°C, exhibiting that it is possible that thermodynamic driving forces favours Ni segregation to the surface to reduce system’s free energy. Meanwhile, O, Si, C demonstrated same behaviour as figure 18 (a, b, c) and were not included this time.

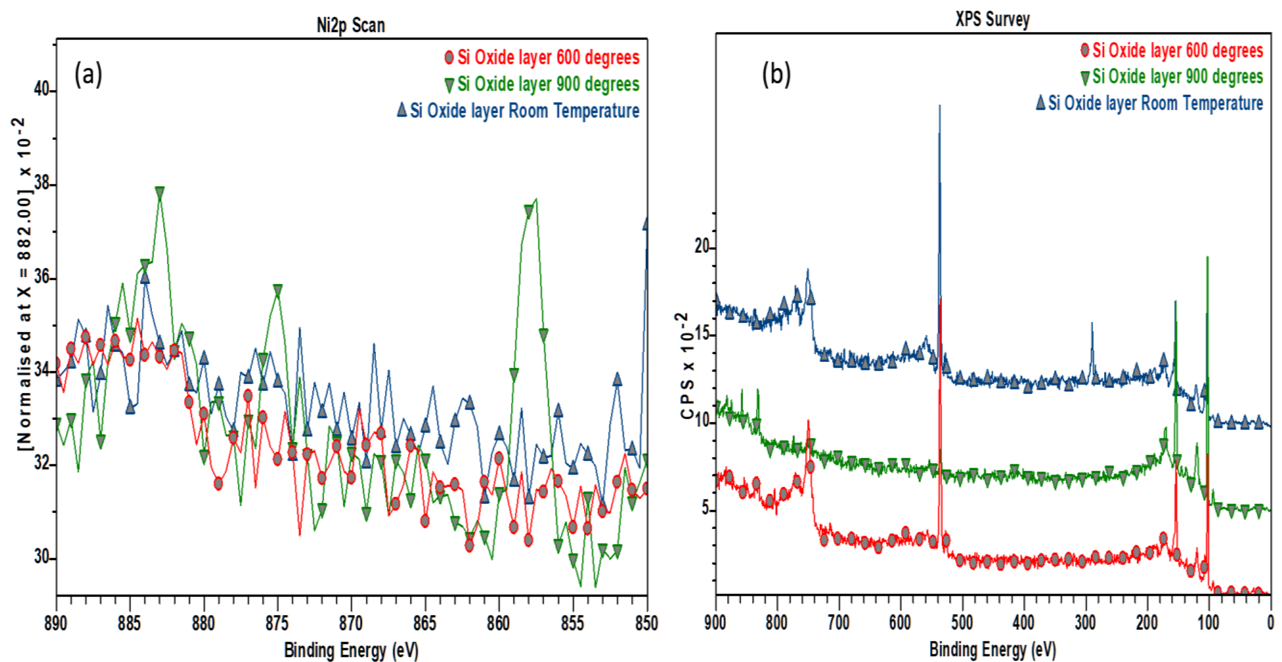



Figure 20: S2 a) Ni2p Scan  b) XPS Survey of Si Surface after Heat Treatments.

In next experiment, sample 3 was analysed using high resolution Thermo Fisher Scientific Nexsa before going through HF etching and UHV heat treatments. In conducted scans, figure

surface Ni was already present along with its satellite peaks in figure 16, selected points 3 and 4, of S3.

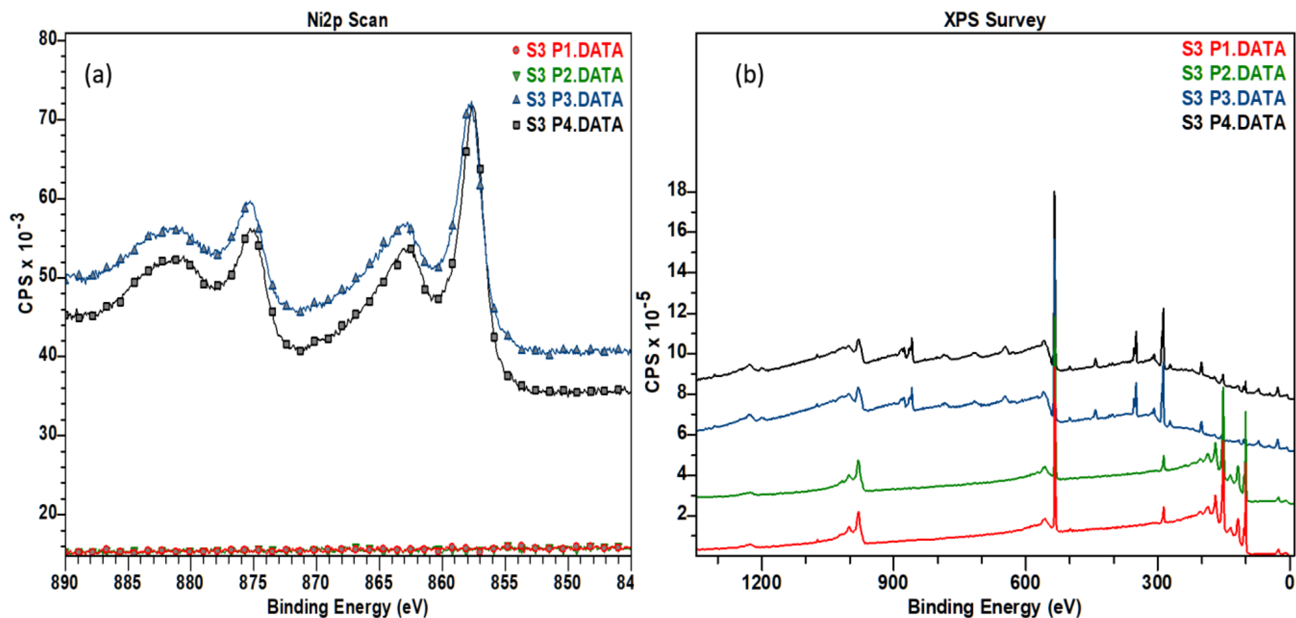
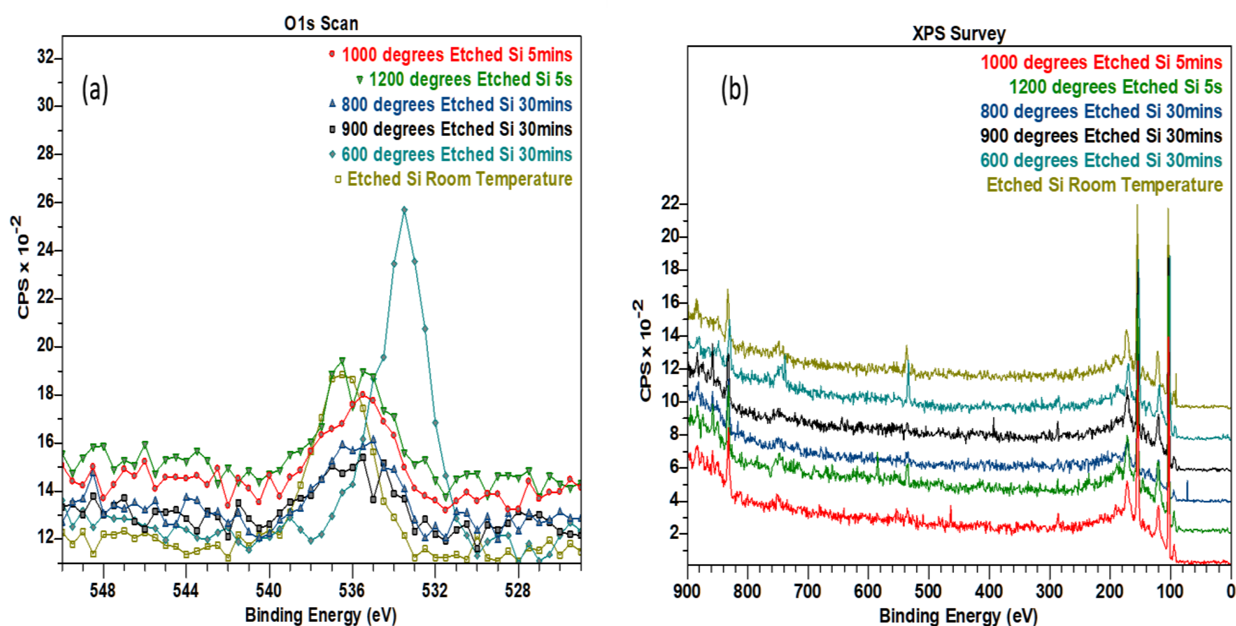



Figure 21: S3 before HF Treatment, a) Ni2p Scan b) XPS Survey

So for experiment 3, above sample was taken and cleaned with HF solution to remove contaminations and oxide layer to reveal Ni behaviour under UHV heat treatments. Cleaned sample was then treated with high temperatures and XPS readings were taken at room temperature, 600 °C, 800 °C, 900 °C, 1000 °C, and 1200 °C



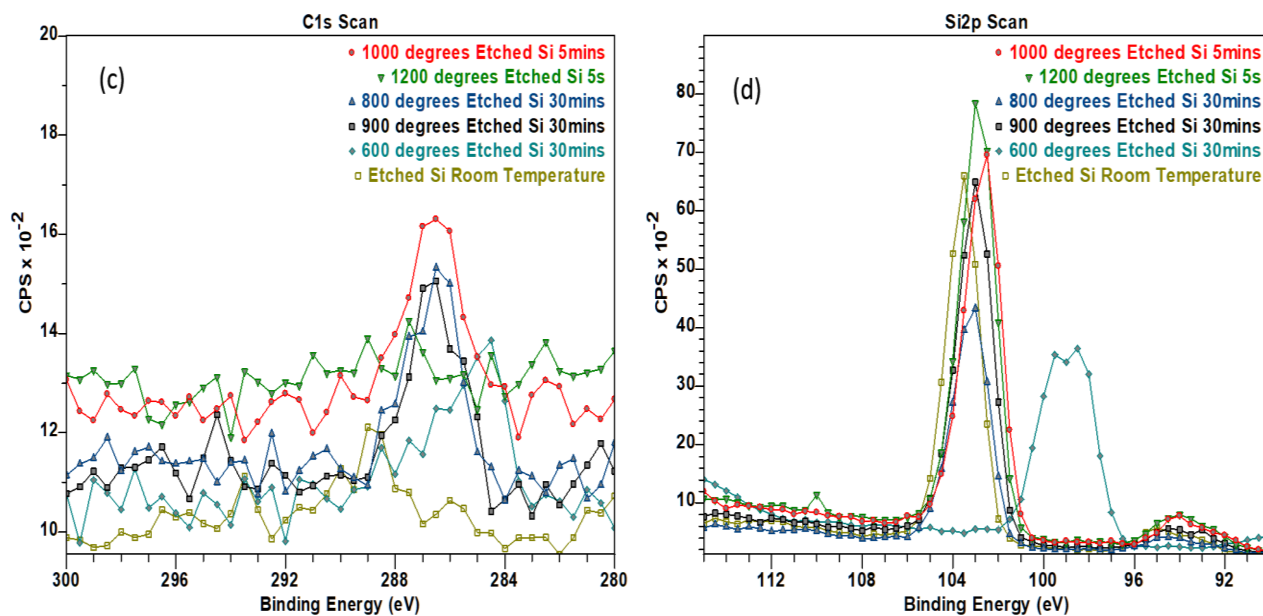



Figure 22: S3 HF Treated XPS spectra a) C1s Scan b) XPS Survey c) O1s Scan d) S2p Scan

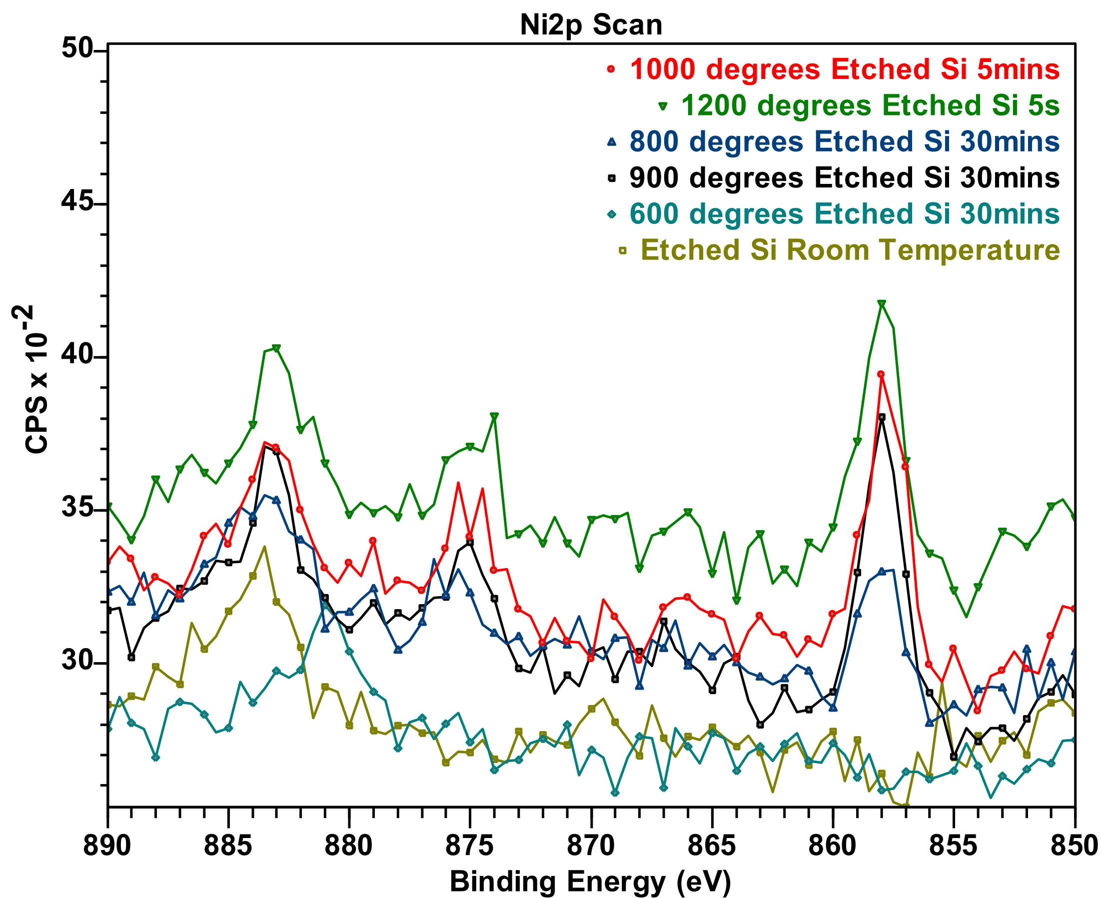
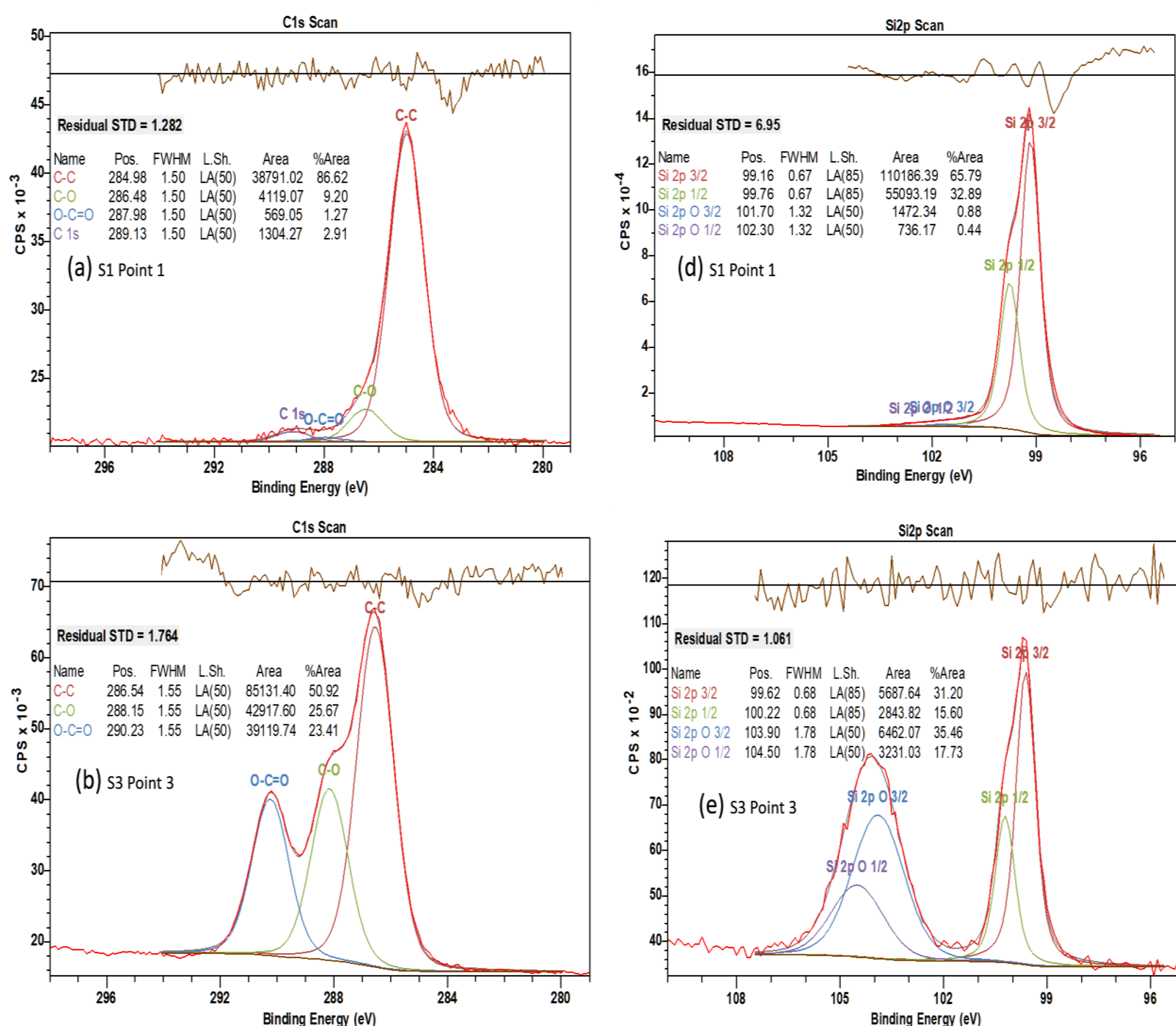



Figure 23: HF Treated S3 Sample Ni2p Scan

Figure 22d, XPS Si2p scan confirms removal of silicon oxide layer. C1s spectrum shows highest carbon content at 1000 °C and lowest at room temperature, suggesting that etching did remove surface contaminations. In Si2p spectrum, slight oxide layer peak is observed at 600 °C, which later on at higher temperature gets eliminated. Additionally, higher oxygen content is also detected at O1s scan at 600 °C, it can be said that Si substrate was getting re-oxidized. From figure 23, Ni contamination begins to emerge with rise in temperature, highest peak was detected at 1200 °C since, the sample already had nickel before HF treatment, that is why we can observe Ni content even at room temperature after HF etching. However, Ni content in HF-treated Si Sample 3 is slightly less than non HF treated Si sample 1.

Sample 1 and HF treated Sample 3 were analysed with high-resolution Thermo Fisher Scientific Nexs XPS after all heat treatments to get information. Following are the curve fittings for C1s and Si2p for sample 1, sample 3, and HF-Treated Sample 3 in figure 24:



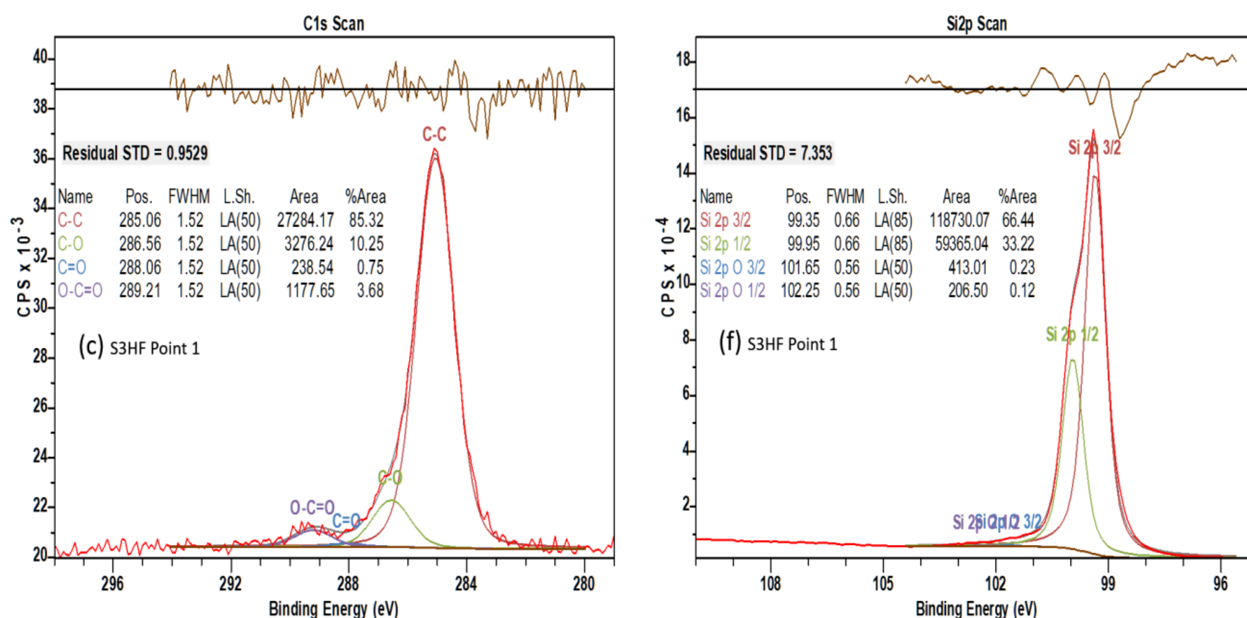



Figure 24: Curve fitting for Sample 1 and Sample 3 with and without HF treatment

Curve fitting graphs for all S1, S3, and HF S3 demonstrates existence of chemical states that were not possible to see in XPS system where samples were heated and observed. HF treatment Si2p scan (figure 24f) reflects significant reduction in oxide states and same goes for (figure 24f), where oxygen content has reduced from carbon as a result of etching and high temperature annealing of the samples. Also, information about Ni2p from the sample scan points for all S1, S3, and S3HF is presented in figure below:

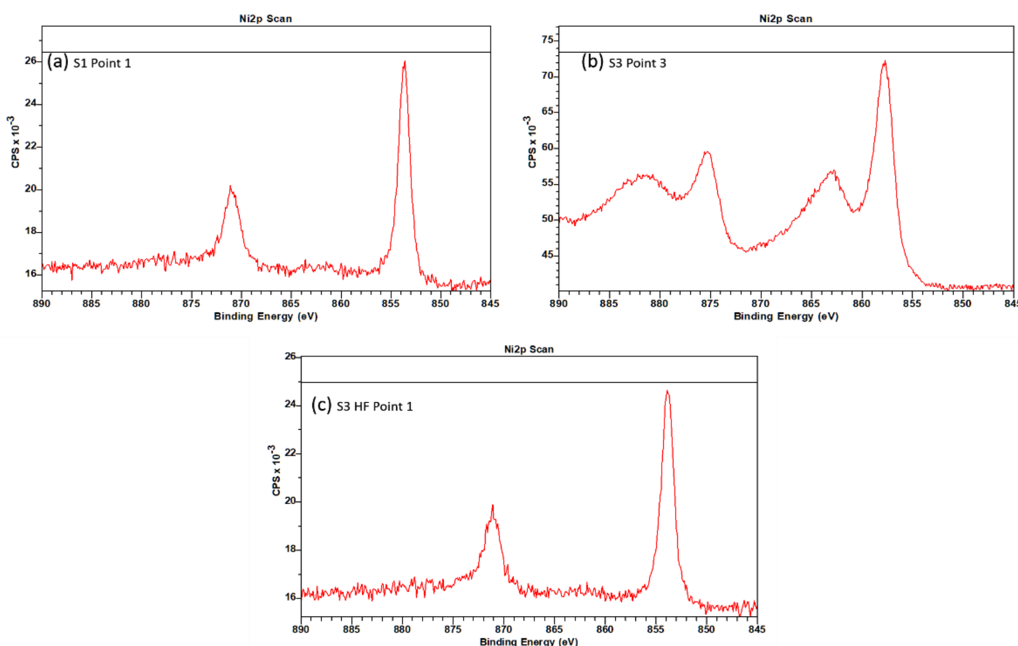



Figure 25: Ni2p Scans from HR XPS in line with points from Figure 24

Nickel oxide states are present in figure 25 (a, b, c), whereas, figure 25b has satellite states of nickel as well. Also, from literature [40], figure 25b which is S3 without HF treatment and had nickel since the beginning, it seems to possess, $Ni_2O_3 2p_{3/2}$ and $NiO_2 p_{1/2}$ states towards higher binding energies along with $Ni_2O_3 2p_{1/2}$ and $Ni_2 p_{1/2}$ towards lower binding energies respectively. But a loss in oxide states have been observed after HF etching and heat treatments under UHV.

Data Obtained for Sample1 point 1 from HR XPS:

| Name | Peak BE | FWHM eV | Area (P) CPS.eV | Atomic % |
|---|---|---|---|---|
| Ni2p3 | 854.83 | 2.51 | 89927.82 | 0.51 |
| O1s | 533.13 | 2.78 | 550886.16 | 11.38 |
| C1s | 286.08 | 2.72 | 361626.92 | 18.06 |
| Si2p | 100.25 | 1.55 | 1411148.86 | 70.05 |

Data Obtained for Sample3 point 1 HF from HR XPS:

| Name | Peak BE | FWHM eV | Area (P) CPS.eV | Atomic % |
|---|---|---|---|---|
| Si2p | 99.42 | 1.05 | 200017.21 | 76.41 |
| C1s | 285.08 | 1.53 | 33849.88 | 13.01 |
| O1s | 532.13 | 1.75 | 63291.48 | 10.06 |
| Ni2p3 | 853.83 | 1.43 | 12010.68 | 0.53 |

Showing almost equal atomic % of nickel for both samples, S1 and HF-treated S3. Overall, the combined sample treatments and XPS observations deliver a coherent picture of how UHV thermal treatments modify both the chemical structure of silicon surfaces and the distribution of nickel impurities. Conducted studies provide a solid experimental foundation for understanding ways of contamination in Si processing as well as for selecting appropriate precleaning/annealing strategies in future work to attain desirable electrical performance across semiconductor devices.

## Conclusion

The thesis aimed to highlight the importance of nickel and silicon interaction and how it can have a huge impact on technological advancement by overcoming electrical performance issues in semiconductor devices. Key resultant products of Ni-Si interactions are nickel silicides that can enhance electrical characteristics of semiconductors if properly engineered at a correct place of device materials. High-performance Ni-Si contacts are one of the examples how studying and controlling the interaction can be beneficial because they hold good conductivity, low contact resistivity, and favourable Schottky barriers. Unintentional Nickel contamination on the other hand can reduce electrical characteristics of Si material by creating deep level traps within Silicon bandgap, decrease charge carrier recombination time, encourage non-radiative recombination, and can elevate leakage current especially on grain boundaries during reverse-biased operation. The effects can have negative impact on overall performance of solar cells, ICs, and MEMS devices where transfer of minority charge carriers defines performance. Conducted study highlights importance of strict contamination control throughout wafer fabrication including cutting and sample handling.

Novel characterization techniques can facilitate better monitoring during Si wafer handling on atomic level to reduce overall contamination. XPS is one of the effective methods that can detect Ni and other common metal contaminations while also giving information about information about chemical state for oxides and silicides.

In our studies, we have heated different silicon substrates at 600 °C (30mins, for gassing out), 800 °C (30mins), 900 °C (30mins), 1000 °C (5mins/20mins), and 1200 °C (5 seconds) at ultra-high vacuum settings. And analysed samples without exposing to air in same UHV settings. It is concluded that there are high chances of the presence of Ni contamination during Si wafer processing and handling because one of the samples S3, had nickel signal before any treatment, and after heat treatment, 0.53% atomic percentage was found in the sample. Also, around 800°C native oxide layer evaporates, and above this temperature, a small percentage of Ni contamination begins to appear in XPS which can be detrimental to device’s performance. Also, sample treated with hydrofluoric acid removed oxide layer and showed a little decrease in Ni contamination as compared to sample 1. The insights provided here can contribute to improved manufacturing practices and higher reliability in Ni-Si electronic technologies.

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# Appendices

## Use of AI programs/tools

No AI tools have been used to create thesis content including figures, results, and thesis body