UNIVERSITY OF TURKU

Memristive devices for neuromorphic computing: from materials to switching mechanisms

Department of Mechanical and Materials Engineering

Bachelor's thesis

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12.5.2026
Turku

Bachelor's thesis

Subject: Materials engineering

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Title: Memristive devices for neuromorphic computing: from materials to switching mechanisms

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Number of pages: 24 pages

Date: 12.5.2026

Traditional von Neumann architecture has brought computing to its current levels of performance. However, the data transfer efficiency between memory and CPU is failing to keep up with the increasing data sizes and requirements of Artificial Intelligence (AI). This well-established challenge has launched the development of new architectures to manufacture computing systems aiming to eliminate the data transfer between two separate units. One of these emerging technologies is neuromorphic computing.

Neuromorphic computing aims to mimic the functional principles of biological brain. This is done by building arrays of synaptic devices that are capable of parallel computing, similarly to connected synapses function in biological brain. Neuromorphic computing systems are complex ensembles with aspects such as algorithms, learning rules and circuit architecture.

This thesis will review different memristive devices as possible candidates for synaptic devices in neuromorphic computing. Memristive devices that are examined are phase-change memory, ferroelectric devices, electrochemical metallization cells, valence change memory and nanowire-based devices. Additionally, 2D and organic materials will be discussed for their possible future implementation in such applications.

A memristive device aims to function as a single unit that combines memory and CPU in one component. This eliminates the need to transfer data between two separate components allowing for in-memory computing. Precisely this functionality makes neuromorphic computing efficient for large data manipulation and AI applications.

Also, in this thesis the operating principle of each memristive device will be explored. Moreover, their advantages and issues as synaptic devices will be presented. After reviewing the memristive devices, the possible strengths of 2D and organic materials for device fabrication and unique applications will be discussed. The thesis concludes with an individual overview of the status of both neuromorphic computing and memristive devices.

Keywords: neuromorphic computing, memristive device, in-memory computing, switching mechanism, artificial intelligence

Kandidaatintutkielma

Koulutusohjelma, oppiaine: Materiaalitekniikka

Tekijä(t): Otto Jääskeläinen

Otsikko: Memristive devices for neuromorphic computing: from materials to switching mechanisms

Ohjaaja(t): Tohtori Konstantinos Konstantinou

Sivumäärä: 24 sivua

Päivämäärä: 12.5.2026

Perinteinen von Neumann-arkkitehtuuri on tuonut tietokoneiden tehokkuuden nykyiselle tasolleen. Kuitenkin tiedon siirtäminen muistin ja prosessorin välillä ei kykene vastamaan kasvan tiedon määrään ja tekoälyn (AI) tarpeita. Tämä ongelma on herättänyt kiinnostusta uusien tietokonearkkitehtuurien kehittämiseksi, joiden avulla tiedon siirtäminen kahden erillisen yksikön välillä voidaan välttää. Yksi näistä uusista arkkitehtuureista on neuromorfinen laskenta.

Neuromorfinen laskenta pyrkii toimintaperiaatteellaan jäljittelemään biologisten aivojen toimintaa. Tämä pyritään toteuttamaan kokoamalla rivistöjä synapsisia laitteita, jotka kykenevät toimimaan samanaikaisesti, matkien biologisten aivojen rinnakkaista toiminnallisuutta ja monimutkaisia kytköksiä keskenään. Neuromorfiset systeemit ovat vaativia kokonaisuuksia, jotka koostuvat esimerkiksi algoritmeista, oppimissäännöistä ja virtapiiriarkkitehtuurista.

Tutkielmassa arvioidaan erilaisia memristoreja mahdollisina ratkaisuina synapsisten laitteiden toteuttamiseksi neuromorfisissa systeemeissä. Arvioitavat memristorit ovat faasimuutos muisti, ferrosähköiset laitteet, sähkökemialliset metallisointikennot, valenssimuutosmuisti sekä nanolanka-pohjaiset laitteet. Laitteiden lisäksi tutkielma esittelee orgaanisten ja 2D-materiaalien mahdolliset hyödyt arvioitavien laitteiden rakentamisessa.

Memristori on laite, joka pyrkii yhdistämään muistin ja prosessorin yhdeksi komponentiksi. Tämän ansiosta tietoa ei tarvitse siirtää kahden komponentin välillä, mahdollistaen toiminnallisuuden laskennallisena muistina. Tästä syystä neuromorfinen laskenta voisi tarjota tehokkaan ratkaisun suuria tietomääriä käsitteleviin sovelluksiin ja tekoälyn hyödyntämiseen.

Tutkielmassa esitellään käsiteltävien memristorien toimintaperiaatteet. Lisäksi eri laitteiden potentiaalia osana neuromorfista laskentaa arvioidaan vertailemalla etuja ja tämänhetkisiä haasteita. Laitteiden vertailun jälkeen esitellään orgaanisten ja 2D-materiaalien hyödyt laitteiden valmistuksessa, sekä niiden mahdolliset uniikit sovellukset materiaali kohtaisesti. Tutkielman lopussa tehdään yhteenveto neuromorfisen laskennan sekä memristorien nykytilanteesta.

Avainsanat: neuromorfinen laskenta, memristori, laskennallinen muisti, tekoäly, resistanssin muutosmekanismit

Abbreviations

PCM = Phase-change memory

FeFET = Ferroelectric field effect transistor

FTJ = Ferroelectric tunnelling junction

ECM = Electrochemical metallization cells

VCM = Valence change memory

NW = Nanowire

LRS = Low-resistance state

HRS = High-resistance state

CMOS = Complementary metal-oxide semiconductor

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1 Introduction

Computers have become a vital part of our modern-day society. Modern computation uses the well-established von Neumann architecture. In von Neumann architecture processing and memory are two separate units that transfer data between each other continuously.[1] The growing interest in artificial intelligence (AI) development and the continuous increase in data volume are causing computing to become more data-centric posing challenges to this architecture, resulting in the so called von Neumann bottleneck [2]. Consequently, due to this fact most of the consumed energy is used not in the actual computation but in transferring data between the processing and memory units [3]. In addition, modern hardware typically utilizes dynamic random-access memory (DRAM) to store data. DRAM requires periodic refreshing and in these devices the processor has to run even while waiting for the receipt of the data causing additional energy consumption [4].

It is becoming apparent that in order to keep the computing hardware competitive with the increasing data volume it is mandatory to develop architectures where memory and processing are more intertwined [3]. One of the emerging technologies to overcome the von Neumann bottleneck is neuromorphic computing. Neuromorphic computing refers to a computing system that takes inspiration from the neuro-biological architecture of the brain [1]. By mimicking the human brain operation, neuromorphic computing systems function through utilizing artificial synapses and neurons, as illustrated in figure 1 [5].

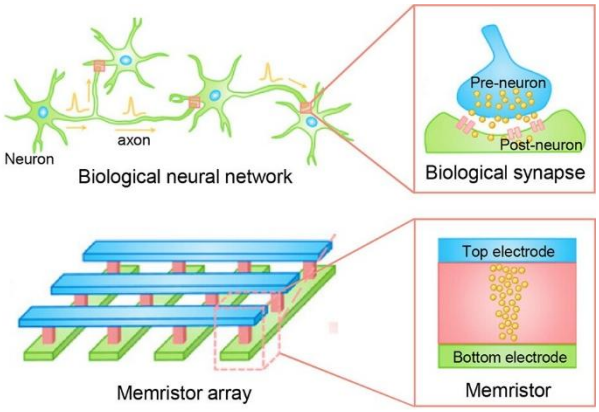

Figure 1 Memristive device as synapse. Image reproduced with permission from [6]. Copyright 2025 American Chemical Society

1.1 Neuromorphic computing system

A neuromorphic computing system typically consists of the synaptic device, the neuronal circuit and a neuromorphic architecture. These systems incorporate memristive devices as the synaptic device eliminating the data transfer between memory and computational units.[7] Memristive devices store information based on resistance or conductance values that can be modified through different mechanisms [3,8]. These values in neuromorphic systems are called synaptic weights [9].

The most appealing properties of the memristive devices are the ability to perform in-memory computing and the potential to function as non-volatile memory [1]. Non-volatile memory operations are enabled by the different mechanisms that alter the states used in memristive devices. These states are referred as memory states, and because they are non-volatile, they remain active without power supply [9]. The availability of more memory states can allow for multi-level (muti-bit) storage in the devices [8]. Enabling factors for in-memory computing (IMC) are the different switching dynamics and analogue tunability used in memristive devices [1].

1.2 Memristive devices

The memristive devices can be divided in two categories depending on their structure and number of terminals, as shown in figure 2. In the two-terminal memristive devices the top electrode (TE) and bottom electrode (BE) mimic the functionality of pre- and post-synaptic neurons, with the corresponding electrical signal between them mirroring the neuronal communication [10]. In the two-terminal devices the synaptic weights are updated by altering the resistive state of the material between the BE and TE.

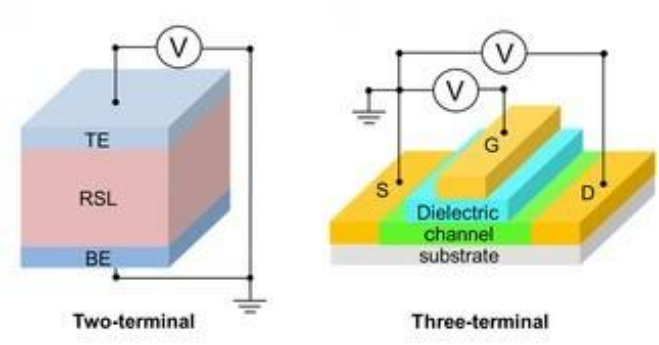

Figure 2 Two-terminal and three-terminal memristive devices. Modified from Xiao et al [9]. Copyright 2024 Xiao, published by Science Parter Journals

Three-terminal memristive devices consist of three electrodes, called drain, source and gate, a dielectric layer and a channel layer. The gate electrode is used to change the state of the dielectric layer, using suitable voltage pulses. Modifying the state of the dielectric layer directly affects the resistance state of the channel layer. The controlled change of the resistive states can be utilized to store information that can be written and read using the source and drain electrodes. [11]

This work prioritizes discussing relevant materials and architectures used as memristive devices in neuromorphic computing applications. From the device perspective phase-change memory, ferroelectric memory, electrochemical metallization cells, valence change memory and nanowire-based devices will be reviewed. 2D and organic materials will be discussed in separate sections because of their relevance and large range of possible applications for memristive devices.

2 Phase-change memory devices

Phase-change memory (PCM) is one of the most mature technologies considered as a possible way of realizing the memristive devices in neuromorphic computing. Phase-change materials have been used as optical memory devices in several applications such as CDs, DVDs and Blue-Ray disks [3]. Therefore, PCM is one of the most widely accepted promising technologies for neuromorphic computing purposes [12]. Over the years, extensive research in the development of PCM devices has been conducted because of their many appealing advantages such as fast read/write operations, non-volatility, long cycle life, small component size, low power consumption, radiation resistance and good scalability [13].

PCM utilizes materials that can be heated to reversibly change between an amorphous and a crystalline state and thus altering the resistance of the material. In the amorphous state no long-range order is present, covalent bonds are dominant, and the electrons are strongly localized causing higher resistance in the material. In contrast, in the crystalline phase resonant bonds are formed between the atoms and the electrons are highly delocalized, leading to lower resistance in the material. Switching between amorphous and crystalline states also affect the refractive index of the material, allowing PCM to be used as rewritable optical data storage in photonic phase-change applications. [14]

Typically, a reversible phase-change material is placed between two metal electrodes that are heated by applying electricity to them. Most used materials for PCM applications are compounds of chalcogenides, usually consisting of Ge, Sb and Te. [1] Heating is provided using different current pulses, an approach that is known as Joule heating [9]. Pulses that are used to change the material between amorphous and crystalline phases are called SET and RESET pulses, as shown in figure 3. After Joule heating the current state is interpreted as data measuring the resistance or refractive index of the phase-change material. [8,13,15]

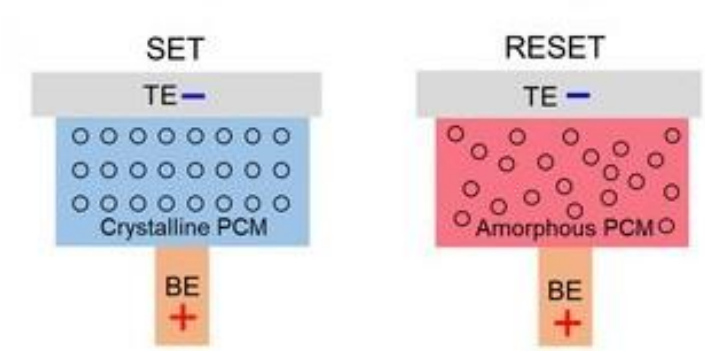

Figure 3 Crystalline (SET) and amorphous (RESET) states of PCM. Modified from Xiao et al [9]. Copyright 2024 Xiao, published by Science Parter Journals

The SET process transforms the material from an amorphous state to a crystalline state with a longer acting moderate intensity pulse [13]. The applied voltage causes the material to be heated to a temperature between the crystallization temperature (T_C) and melting temperature (T_M). The following RESET operation rapidly heats the material, with a shorter pulse of higher intensity, above the melting point and subsequently cooling it, resulting in the formation of the amorphous structure (melt-quench process). [16]

A key property of PCM is the ability to reversibly switch between two resistive states in a non-volatile fashion, generating the potential to function as binary storage unit. Since the high-resistance state (HRS) and low-resistance state (LRS) can be interpreted as binary states 0 and 1, this property allows for easy integration to the present logical operations used in computing. This could enable connecting PCM devices with the currently used complementary metal-oxide semiconductor (CMOS) technology. [1,3]

In addition, PCM can achieve a continuum of different resistance or conductance values between these two low-resistance and high-resistance states making it possible to run matrix-vector multiplications (MVM) in $O(1)$ time complexity [1]. This can be accomplished by applying partial RESET pulses to create partial states between the amorphous and crystalline states [3]. The MVMs are traditionally computationally expensive tasks in AI applications and they are used for example in pattern recognition [14]. In addition, MVMs are used to train deep neural networks (DNN) [7]. The possibility of running these tasks with in-memory computing would impact the future AI efficiency.

Another feature of PCM appealing for neuromorphic computing applications is the crystallization kinetics inside the memory device. It has been observed that it is possible to progressively reduce the device resistance by the successive applications of SET pulses of the same amplitude. This approach can be used to implement synaptic weight updates in an effective way, making the learning process of DNNs more efficient. [1,3]

Meanwhile, despite PCM devices are one of the most advanced technologies utilized for applications related to neuromorphic computing, there are still certain issues that need to be resolved before being plausible for wider usage. PCM devices can be scaled down to nanoscale dimensions, but there are challenges with connecting them in larger arrays relating to etch damage and depositing the materials in high-aspect ratio pores [1]. Additionally, further research on the material side is needed to improve reliability, long-term stability, switching speed and RESET current [15]. Another issue is the stochastic process associated with crystal growth during the recrystallization of the material inside the device, which is a key challenge in accumulative behaviour applications used for training neural networks [3].

3 Ferroelectric memory devices

Ferroelectricity was discovered originally in 1920. It refers to the ability of non-centrosymmetric crystalline materials to exhibit multiple permanent electric polarization states. These states can be reversibly switched by applying an electric field, known as coercive electric field (E_C). This property has led to the development of several different devices using ferromagnetic properties as a data-storage concept. [1,17]

The first application for ferroelectric materials in computing was the ferroelectric capacitor (FeCAP) based memories (FeRAM) proposed in 1950s. However, these did not become commercially available before 1990s. Even though FeRAM has reached commercial stage it will not be discussed in this work, because it suffers from destructive read operation and scalability issues, making it a poor choice for neuromorphic systems. Another ferroelectric memory device that was developed in the 1950s was the ferroelectric field effect transistor (FeFET). The ferroelectric tunnelling junction (FTJ) was first demonstrated in 2009. Despite these devices have not found commercial success yet, the ferromagnetic memory devices are considered to be promising candidates for neuromorphic applications. [1,17,18]

The discovery of ferroelectricity in Si-doped HfO_2 marked a great leap in the ferroelectric based memory devices, since it is a well-established material in CMOS technology [18]. Typical ferroelectric materials are various perovskite oxides such as $BaTiO_3$, $BiFeO_3$, and $Pb(Zr,Ti)O_3$ [10]. Ferroelectricity has also been observed in various organic materials and 2D materials [17].

3.1 Ferroelectric field effect transistors

The structure of FeFET is a three-terminal memristive device similar to the structure of a MOSFET transistor, but in FeFET the gate dielectric layer is replaced with a ferromagnetic layer [17]. In FeFETs, the non-volatile memory operation relies on the presence of two stable polarization configurations of ferroelectric domains in the layer (“up” and “down”), which can be switched by applying sufficiently large positive or negative gate voltages, called coercive voltage (V_C) [12].The polarization state of the ferroelectric layer directly affects the threshold voltage (V_T) [18]. The V_T can reach

respective low-voltage and high-voltage states that can be used to store binary information, and the threshold between the two states is called memory window [12]. Applying a positive gate voltage reduces the V_T and it is referred as program state, while applying a negative voltage increases the V_T and it is referred as erase state [18]. The V_T can be read non-destructively, similarly to flash memory, using voltages below V_C [17].

FeFET applications are appealing for neuromorphic computing due to their ability to store large number of different V_T values. This is possible by partially switching the polarization states in the ferroelectric layer of the gate stack. This allows FeFETs to store multiple different values of synaptic weights and act as an analogue memory. Because these states can be achieved by exploiting gradual switching of polarization, it allows gradual updating of synaptic values. This is a clear advantage compared to PCM devices, for instance, that suffer from the stochasticity associated with crystal growth. [10,12]

Another aspect that has made FeFETs interesting candidates for neuromorphic computing applications is the fact that they have similar structure with the existing transistor technology that is well established. This has allowed for modifications in the structure to meet occurring challenges in the devices. For example, by adding a metal layer between the ferroelectric and insulator layers the architecture of the gate has been modified accordingly to better accommodate multiple ferroelectric domains. [10,18]

Other advantages in FeFETs are their three-terminal structure (drain, gate and source) and the compatibility with CMOS technology since the discovery of ferroelectricity in HfO_2. The three-terminal structure offers a greater resistance to sneak path current and IR drop, hence providing more accurate MVM operations. HfO_2 is already well established to be CMOS compatible and HfO_2 based FeFETs have demonstrated fast switching, good data retention and low operating voltages. [1,12,18]

One of the key limitations in FeFETs is the scalability of the devices. It has been observed that the ferroelectric properties are suppressed or vanish when the size of the device is decreased to certain nanometer scales [10]. Other limitations in FeFETs are processes related to charge trapping at the interfaces, weak charge compensation by

the semiconductor channel and gate leakage. These issues can cause drift in the V_T and destruction of the memory state. [10,17]

3.2 Ferroelectric tunnel junctions

An FTJ is a two-terminal device that has a “sandwich” structure consisting of two metal or semiconductor electrodes and a very thin ferroelectric film [17]. FTJs can reversibly change their resistance by polarization switching of the domains in the ferroelectric layer, which is achieved by applying an electric field exceeding the E_C [12]. This process is visualized in the schematic shown in figure 4. In FTJs the current transportation utilizes quantum tunnelling and the polarization direction of the ferroelectric layer [18]. The polarization direction controls the charge distribution at the electrode and the ferroelectric interface, while altering the charge in the interface changes both the width and the height of the tunnelling barrier. When the polarization is directed towards the TE, the tunnelling barrier becomes wider. This leads to a lower tunnelling probability resulting in HRS. In contrast, when the polarization is directed towards the BE, the tunnelling barrier becomes thinner, increasing the corresponding probability and leading to LRS. The ratio between LRS and HRS is called tunnelling electro-resistance ratio (TER). A large value of TER lowers errors and power consumption during read and write operations. [12,17,18]

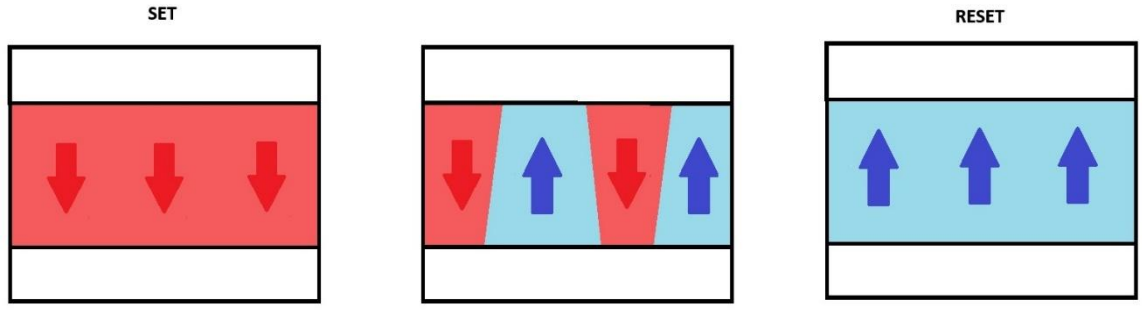

Figure 4 Transition from LRS to HRS in an FTJ device. Figure by Otto Jääskeläinen

Similar to FeFETs an FTJ can achieve multiple different polarization states, enabling analogue and accumulative learning applications for neural network training [12]. The

partial switching in the ferroelectric domain can be precisely controlled making the FTJ technology promising for neuromorphic computing devices [17].

FTJs have gathered rapid interest in the current state of neuromorphic system development because of their compatibility with the existing computing technology. FTJs can be made to be fully CMOS compatible, and their two-terminal structure makes them an ideal contender for crossbar array architectures that can be used to realize artificial neural networks (ANN) [18]. Experimental results mimicking biological brain functions using FTJs have been recently reported in the literature [17].

The switching of polarization states in ferroelectric devices corresponds to a more energy efficient resistive switching process compared to other device operations, such as valence change or phase change memories. In FTJs the switching happens in a nanosecond range, allowing almost simultaneous parallel computing in ANNs [12].

Most of the limiting factors associated with FTJs are related to the read operation of the device. The low read current values of FTJs are in the same range as the junction leakage currents of the connected CMOS transistors, leading to possible issues in reliability. Additionally, to implement analogue and accumulative switching the polarization state should be measured before every programming operation, unless using identical voltages in the system. This causes latency and makes the circuitry more complex. [12] Other limitations stem from the fabrication of very thin ferroelectric layers that currently suffer from unintentional dead interfacial layers between the electrodes. These dead layers are thin spaces at the interface of the ferroelectric material with the electrode that have lost their ferroelectric properties, leading to leakage currents. [1]

4 Electrochemical metallization cells

Electrochemical metallization memory (ECM) is a resistive-switching random-access memory (ReRAM) that is based on a form of ionic movement, and it has been viewed as a promising new technology for the future of memory devices [19]. ECM devices have been under development for the past 20 years, but they are still yet to reach their full potential [1].

ECMs are two-terminal devices that consist of an electrochemically active metal electrode, a solid-state electrolyte and an inert metal electrode [9]. Internal or applied voltage is used to trigger an electrochemical reaction resulting in metallic ions to move from the active electrode to the inert electrode [1,19]. The movement of the metal ions gradually forms a conductive filament (CF) between the electrodes, causing them to connect and create a short circuit leading to LRS. This is referred to as the SET operation of the device, as shown in figure 5. The RESET operation is implemented by applying voltage of opposite polarity causing the CF bridge to break down, and thus returning the device to HRS. [1,9,19]

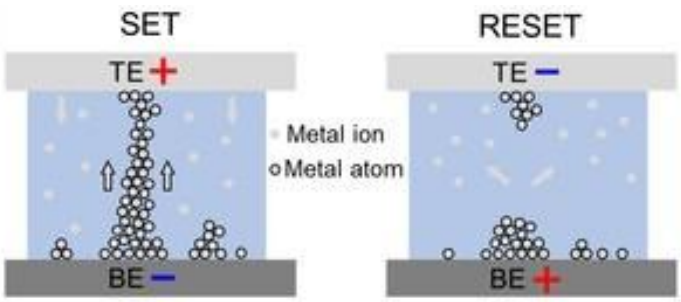

Figure 5 SET (conductive filament is formed) and RESET (conductive filament is dissolved) states of ECM. Modified from Xiao et al [9]. Copyright 2024 Xiao, published by Science Parter Journals

The active electrode is typically made of Ag, Cu, Ni or Fe, while the inert electrode usually consists of W, Au, Pt, TiN or Pd [1,19]. The resistive switching area is based on a chalcogenide solid-state electrolyte, with compounds such as GeS and GeSe to have shown promising performance for practical applications [20]. Recently, halide perovskites have gained much interest as the material employed in the switching layer [21].

While the HRS and LRS provide a clear functionality for binary storage, ECM can also exhibit analogue behaviour. The formed CF can have a varying thickness, while it can act as a complete bridge or be partially dissolved within the electrolyte, offering varying resistance states. [1]

Another appealing property of ECM is that it can be implemented in various environments and systems. This is possible due to ECM being stable against radiation, high-energy particles and electromagnetic waves, while also being operatable in high-temperature regimes. Also, the variety of the available solid-state electrolyte materials offer possibilities for different device fabrication levels. [1]

Moreover, it has been noticed that ECM devices have lower power consumption for synaptic operations than biological synapses [1]. While this has been observed in other types of ReRAMs, the operating voltage for ECMs is lower than in any other redox-based devices, for example valence change memories, making it superior to other candidate technologies [1].

Most of the limitations of ECMs are associated with the operating conditions in the device. Small device volume and non-equilibrium states cause challenges in understanding and controlling the processes inside the devices [1]. Also, there are challenges to sustain the reached resistive state after switching off the applied electric field, making analogue memory operations unstable [21]. The fabrication of ECM devices also suffers heavily from even the smallest of impurities affecting the electrical properties of the device [1].

5 Valence change memory

Valence change memory (VCM) devices have demonstrated fast operation speed, great scalability and low operating power making them plausible options for future memory devices [19]. Three different types of VCM devices exist, namely: filamentary VCM, interfacial VCM and three-terminal VCM redox transistors. It is noted that the three-terminal VCM and interfacial VCM are both still in their infancy and they will not be discussed in as much detail as the filamentary VCM. [1]

In many ways, VCM and ECM share several similarities. VCM devices utilize oxygen ion migration comparable to the metal ion movement of the ECM. There are two ways to implement two-terminal VCM devices. The first and more advanced method is filamentary VCMs, in which there are two electrodes and an electrolyte placed between them, with typical electrolyte materials being binary oxides. Another notable aspect is that usually the bottom or top electrode is reactive and will be oxidized, in turn reducing the oxide electrolyte. In filamentary VCMs an external electric field is created by applying appropriate voltage pulses. This applied electric field causes oxygen vacancies to form a CF between the two electrodes. [19,20,22]

The SET process refers to the operation that oxygen vacancies forming the CF when voltage is applied in the device. When the CF is formed in the oxide electrolyte part, the VCM device is in LRS. The RESET process takes place when the CF is ruptured using voltage of reversed polarity leading to the HRS, as seen in figure 6. [22] While most VCM devices use opposite voltages for the SET and RESET processes, there are certain conditions that unipolar operation voltages can be used. This is usually linked to the filament rupture due to Joule heating [22]. In such applications both electrodes of the device are inert [20].

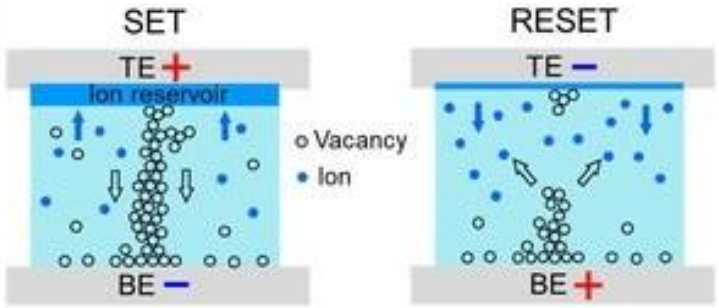

Figure 6 SET (conductive filament is formed) and RESET (conductive filament is dissolved) states of VCM. Modified from Xiao et al [9]. Copyright 2024 Xiao, published by Science Parter Journals

Metal oxides such as TiO_2, NiO, HfO_2, Ta_2O_5 and ZrO_2 have been considered as the electrolyte component in VCM applications [19]. The most studied systems are based on HfO_x and TaO_x [20].

In interfacial VCM devices, there is no formation of CF between the electrodes. Instead, the change in resistive state is based on the homogeneous movement of oxygen ions in the electrolyte [1]. This approach can be exploited in complex oxides where the oxygen atoms are weakly bound [20]. In the three-terminal VCM devices the mechanism is related to the control of the oxygen vacancy concentration in the bulk of the transistor channel [1].

An appealing reason for VCM devices to be considered for neuromorphic systems stems from the fact that successful prototypes of HfO_x and TaO_x based VCM neuromorphic chips have been demonstrated [1]. Combined with their full compatibility with existing CMOS technology VCM corresponds to a compelling candidate for further development [22]. Even though the current VCM devices exhibit challenges for large array integration, it is believed that most of these issues could be mitigated or resolved with advances in the circuit level [1].

In addition, VCM devices have shown a high endurance up to billions of switching cycles, that is higher than any other resistive switching operating device [21,22]. Furthermore, it has been noticed that VCM devices exhibit high dynamic range and low switching energy [22].

Nevertheless, while the first prototype neuromorphic chips have been already developed, they do not yet support on-chip learning [1]. Another challenge is associated with the implementation of analogue memory functionality, common in both filamentary-based devices, and it is caused by the unstable nature of the filament in non-volatile conditions. [20] The further development of interfacial and three-terminal VCM devices could offer solutions to the analogue behaviour challenges [1].

Moreover, for the realization of larger neuromorphic systems the resistance of filamentary VCM devices is too low. Program and read disturbs are also a problem that currently hinders their further integration for neuromorphic applications. These disturbs are caused by the unstable nature of the filament leading the low power read operations to possibly alter the state of the filament. In an array system these disturbs could also be caused by unintentional sneak currents in the system. [1,20]

6 Nanowire-based devices

While the crossbar arrays of memristive devices are the most researched architecture to realize artificial neural networks, they have challenges meeting the complexity of connections in the biological brain. Memristive nanowire (NW) networks have been proposed to implement a more biologically-inspired structure with complex connections [1]. NW-based devices have gained attention because of their high-speed computing characteristics, low-power consumption and high surface-to-volume ratio. [23,24]

NW-based neuromorphic devices can be constructed with a single NW, and various architectures of connected NWs such as two crossed NWs, regulated arrays and complex networks. Apart from different NW architectures, different types of devices are also available ranging from two-terminal devices to more complex three-terminal devices. NWs are commonly made of a core wrapped in an insulating shell layer. In NW networks the change of resistive state occurs at the interfaces of the connected NWs. The most standard method of resistive switching in NW networks is the same as in ECM, but in an NW network the CF forms between the NWs instead of the electrodes. Nevertheless, the formation of CF is possible even in a single NW making the fabrication of single NW devices feasible. [1,23] There also exists other mechanisms for NWs to function as a memristive device, such as vacancy migration and charge trapping [23].

NW-based memristive devices can be fabricated from a large variety of different materials, such as active metals, metal oxides, perovskites, semiconductor materials or organic materials. The material of choice dictates the mechanism used to alter the resistive state of the NW. [23]

For active metal core NWs, the most comprehensively studied material is Ag. This is due to the high conductivity and good bending resistance of the Ag-based NWs. Even with Ag as the core material, it is possible to fabricate devices with different characteristics by modifying the insulating shell material and the electrode material. Because the CF is formed by the core over the shell layer, the material of the shell layer can affect the formation of the CF. [23]

Metal-oxide NWs do not have an insulating layer. In metal oxide-based NWs there are different mechanisms to realize memristive behaviour. One approach consists of building an ECM unit where the electrolyte is replaced by a ZnO NW. Then by applying suitable voltages it is possible to cause the nanowire to connect or disconnect. The formed and broken NW can be thought of as CFs directly altering the resistive state of the device. Metal-oxide NWs can also utilize ion and vacancy migration to modify their synaptic weights. In such scenario, ions or atom vacancies travel from one electrode towards the other electrode changing the electrical properties of the NW. Vacancy migration is the mechanism used in WO_3 and TiO_x-based devices. Ion and vacancy migration is also the switching mechanism used in perovskite NW devices.[23]

Semiconductor NWs are typically constructed with a network architecture, and the most used switching mechanism is charge trapping, in which the charge carriers are gathered (or “trapped”) at the junction of the NWs causing changes in the conductive state. The most used material for semiconductor NWs is Si. [23,24]

Organic NW devices can be fabricated from single NW or based on a network architecture. Single NW devices can utilize NW-confined filament growth that is caused by Ag electrode atoms moving across the NW [25]. Alternatively, organic NWs have been constructed from protein NW networks or single P_3HT core wrapped in poly(ethylene oxide) (PEO). The core and shell structure was used to fabricate a three-terminal device where the NW was submerged in ionic gel. The P_3HT core functions as conductive channel, and by applying external pulses the negative ions from ionic gel penetrate the shell. This can be reversed using opposite polarity pulses. These pulses can be used to accumulate negative ions toward or away from the conductive channel causing the resistive state to change. [23]

The most appealing aspect of the NW-based memristive devices is the large array of different brain-like learning methods that can be implemented using different materials and compositions. The potential tunability and structural flexibility of NW devices could allow for a wide range of possible applications. NW devices also offer superior scalability compared to many other memristive devices due to their 1D structure. [23]

However, there are still many issues that need to be addressed before NW-based devices can compete with other memristive devices. Certain NW materials have a problem in retaining memristive properties over long periods of time that is caused by their sensitivity to the external environment, which is further enhanced by the high surface-to-volume ratio of the devices. [23] In addition, there are challenges in understanding the behaviour related to different network topologies and the mechanisms at the individual NW-NW junction level [1,23].

7 2D materials for memory devices

Traditional CMOS technology has been the foundation of electronics and for random-access memory devices. This technology is reaching its limits in the present several nanometer scale, where quantum effects start to affect the current transportation. Since the discovery of graphene in 2004, the first ever two-dimensional (2D) material, the research in various 2D materials has expanded rapidly [5]. Today there is a large amount of 2D materials with different properties, ranging from insulators and semiconductors to ferroelectric and phase-change materials [6]. The research for employing such materials for memristive applications has increased due to their appealing physical properties, such as chemical inertness, good thermal stability and atomically thin geometry, as well as their excellent electronic properties [1].

Alongside the aforementioned properties, the 2D materials also offer different doping possibilities to generate structures with different properties. Moreover, 2D materials can also be stacked on top of each in order to create different van der Waals (vdW) heterostructures.[5] The vdW heterostructures are especially intriguing due the fact that they do not only retain the properties of the individual materials that are made of, but also they exhibit additional interesting functionalities. These new properties can be tailored using not only different materials but also different stacking orders.[1]

2D materials can be prepared with multiple different methods. While it is possible to synthesize 2D materials of high-quality and purity using mechanical exfoliation, the experimental challenges are currently related to time consumption and scalability of the manufacturing processes. Alternatively, certain chemical methods could offer larger production yield, but these methods cannot result in high quality materials. [5]

As mentioned above, a large range of 2D materials with different properties are available. 2D materials have gathered a lot of interest for memristive device fabrication due to their good scalability, while they can be used to fabricate devices based on many different mechanisms. 2D materials can exhibit all resistive switching mechanisms discussed in this work, and in some cases can offer advantages over traditional bulk materials. For example, in PCM devices the phase change in traditional chalcogenide compounds can cause accumulation of waste heat, but in 2D materials the waste heat

will not increase due to their anisotropic electrical properties and large interlayer space.[5]

While 2D materials provide many desired properties, they still need to progress before they can be further utilized in memristive device fabrication. The key challenge is related to complications for large-area synthesis of high-quality 2D materials [1]. Further challenges that need to be addressed are the high-power consumption and the stability of the devices. It is worth mentioning that some of the issues related to stability and data retention might be potentially resolved via device engineering instead of material level properties.[5]

8 Organic materials for memory devices

Organic semiconductors (OSCs) have been regarded as a promising material solution for memristive devices. This is mainly due to the tunability of their properties making them adaptable for a range of applications. [1] OSCs can be utilized to fabricate two-terminal and three-terminal devices with different resistive switching mechanisms. In principle, organic materials feature low-cost, CMOS compatibility and low energy consumption.[26]

OSCs can be classified either as p-type or n-type semiconductors. In p-types electron holes function as the current carriers, whereas in n-types this is done by electrons. N-type organic materials are heavily limited by the fact that they rapidly deteriorate under ambient conditions and have difficulties in accepting electrons from the conventional electrode materials used in these devices. These limitations in n-type organic materials have led to the use of p-type OSCs in most device architectures. In particular, a combination of two distinct polymers known as PEDOT: PSS is one of the most promising organic p-type material for memristive devices. However, in future, a combination of both n- and p-types could be used to achieve further complex synaptic functionalities. [26]

OSCs can be customized electrically, mechanically and chemically depending on the application [25]. Such tailoring of properties can be utilized to influence the performance of the device. Through chemical modification it is possible to fine-tune the operation speeds, energy levels and electronic conductivity. [1] Organic compounds typically offer a wide range of material and resistive states allowing analogue memory functionality [25].

The biocompatibility and their flexible mechanical properties have made organic-based devices interesting for possible connections between biological and neuromorphic systems. In these applications, they could form direct interfaces with tissue and could be used to create adaptive prosthetics, for example. [1] However, these fully organic neuromorphic systems are still heavily under development, and it is more likely that OSCs materials will be implemented with inorganic CMOS-technology before all-organic devices can be realized [25].

Organic materials show a considerable promise for neuromorphic systems, but there are still some issues that need to be solved. Organic materials are typically programmed at such low currents that the read and write currents are of similar amplitude. This can lead to the read operation causing changes in the memory state resulting in reliability issues. [25] Another evident problem at the system level is the integration of organic-based devices with inorganic systems. The electronic properties of OSCs degrade at elevated temperatures, that are far lower than those used in annealing circuits, which causes concerns for system fabrication.[1]

Another notable issue is that many OSCs suffer from poor environmental and electronic stability. Hence, even small exposure with ambient conditions can affect the stability of the device and the resistive state retention. [1,26] Moreover, in OSCs the device speed is often hindered by the electronic and ionic mobilities, while defect-related configurations in the atomic structure of the material can further limit the speed of organic devices.[1]

9 Conclusions

9.1 Status of neuromorphic computing

Neuromorphic computing has reached a stage of progress where the first functioning neuromorphic chips have been developed. In addition, many small-scale memristive device arrays have been built to demonstrate the effectiveness of neuromorphic systems for in-memory computing. However, there is still much work to be done before a true breakthrough. While this thesis prioritized discussing neuromorphic computing from the memristive device perspective, it is worth noting that this is just one part of the complex architecture of the neuromorphic systems.

In neuromorphic computing, memristive devices need to be viewed as a part of more sophisticated systems. This needs to be done by utilizing different algorithms. Currently most existing algorithms are still based on traditional computing logic, therefore further development is still required. However, it could be possible in the future some of the issues related to memristive devices to be mitigated or fixed using advanced algorithms and more optimized circuitry.

9.2 Status of memristive devices

In this work PCM, Ferroelectric memory devices, ECM, VCM and NW-based devices are discussed, and from materials perspective 2D and organic materials were highlighted. Additional switching mechanisms exist based on charge trapping and electron spin manipulation. The discussed memory technologies were chosen for their relevance in neuromorphic computing applications. Even though this work focused on the utilization of memristive devices in neuromorphic computing, their individual functionalities could be utilized outside of these applications. Many of the memristive devices are compatible with existing CMOS-technology. While neuromorphic computing is still many steps away from becoming commercialized, there could be applications for in-memory computing in more traditional systems.

The main limitations for all the discussed memristive technologies are scalability, reliability and cyclic endurance issues. The scalability problem could be tackled with

advances in device fabrication and the utilization of innovative materials, such as 2D materials. Reliability is an issue mainly caused by variables related to resistive switching mechanisms. The only way of resolving these issues is the extensive study and fundamental understanding of the switching mechanisms. The cyclic endurance is a difficult challenge in many of the presented memory devices, and it corresponds to an obstacle for commercial implementation.

It is apparent that several issues associated with the operation of memristive devices need to be resolved before neuromorphic computing can make new significant technological advances. Consequently, concepts related to memristive devices will remain an interesting, active and topical field of study, while breakthroughs could help the current computing systems to take their next leap forward.

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