Structurally simplified GCMO crossbar design for artificial synaptic networks

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Harnessing the full power of memristors as artificial synapses demands a simple and scalable crossbar architecture enabling their seamless integration into diverse applications. This letter presents the 3×3 memristor crossbar array configuration featuring a grid of interconnected devices. The composition includes Al as the reactive top electrode connecting the device columns and $Gd_{1-x}Ca_xMnO_3$ (GCMO, $x = 0.8$) serving as the bottom electrode connecting the device rows as well as the memristive material eliminating the need for additional layers and fabrication steps. Controlled sized vias through insulating Al_2O_3 layer connect the electrodes forming the active interface. The idea is validated with a test sample of 3×3 crossbars with Au/GCMO/Al structure, Au enabling Ohmic contact to GCMO, with device resistive switching ratios mostly around 10^2 and yield of over 90%. The devised crossbar structure could provide a highly scalable, yet simple, geometry suitable for synaptic networks.

In recent years, memristors have emerged as a promising technology for neuromorphic computing systems due to their ability to emulate both synaptic weight modulation and the dynamic functionality of neurons[1,2]. These devices, which exhibit resistive switching (RS) behavior, can be fabricated from a variety of materials. Oxide-based materials such as HfO_2[3–9] and Ta_2O_5[10–12] have been well established in neuromorphic applications. Hindering their larger scale utilization is their localized filament-type resistive switching, known for the need for an electroforming process, the stochasticity of conductive filament formation and rupture, and relatively low device yield[2].

Cation-doped perovskite manganite oxides, such as $La_{0.7}Sr_{0.3}MmO_3$ (LSMO)[13], $La_{0.7}Ca_{0.3}MnO_3$ (LCMO)[14], and $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO)[15–17], have garnered considerable attention for their promising properties for neuromorphic computing systems[18,19]. These materials share the key factor of highly mobile oxygen vacancies within the lattice, enabling the high resistance state through the electric field-induced oxidation of the active electrode metal, simultaneously modifying their distribution in the material, with controlled reduction reactions enabling the return to the low resistance state[2,18–20]. One such perovskite manganite, $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO), has been proposed as a potential candidate for memristive systems[21–23]. GCMO-based devices are compliance-free and forming-free[21] requiring no larger forming voltages, a feature also reported with PCMO-based memristors[24].

The coveted crossbar architecture, usually a two-dimensional grid of intersecting wires, offers a scalable and compact design for memory and neuromorphic computing applications[25–28], a structure also utilized for PCMO[29,30]. Among perovskites, GCMO stands out due to its higher optimal cation doping[21], coupled with the gradual transition from insulating to metallic behavior at high doping concentrations[31], presenting an advantageous feature for efficient charge transport within the bottom electrode of the crossbar array. In comparison to existing PCMO crossbars[29,30], the number of needed layers and fabrication steps is reduced due to the omission of a separate bottom electrode. This offers a way to decrease fabrication-related costs without compromising the usability and properties of the memristor devices. When pairing GCMO with aluminum, Al_2O_3 is formed at the interface, mirroring the behavior of other perovskite manganites[2,18,19]. The higher interface resistivity, attributed to the insulating oxide barrier at the interface, combined with the relatively low bulk resistance of GCMO (especially around $x = 0.8$)[21,31–33], presents an opportune feature combination for the presented crossbar structure. The employed GCMO

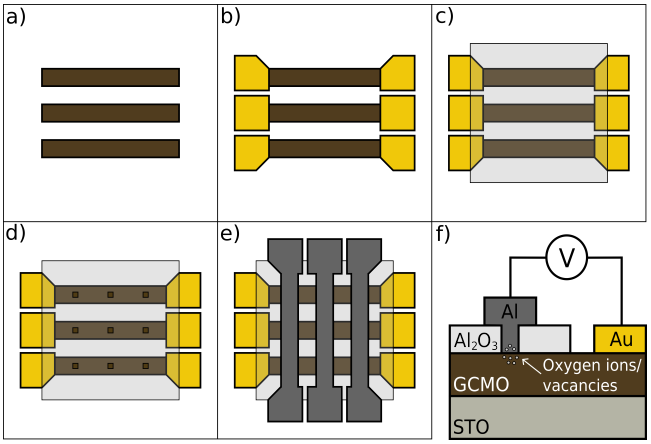

FIG. 1. Schematic of the crossbars, not in scale. a) Patterned GCMO layer. b) Patterned Au pads at the ends of GCMO stripes. c) Insulating Al_2O_3 layer covering the previous layers. d) Controlled size vias through the oxide layer. e) Patterned Al stripes, and filling of the vias. Completed design with a 3×3 crossbar array. f) Final device cross-section with oxygen ions/vacancies moving at the active GCMO/Al interface.

doping concentration, $x = 0.8$, also corresponds to the lowest Poole-Frenkel trap energy level of 0.3 eV, which coincides with the highest RS ratios[21,34].

This study explores the viability of our proposed GCMO-based memristors crossbar architecture. Investigation of GCMO-based memristors' behavior in the crossbar configuration is crucial for advancing the understanding of the material's potential as a building block for next-generation non-volatile memory and synaptic networks. Through a thorough analysis of GCMO's resistive switching characteristics when paired with Al in a crossbar architecture, we aim to contribute valuable insights to the ongoing efforts in optimizing oxide-based materials for broader applications.

An 80 nm thick GCMO thin film was deposited on top of a 5 mm × 5 mm single crystal $SrTiO_3$ (100, Crystal GmbH) by pulsed laser deposition (PLD) according to the process and parameters detailed in our previous works[35,36]. The film was patterned to 200 μm × 1.6 mm stripes with maskless photolithography and wet chemical etching (Fig. 1a). The second step in the fabrication process included depositing 100 nm thick Au pads utilizing a lift-off process with photolithography and Electron Beam Evaporation (E-beam) at the ends of the GCMO stripes (Fig. 1b). Even though the GCMO layer acts as the bottom electrode, we opted for Au pads to ensure Ohmic contact with the GCMO stripes, other alternatives being Au wire bonding or suitable probing stations. The advantage of the chosen geometry comes from omitting a separate device-connecting bottom electrode fabrication step, simplifying the fabrication process, especially when the selected means of forming the Ohmic electrical contact does not require additional fabrication. The whole sample surface was covered with an insulating and uniform, 10 nm thick, Al_2O_3 layer deposited with Atomic Layer Deposition (ALD) (Fig. 1c). The insulating layer was thick enough to guarantee sufficient insulation. To access the GCMO layer, controlled-sized vias (15 μm × 15 μm) were required in the Al_2O_3 layer. We opted for laser writer and photolithography, followed by Ar-ion milling with Broad Ion Beam (BIB) (Fig. 1d). Subsequently, these vias were filled with 50 nm of our active electrode material, Al, providing us with the rectifying interface for the memristor. The striped pattern of 150 nm thick and 200 μm wide (excluding end pads) Al, i.e., the top electrode connecting the crossbar, was then created using a lift-off process and E-beam (Fig. 1e). A schematic of the sample fabrication process (steps a–e) and cross-section of one device (f) is presented in Fig. 1.

The electrical contacts to the devices were obtained with an ultrasonic wire bonder and 33 μm thick Al wire, bonding to one Au pad and Al wire per row or column in the crossbar (one contact for each bit and word line). Each crossbar had 3×3 devices, and in total two crossbars (18 devices) were characterized. Electrical measurements were done with the ArC ONE memristor characterization platform[37] and a Keithley 2614b source meter with a measurement program written in Python. The selected measurements were varying voltage range repeated sweep *IV* measurements constrained by V_{min} and V_{max}, as well as fixed range *IV* measurements, retention, and endurance tests, all recognized as essential electrical parameters for characterizing memristors[38]. The employed sneak-path mitigation technique was the *V*/2 biasing scheme[39], where the other bit and word lines are biased to half of *V*, ensuring that at most half of the applied voltage affects the other devices.

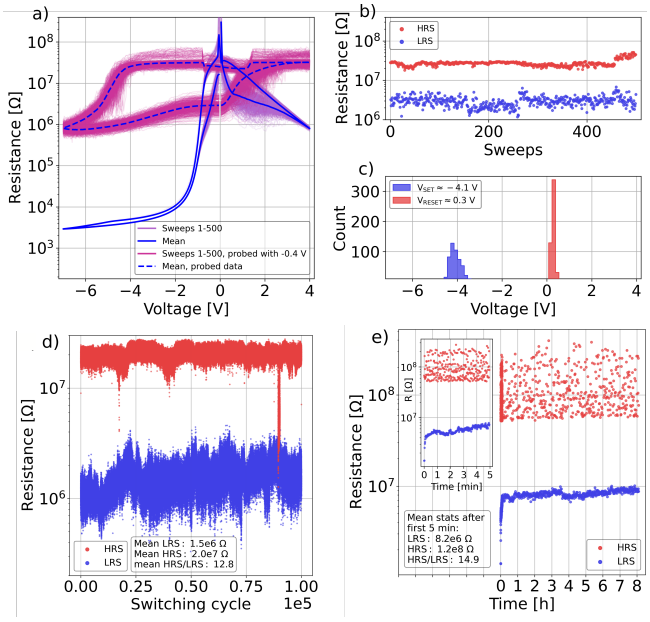

FIG. 2. a) *RV* plot of 500 sweeps for one device with calculated mean (solid blue), and with corresponding V_{probe} = -0.4 V probed *RV* with calculated mean (dotted blue). b) HRS and LRS values extracted at -0.4 V from probed data, presented over the measured 500 sweeps. c) Histograms of the extracted V_{set} and V_{reset} values. d) Write endurance of one device, 10^5 switching cycles, utilizing current-visible pulsed voltage stresses (PVS). One cycle comprises five 0.2 ms pulses of -7 V and 4 V. The device failed the reset process to HRS in some cycles and displayed notable variance in both HRS and LRS. LRS had more variance between cycles. e) State retention of HRS and LRS for one device for 5 min (inset) + 8 hours (main), V_{read} = -0.4 V. States were set by twenty 20 ms pulses of -7 V and 4 V. Fast relaxation of LRS at the start, after which the state stabilizes. High HRS variance is due to ArC ONE's detection limit.

All characterized devices exhibited similar results in the measurements. In all panels of Fig. 2, we present results for only one device as an illustrative case to highlight their performance in detail. Fig. 2a provides an *RV* plot from Keithley measurements (500 sweep *IV*, voltage range -7 V to 4 V), with the included probed -0.4 V measurement. The shape of the curve is characteristic of bipolar RS, and the gradual changes between the high and low resistance states (HRS and LRS, respectively) indicate analog operation suitable for artificial synapses[40,41]. The conduction model for GCMO has been previously studied, concluding that there is a coexistence of both Schottky and Poole-Frenkel conduction models[21]. Fig. 2b showcases the HRS and LRS values extracted at -0.4 V from the probed data, with quite stable one order of magnitude RS ratio (HRS/LRS) displaying small cycle-to-cycle variation, HRS being the more stable of the two states. Fig. 2c includes the V_{set} and V_{reset} histograms collected from the probed

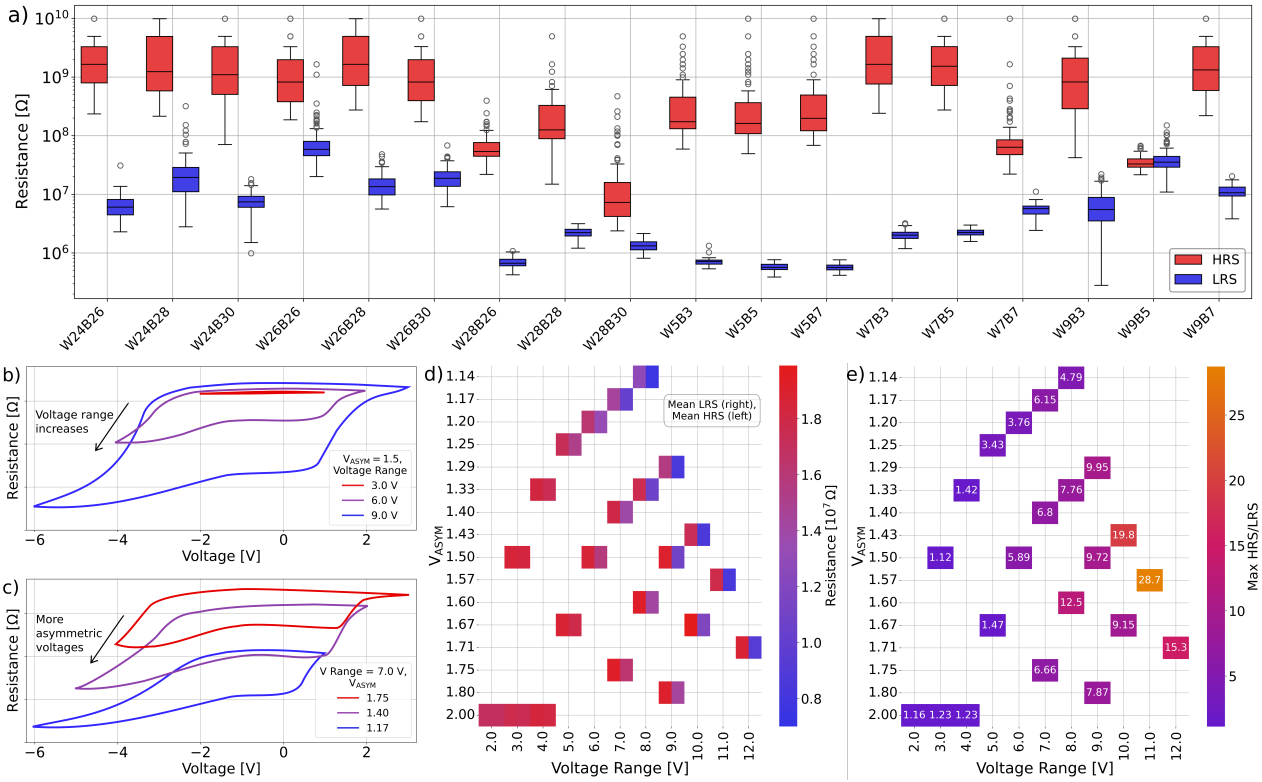

FIG. 3. a) Device-to-device variability from 100 sweep *IV*s, featuring values extracted directly from *RV* curves at -0.4 V. Even though the resistances of the devices differed, the *IV* curve profiles were similar, and 17 out of 18 devices had distinguishable HRS and LRS. b) Schematic of how changing the voltage range with constant $V_{\text{asym}} = 1.50$ modifies the probed resistance data. c) Schematic of how changing the V_{asym} with constant voltage range$= 7.0V$ modifies the probed resistance data. Heatmaps presenting the) mean LRS (right side of the squares) and mean HRS (left side of the squares) resistances within the same plot and the e) max HRS/LRS across a range of voltage values ($V_{\text{max}} - V_{\text{min}}$) and asymmetry ($V_{\text{asym}} = (V_{\text{max}} - V_{\text{min}})/|V_{\text{min}}|$) conditions. The first heatmap with HRS and LRS values depicts the average resistance values of all measured devices obtained from *IV* sweeps conducted at different voltage ranges, and the max HRS/LRS heatmap depicts the maximum ratio obtained during the varied *IV* sweeps. The modifiability of LRS (color change in the heatmap), thus the HRS/LRS ratio, supports the possibility of utilizing this material and device/crossbar geometry for a synaptic network, as the states are programmable via altering the voltage range and asymmetry.

RV data according to the following 5+5% criteria: The rule for V_{reset} (transition from LRS to HRS): resistance increases 5% compared to the mean of already checked points and the average of the next four data points also an additional 5%, and the rule for V_{set} (transition from HRS to LRS): resistance decreases 5% compared to the mean of already checked points and the average of the next four data points also an additional 5%. The values for V_{set} and V_{reset} are highly asymmetric reflecting the asymmetric and self-rectifying nature of the *IV* curve also characteristic for PCMO memristors[42]. Increased asymmetry can offer many advantages, especially concerning sneak-paths[43,44]. The *RV* plots from *IV* measurements capture the RS behavior, and the extracted or probed HRS and LRS values at -0.4 V and the V_{set} and V_{reset} values provide insights into the stability of the phenomenon across different measurement techniques.

The write endurance of one GCMO-based device subjected to 10^5 switching cycles is illustrated in Fig. 2d. Current-visible pulsed voltage stresses (PVS) suggested by Lanza *et al.*[45] were applied with alternating -7 V and 4 V of five 0.2 ms pulses revealing mostly sustained RS, with only a few cycles where the device had problems resetting to HRS. Similarly to other measurements, HRS seems more stable over time, as LRS drifts slightly towards HRS decreasing the achieved HRS/LRS ratio. After the measured switching cycles the two states are still clearly distinguishable with about one order of magnitude ratio indicating maintained endurance capabilities even over the measured switching cycles. Linear fitting of the data indicated that the LRS reaches the HRS in approximately 10^7 switching cycles.

Fig. 2e depicts the state retention characteristics of HRS and LRS in one GCMO-based device over 8 hours, after the LRS and HRS states were set. The inset focuses on the first five minutes, revealing a swift relaxation of LRS. After the fast initial relaxation/drift of LRS typical for perovskite manganite oxides[42,46,47], the states of the device usually stabilize over time. Within the time frame measured, HRS remained stable and LRS only slightly drifted towards HRS. Linear fitting of the data suggests state retention exceeding 10 years, with the resistances of both states increasing over time. One order of

magnitude ratio (calculated from mean HRS and LRS resistances) was present throughout the measurement, emphasizing the long-term stability of the RS states. The high variance in HRS is attributed to ArC ONE's detection limit.

Fig. 3a depicts the device-to-device variability observed in the studied crossbars via resistance box plots derived from 100 sweep *IV*s (*RV* plots), featuring values extracted directly from *RV* curves at -0.4 V. Most of the devices exhibit RS ratios of over 10^2, some even up to 10^3, not to be confused with the RS range or states gained from probed *IV* measurements depicting the remnant RS. There were considerable differences in the resistance levels of the devices, suggesting some inconsistencies in the fabrication process of the crossbars, e.g., resulting in slight variations in device areas. The interface quality could also be improved with additional optimization of the fabrication procedure. Furthermore, the chosen operation voltages, which were identical for all measured devices, are not optimized for each device individually, thus they do not account for device-to-device behavioral variations. Therefore, the results in Fig. 3a should be interpreted as an initial validation of the concept, rather than the final optimized result. Despite the variability in resistances, the *IV* curve profiles were similar, all exhibiting bipolar RS. The similarity in *IV* curve profiles across devices and the distinguishable HRS and LRS states in 17 out of 18 devices highlights the robustness and consistency of the RS phenomenon in the suggested device configuration of GCMO-based memristors, even in the presence of inherent device-to-device variations.

Additional measurements were done to understand the modifiability and programmability of the states with the employed voltage range ($V_{\mathrm{max}} - V_{\mathrm{min}}$) and asymmetry ($(V_{\mathrm{max}} - V_{\mathrm{min}})/|V_{\mathrm{min}}|$) of the voltages. Fig. 3b and c depict schematically how changing the voltage range with constant $V_{\mathrm{asym}} = 1.50$ or how changing the voltage asymmetry with constant voltage range $= 7.0$ V modifies the probed resistance data. While increasing the voltage range the HRS will remain mostly constant, and the LRS resistance decreases increasing the RS ratio. Modifying the voltages to be more asymmetric, the RS ratio will remain mostly constant as the overall resistance (both HRS and LRS) will decrease.

Fig. 3d collects the extracted HRS (left side of squares) and LRS (right side of squares) from varying voltage limit (V_{min} and V_{max}) *IV* measurements done on all 18 devices determined similarly as in Fig. 2b. Each point in the heatmap represents the average achieved value for the resistance states across all devices for that specific voltage range and asymmetry combination. The color changes over the different parameter axes, voltage range and asymmetry, depict the changes in mean HRS and LRS values, illustrating the potential of GCMO crossbar architectures for synaptic networks. Fig. 3e presents the highest achieved HRS/LRS ratios over the altered asymmetry and voltage range. The programmability of states, particularly LRS, can be achieved through adjustments in voltage range and asymmetry, as was schematically shown in Fig. 3b and c. This enables us to access more than the two main states through different programming sequences. This observation highlights GCMO's adaptability, aligning with the requirements for neuromorphic applications, where controlled variations in states are crucial for efficient computing systems. The figure underscores GCMO's versatility and its promising role in the development of programmable synaptic functionalities. Although spike-timing-dependent plasticity (STDP) has not been studied with the presented crossbar structure, the measurements with planar GCMO-based memristors have proven the possibility of utilizing the material as a bio-plausible synapse[23].

To successfully implement memristor crossbars as synaptic networks, it's crucial to increase the array size and validate the feasibility of wafer-scale manufacturing processes at an industrial scale. Scaling up the presented crossbar design to wafer-scale and larger arrays introduces a new set of challenges. While the commonly used PLD fabrication is suitable for operations on a smaller scale, it becomes an expensive method when used to create thin films on wafer-scale substrates. The presented crossbar architecture with GCMO acting as both the bottom electrode and memristive material opens up the possibility of utilizing chemical solution deposition (CSD)[48,49] for thin film fabrication to its fullest potential in the future. The CSD process for fabricating GCMO thin films is more environmentally friendly and cost-effective than the more frequently used PLD method, and it allows us to fabricate wafer-scale thin films. The ease of fabrication with CSD could be combined with the designed crossbar structure, enabling simple and cheap chip alternatives for edge computing and neuromorphic solutions. As of now, the PLD-fabricated thin film quality surpasses that of CSD-fabricated[48], guiding our choice to utilize PLD-fabricated GCMO for this work.

Increasing the size of the array, i.e., the number of rows and columns, increases the complexity of the fabrication process and the control of individual devices becomes more difficult. The resistances of the top and bottom electrodes become more significant due to increased lengths and decreased widths of patterns. Given that GCMO is more resistive than common metals[31], the simplified crossbar structure results in higher line resistances than there would be with a separate metal bottom electrode. Increased line resistances of the electrodes will hinder the operation of the devices through a so-called *IR* drop, causing decreased read margin between states and increased power consumption by higher operation voltages[39,50]. On the other hand, with high cation doping ($x = 0.8$) GCMO exhibits metallic behavior[31], supporting its usability as the connecting medium in the crossbar.

The density of the devices could be enhanced by the miniaturization of individual memristors, decreasing the size of the device's active area (lateral size). This approach might cause unexpected changes in device performance, e.g., worse endurance of the HRS and LRS states, due to there being fewer RS-inducing intrinsic defects in the decreased memristive active material volume[45]. When dealing with interface type RS, the device resistance should increase as the active area decreases, impacting the operation voltages and currents of the devices[18]. Higher overall resistances of the GCMO devices will limit unwanted currents in addition to decreasing the power consumption on the devices. Inherently, larger crossbars will also encounter more issues with sneak currents due to the increased number of potential pathways. The opera-

tion voltage scheme ($V/2$) for the sneak-path mitigation used in this work could be applicable for larger crossbars as well. With larger crossbars, the biasing scheme needs to be considered carefully, as the power consumption of the $V/2$ technique is higher than only applying voltages to the selected cell[39]. Common hardware strategies to overcome the sneak paths include the use of highly self-rectifying memristors or the incorporation of additional selector devices such as transistors and diodes within the array, all limiting the sneak currents through the unselected devices due to having rectifying or highly nonlinear IV behavior[1,39].

In summary, we presented a scalable design for GCMO-based memristors using a simplified crossbar array structure. The specific layer configuration of Au/GCMO/Al, in conjunction with the crossbar structure and controlled-sized vias through insulating Al_2O_3, resulted in a high yield of memristors exhibiting RS ratios mostly around 10^2, retention exceeding 10^4 s, and endurance surpassing 10^5 cycles. The multilevel RS, which arises from the tunable LRS, paves the way for future utilization of these crossbars as synaptic networks. This work emphasizes the potential of GCMO-based memristors in neuromorphic applications and offers beneficial insights into optimizing their synaptic behaviors by varying the operational voltages, while also identifying the need for further research related to improved device manufacturing.

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AUTOR DECLARATIONS

Conflict of Interest Statement

P. Paturi, A. Schulman, and H. Huhtinen have Patents FI20205101 (31.1.2020), PCT/FI2021/050057 (29.1.2021), TW110103063 (27.1.2021)[33].

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Author Contributions

Anni Antola: Conceptualization; Formal Analysis; Investigation; Methodology; Visualization; Writing - Original Draft. **Ilari Angervo:** Conceptualization; Writing – Review and Editing. **Hannu Huhtinen:** Conceptualization; Supervision; Writing – Review and Editing. **Mikko Miettinen:** Resources. **Alejandro Schulman:** Conceptualization; Writing – Review and Editing. **Petriina Paturi:** Conceptualization; Funding Acquisition; Project Administration; Supervision; Writing – Review and Editing.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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