Engineering the bottom electrode to enhance functionality in GCMO memristors

Master's thesis
University of Turku
Physics
2026
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UNIVERSITY OF TURKU
Department of Physics and Astronomy

Afrin, Poroma Engineering the bottom electrode to enhance functionality in GCMO memristors

Master's thesis, 64 pp.
Physics
June 2026

The development of the history of society via complementary metal-oxide-semiconductor (CMOS) transistor scaling under Moore's Law is currently attaining a conclusive high point due to significant physical and economic limitations. Quantum tunnelling makes it difficult to scale down devices because it leads to power loss and overheating. Rising manufacturing and cooling costs threaten long-term computing growth. The Von Neumann architecture has kept processors and memory apart since 1945. This has made modular design possible, but it has also caused the Von Neumann bottleneck, which is a slow, high-power-consuming data transfer. This limit makes modern workloads worse, and people are more interested in brain-inspired artificial neural networks because of it. Even with improvements like graphics processing units (GPUs) and tensor processing units (TPUs), traditional CMOS systems still have problems with scaling and energy use because of the Von Neumann bottleneck. Neuromorphic computing solves this problem by combining memory and processing, which makes brain-like computation possible. Memristors are strong candidates for neuromorphic computing as they emulate neurons and synapses through history-dependent conductance changes. They also provide fast switching, low power consumption, and high reliability, making them suitable for next-generation memory.

In this thesis, I have studied the fabrication process of $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) with different buffer layers such as Nb-doped STO (Nb:STO) and $SrRuO_3$ (SRO) between $SrTiO_3$ (STO) substrate and GCMO. Additionally, Nb-doped STO (Nb:STO) has been utilised as a substrate (no buffer layer) in one sample and another sample with STO (no buffer layer). The fabrication methods that were used in this thesis were pulsed laser deposition (PLD), photolithography with etching, and electron beam evaporation (E-beam). Four samples were fabricated using these methods. The structural characterisation of the fabricated sample was performed mainly using X-ray diffraction (XRD) and atomic force microscopy (AFM), with GCMO growth and surface quality checks. And the result shows a good growth of GCMO on top of the substrate and buffer layers. The electrical transport measurements using Keithley and ArC ONE indicated some variation in resistance and current at the final device connection of each fabricated sample. For the electrical characterisation, these designs for memristive properties need further study, as the device-to-device variation was not as expected.

This study compares buffered and unbuffered samples to understand how the bottom electrode influences the growth of GCMO and the memristive properties of the GCMO memristor. This work is important for optimising device performance and improving the design of future neuromorphic applications.

Keywords: Neuromorphic computation, resistive switching, memristor, GCMO, memristor crossbar, bottom electrode, buffer layer.

Contents

Preface

This study focused on the effect of bottom electrodes (buffer layers) on the performance of manganite oxide-based memristor devices, with the primary objective of analysing how different buffer layer materials affect GCMO growth and overall memristive properties. As standard computer chips reach their physical limits, neuromorphic computing offers a new way forward by working like the human brain. Memristors are a key part of this technology because they can act like artificial brain synapses. By testing different bottom electrode materials, this study aims to help future memory device engineering be more reliable and efficient for artificial intelligence hardware.

In this study, all four thin films have been fabricated with slightly different structures to observe the GCMO growth on each chosen substrate and buffer layer top surface. The crystallographic and morphological analysis in this study shows that all the GCMO layers were formed perfectly on top of the substrate and buffer layers. X-ray diffraction and AFM analysis confirmed good crystalline growth and epitaxial alignment. However, the electrical transport measurements revealed that the electrical properties did not behave as expected for standard memristive operations. The expected resistive switching hysteresis was absent under the initial testing parameters. Consequently, this study requires further observations, including deeper interfacial defect analysis and modified electrical measurement conditions, to completely understand the underlying transport mechanisms.

In future work, this analysis can be used to address the electrical issues and improve the switching performance of these types of memristor device configurations. By building on the perfect thin-film growth achieved in this study, researchers can find the right bottom electrode to make the memristors more reliable and stable.

1 Theory

1.1 Neuromorphic engineering

Neuromorphic computing has been developed to address the shortcomings of the conventional Von Neumann architecture. Since data processing requires constant data movement between the central processing unit (CPU) and memory, a shared connection between the CPU and a separate memory unit was necessary. Consequently, by widening the gap between the processor and memory speeds, this designed structure produces a memory wall [1]. Minimal power consumption is essential for high-efficiency computing, and to address this matter, researchers are turning to neuromorphic engineering, which uses computer hardware to create a structure resembling the human brain [2, 3]. Compared to traditional computers, the brain uses much less energy when doing complicated calculations. Neuromorphic systems aim to mimic neurons and synapses, two essential components of the brain. Neurons control information processing in the system, whereas synapses control signal transmission and memory storage. In this approach, computational efficiency is improved, and the requirement for continuous data transport is decreased by moving closer to the memory. This is achieved by implementing learning mechanisms, such as Spike Timing Dependent Plasticity (STDP), directly into the hardware [2, 3].

Complementary Metal-Oxide-Semiconductor (CMOS) and artificial neural circuits were successfully combined to create the first fully manufactured neuromorphic hardware in the early developments. Based on this concept, the first neuromorphic circuit was created using metal-oxide-semiconductor field-effect transistors (MOSFETs). However, in order to simulate a single neuron, CMOS-based configurations need a large number of transistors and constant power to preserve the stored data. Because of this, a different device is required to address this, and researchers have discovered a component that is especially memory-based, namely, memristors. Be-

cause they integrate memory while simultaneously performing computation in a single device and use very little power, memristors are intriguing technologies for neuromorphic applications. Their great durability and ability to store information even in the event of a power outage, a feature known as non-volatile memory, are advantages. They are an ideal platform for creating effective neuromorphic neural circuits due to these qualities [2–4].

1.2 Memristors

Memristors have attracted interest as an emerging technology for neuromorphic computing systems because they can emulate key functional properties of biological synapses and neurons, particularly those of the human brain. A memristor is a basic two-terminal electronic part that connects electric charge and magnetic flux. The word "memristor" comes from the words "memory" and "resistor". People often call it the "fourth fundamental circuit element," along with the resistor, capacitor, and inductor [5]. Its main feature is that it remembers its internal resistance based on the voltage and current that have passed through it in the past. One of the main characteristics of memristors is their resistive switching (RS) behaviour, which allows them to retain information and change electrical resistance between states. Among the great variety of materials, oxide-based materials like tantalum oxide TaO_2 [6–8] and hafnium oxide HfO_2 [9–15] have been extensively employed and researched in neuromorphic applications. However, because their resistivity change usually takes place via the localised conductive shorter channel known as a filament, produced inside the material, these materials have certain systematic constraints when scaled up. Because of their stochastic filament formation, unstable switching behaviour, and decreased device yield, they pose problems for large-scale integration [16].

In light of these constraints, studies have investigated cation-doped perovskite manganite oxides as substitute materials, such as $La_{1-x}Sr_xMnO_3$ (LSMO) [17],

$La_{1-x}Ca_xMnO_3$ (LCMO) [18] and $Pr_{1-x}Ca_xMnO_3$ (PCMO) [19, 20] and these materials show promising neuromorphic computing [21, 22] due to the significant mobility of oxygen vacancies within their crystal structure. The materials can transit from a high resistance state (HRS) to a low resistance state (LRS) when subjected to an electric field due to the migration of these oxygen vacancies. This is an interface-type switching mechanism in general, in which the resistive switching behaviour peimarily occurs at the interface between the manganite layer and active electrode. In particular, the application of an electrical field causes the active electrode metal to oxidise and redistribute oxygen vacancies within the material, resulting in the HRS. On the other hand, a regulated reduction process and the restoration of the LRS can reverse this effect [16, 21–23]. Compared to filament-based switching, this method exhibits a more consistent and regulated switching mechanism.

Memristors can have a variety of fundamental structure geometries. For example, the planar (in-plane) memristor or a capacitive memristor crossbar array arrangement has been extensively researched because of its potential behaviour as a neuromorphic device basis [4, 24–26].

1.2.1 Resistive switching and its classifications

Resistive switching is a physical phenomenon in which a strong external electric field causes a dielectric material's resistance to change non-volatilely. This external electric field can also be used to non-destructively measure the device's resistivity, which can be repeatedly changed and returned to its initial state [27]. Numerous insulating materials [28], such as oxides [29], nitrides [30, 31], chalcogenides [32], semiconductors [33], and organic materials [34, 35], exhibit this phenomenon; nevertheless, the oxides have been the subject of extensive research.

In the case of memristor devices, the electrical components maintain their internal resistance based on their history of applied voltage and current. Many research

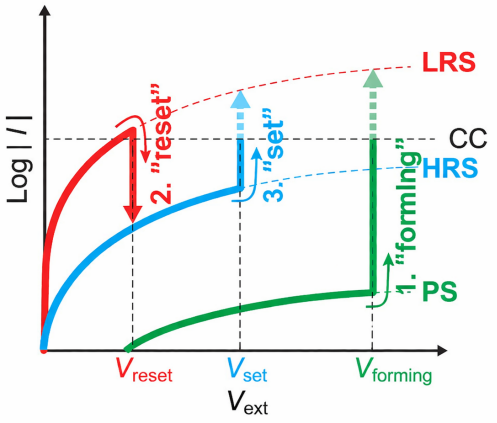


Figure 1. This resistive switching (RS) schematic $I-V$ curve shows that the device begins in a high-resistance pristine state. In the following figure, the strong electric field generates a sudden current increment known as (1) "forming", which switches it to the low resistance state (LRS). However, when an external bias is applied once more, known as (2) "reset", the LRS turns to the high-resistance state (HRS). On the other hand, an LRS, referred to as the "set", can be converted from an HRS (3). Reversible switching is possible between the HRS and LRS [27].

studies have reported resistive switching in memristive devices [36–39]. The RS devices' basic functionality is shown in Figure 1. Because of their large energy band gap, oxide materials have very high resistance in their initial state. When a high enough external voltage V_{ext} is applied, the device undergoes an electroforming process, as shown by the green line in the figure, and enters the low-resistance state (LRS), where the required voltage is termed the "forming voltage," V_{forming}. During the forming process, it is important to limit the flowing current; otherwise, the film will experience a complete dielectric breakdown. To prevent such irreversible damage, there should be a maximum value of flowing current, which is called the compliance current [27]. By adjusting the V_{ext}, the following forming process, it can be switched between the LRS and HRS. In the LRS, as V_{ext} increases, a sudden rise in resistance occurs, as indicated by the red curve of Figure 1. This is called the "reset" process, and the corresponding voltage is called the "reset voltage" V_{reset}. When V_{ext} increasing from zero once more, the device can be switched back to the LRS when V_{ext} reaches the set voltage, V_{set}, as shown by the blue curve in Figure 1,

and this process is called the "set" process [27]. This device can repeat this cycle numerous times, and these switching events can be sudden or gradual. Furthermore, the resistance levels are still visible despite variations, enabling the two states to represent binary data in non-volatile memory [27]. These two primary states, which correspond to low and high conductivity of the devices, are likewise present in GCMO memristor devices. The conductivity variation occurs due to two primary reasons: resistivity switching based on an electrochemical metallisation (local phase change from insulating to metallic) and a valence change. Compared to memristors with a planar structure, capacitive memristors are more frequently electrochemically metallised. The oxide material loses oxygen when an electric field is applied, which causes local metallisation and a conducting filament to form between the electrodes. When the filament is formed, dissolved, and reformed by the applied electric field via the weakest percolation path between the electrodes, the HRS and the LRS are accessed.

The switching mechanism of interface-type GCMO-based memristors is driven by a valence change, meaning that the migration of oxygen vacancies (or ions, depending on the type of semiconductor) at the interface between the oxide and the reactive electrode causes the change in conductance [27]. However, in the planar structure of GCMO memristors, the valence change occurs when the oxygen vacancies move at the interface between the oxide and reactive electrodes (such as the aluminium), which is primarily responsible for the switching. In this instance, the AlO_x layer's creation permits oxygen depletion in GCMO, and the movement of oxygen ions under an electric field changes the interface conductivity and barrier characteristics [24, 27].

Depending on whether the electric field's polarity influences the device's polarity or not, resistance switching is divided into three categories: unipolar, bipolar, and threshold switching, as shown in Figure 2. Set and reset voltages, V_{set} and V_{reset}, are

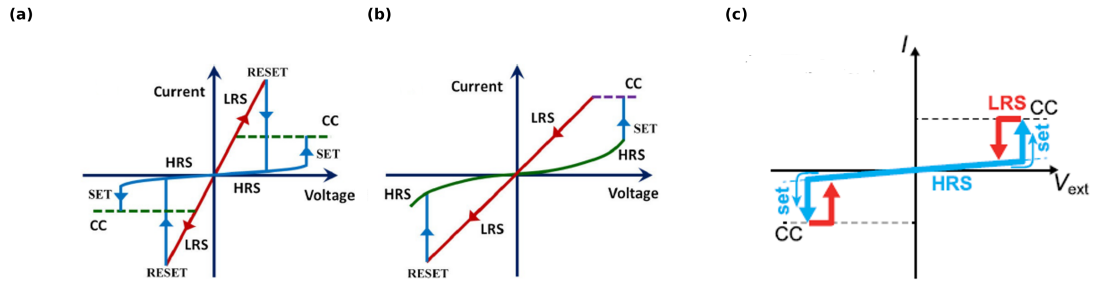


Figure 2. Characteristic $I - V$ curves that distinguish between high and low resistance states (HRS and LRS). (a) Unipolar switching devices, (b) bipolar switching devices [40], and (c) threshold switching devices [27].

the voltages required to switch between the HRS and LRS in the circumstances of the $I - V$-curve characteristics. In unipolar switching (Figure 2 (a)), a device switches between two stable resistance states. From Figure 2 (a), the entire switching cycle occurs within the same quadrant (the positive side of the graph). Starting from the origin in the HRS (lower blue line), the current increases as the voltage moves towards the right. Once it hits the vertical blue line labelled SET, the device jumps to the LRS (red line). Note the dashed green line labelled CC (current compliance), which is a limit set to protect the device. To go back, it continues in the same polarity. Following the red line, the current reaches a peak at RESET, where it suddenly drops back down to the HRS (the lower blue line). The V_{set} is further from the centre (larger amplitude) than the V_{reset}, and both are on the same side of the y-axis.

Bipolar switching is defined by the requirement of both voltage polarities to transition a device between resistance states. In a typical configuration, a negative bias initiates the reset process from a low- to high-resistance state, while a positive bias drives the set process back to a low-resistance state, though some systems may reverse this polarity logic. In Figure 2 (b), the switching behaviour is split across different quadrants, meaning polarity matters. On the right (positive) side, the device follows the green HRS curve until it reaches the SET point, where it jumps

up to the red LRS line (limited by the CC). To return to the high resistance state, it cannot stay on the positive side. It must sweep the voltage to the negative (left) side. Once the negative voltage reaches the RESET point, the current "snaps" back from the red LRS line to the green HRS curve. The SET and RESET operations happen on opposite sides of the vertical axis. This is the mechanism most commonly used for neuromorphic applications due to its stability.

Figure 2 (c) shows a "volatile" behaviour, where the device refuses to stay in the low-resistance state without an active field. Like the others, it starts in HRS. When the voltage reaches the SET threshold, the current jumps vertically to the LRS, and the red arrows point back towards the origin. As soon as the voltage V_{ext} decreases, the device does not stay in the LRS (red line); it automatically "drops" back into the HRS blue line before reaching zero. There is no "RESET" voltage required to bring it back to HRS; the device returns to its original state naturally when the power is lowered, making the graph look like two symmetric "wings" [27, 41]. Threshold switching is crucial for scientific and technological purposes, even though it's less frequent than unipolar or bipolar switching. It is also comparable to unipolar switching in that its $I - V$ behaviour is symmetrical with respect to polarity.

1.2.2 Switching in various geometries of memristive devices

Memristive devices are mainly made using capacitive and planar structures. An oxide thin film is positioned between the top and bottom electrodes of typical RS devices, which feature a two-terminal arrangement resembling a capacitor, as shown in Figure 3 (a). This design is easy to manufacture for real-world memory devices, but in particular, scientists have trouble watching the tiny conductive filaments that form and grow through the material when electricity is applied. To better monitor the changes that the material experiences during RS, some researchers have employed an in-plane design, Figure 3 (b), instead of a capacitor-like configuration

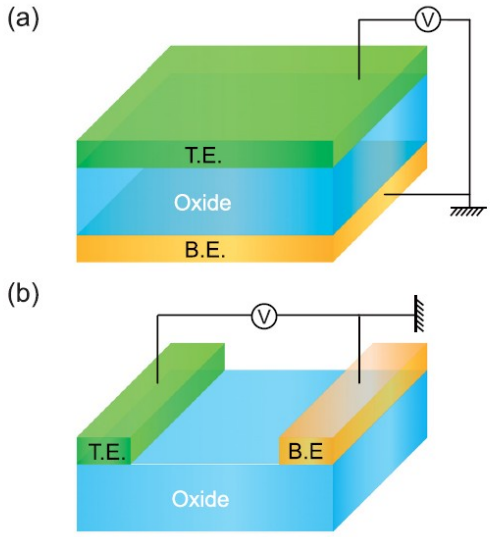


Figure 3. Schematics of a typical experimental setup for RS: vertical (a) and planar (b) structures. T.E. and B.E. refer to the top and bottom electrodes, respectively [27].

[42–45].

A planar structure is essentially a thin layer of memristive material, such as manganite, placed over an appropriate substrate, with electrical connections made between the selected active metal electrode and a non-active metal electrode. The memristor is "two-dimensional" since every component is positioned in a single plane. The interface between the active metal electrode and the memristive film plays an important role in device behaviour [24].

The LRS and HRS distance stays 2 or 3 magnitudes that also shown in the capacitor and planar structure. As it resembles the memory window and also depends upon the quality of the memristor devices according to their memristive behaviour. Previous research on resistive switching for GCMO ($x = 0.8$) was limited to planar geometry, where the switching was bipolar [24, 46]. Capacitive GCMO devices are expected to behave similarly based on the PCMO results. Three primary criteria are used to assess the quality of memristive devices in the planar configuration: asymmetry of the $I-V$ curve, which refers to the different paths of the $I-V$ curve in the

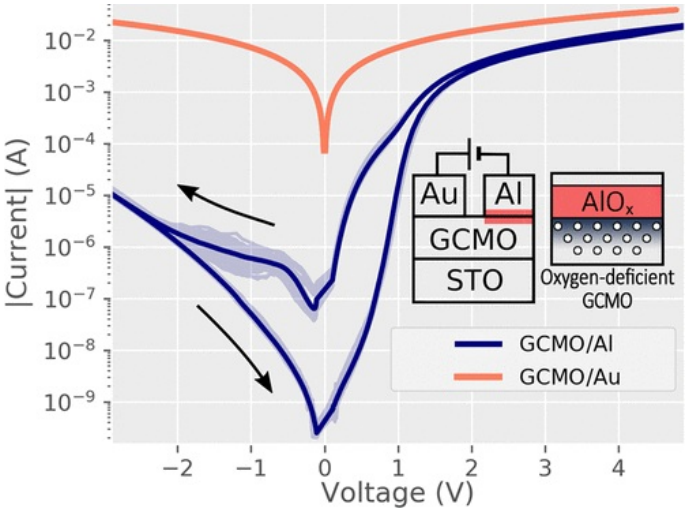


Figure 4. A planar GCMO (x = 0.85)-based memristor's characteristics $I-V$ curve and the corresponding schematic of the device layer structure [24].

positive and negative voltage sides; overall resistance level; and the ratio between LRS and HRS, which is shown in Figure 4.

The $I-V$ loops were measured by sweeping the voltage in a series of steps $0 \rightarrow V_{\max} \rightarrow -V_{\min} \rightarrow 0$ with linear amplitude progression, 100 ms step width, and a 100 ms low-voltage read between each step. The voltage amplitudes used to induce the LRS and HRS were selected to provide a sufficiently high switching ratio without causing any damage to the device and to prevent the sneak path from forming, particularly in crossbar array structures.

1.2.3 Mechanisms

The RS mechanism defines the conductive mechanism of memristors and is thought to be dominated by oxygen vacancy migration at the interface layer between the GCMO active layer and an active electrode, thereby forming an insulating oxide barrier layer [24, 27, 47]. The controlled electric field modifies the barrier properties. Similar findings, such as PCMO, which corresponds to the oxygen diffusion mode with oxygen vacancies accumulating near the active interface under an electric field, or, accordingly, oxidation of the active electrode, have been confirmed [48, 49].

The interface-driven switching mechanism in the Al/GCMO fundamental structure of the memristor under investigation is thought to depend on the formation of an AlO_X (Al_2O_3) interfacial layer at the active interface and a modulable high resistance barrier with the selected voltage pulsing methods [47]. The Schottky barrier properties are influenced by oxygen vacancies. The geometry shown in Figure 4 involves an interface between the electrodes and the oxide layer. Depending on the work function difference between the oxide and the metal electrode, a Schottky barrier can be formed. External bias changes the distribution and density of oxygen vacancies, which alters the height and width of the Schottky barrier, resulting in the resistance of the sample. It has been reported that oxygen vacancies can act as electron traps at the Schottky barrier region. In this case, the Schottky barrier modification due to the neutralisation of oxygen vacancies by the trapping of the electrons may produce RS phenomena [27].

Now, if we think about the addition of a buffer layer between the substrate and the active layer, the buffer layers in our study are strontium ruthenate (SRO) and Nb:STO. Strontium ruthenate (SRO) is a highly conductive oxide electrode and has a relatively low resistance of about $300\,\mu\Omega \cdot \mathrm{cm}$ [50], meaning current can easily pass through it. To guarantee that the interface between SRO and GCMO is non-rectifying, both of these are of the same semiconductor type (n-type)[46]. Because of its metallic-like conductivity and epitaxial growth on top of the STO substrate [51], SRO was used as the bottom electrode, offering an excellent growing medium for the GCMO layer. Furthermore, research has demonstrated that Nb-doping maintains good electrical conductivity while exhibiting homogeneous epitaxial growth on STO [52]. Therefore, Nb:STO is used as the substrate and buffer layer in our other two thin films. In this case, we used a 5% niobium-doped STO layer as the buffer layer between GCMO and STO, although we are unaware of the final concentration of niobium that was obtained during the deposition. 1% of niobium-doped STO has

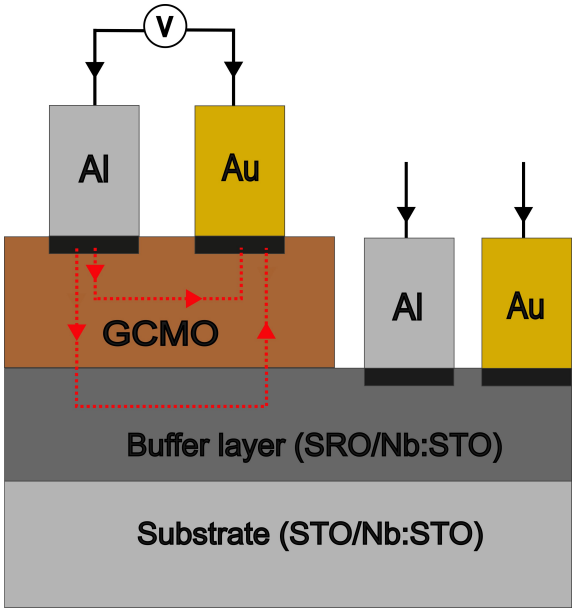


Figure 5. Structural design of the samples.

been utilised as a substrate in other thin films.

1.3 Materials

Several materials have been used in this thesis to create the memristive devices. In our sample, a buffer layer is introduced between the substrate and the active layer, with electrodes deposited on top, forming the sequence: substrate, buffer layer, active layer, and electrodes. The active layer and electrodes are composed of the substrate in two of these four thin films, which do not have a buffer layer. STO has been utilised as the substrate for three thin film samples, while Nb:STO has been used for one sample as a substrate.

In all four samples, GCMO was utilised for the device active layer, while SRO and Nb:STO were used for the buffer layers. Table I shows the sample design that has been created for this thesis work, and Figure 5 illustrates the structural design of the samples, and the red dotted line shows the conductive connections; the following sections describe details about the characteristics of these materials and why these materials fit for this structure.

Table I. Thin film structures made in the study.

Structure No.	**Substrate**	**Buffer Layer**	**Active Layer**	**Electrodes**
030226-1	STO	–	GCMO	Al-Au
030226-2	Nb:STO	–	GCMO	Al-Au
290126-1	STO	SRO	GCMO	Al-Au
030226-4	STO	Nb:STO	GCMO	Al-Au

1.3.1 Substrates

Strontium titanate ($SrTiO_3$), STO was the primary substrate used in our memristive thin-film measurements. Because of its similar perovskite crystal structure and electrical-chemical compatibility with several oxide-based switching materials, it is frequently utilised as the substrate in memristive devices. The lattice parameter of the cubic structure of the STO substrate is 3.901 Å [53]. To reduce the lattice mismatch between the substrate and the films, the films are expected to grow along the diagonal of the substrate unit cell, as the lattice parameters of the substrate and the GCMO bulk samples differ. STO is a desirable substrate for thin-film deposition due to its three-dimensional perovskite structure, as shown in Figure 6.

Because it will make the deposited thin film more likely to adopt a cubic structure, its cubic structure is especially appealing. Furthermore, STO can be made metallic by vacuum annealing or niobium doping to change conduction via different mechanisms to encourage oxygen reduction [17]. The unit cell of STO has planes of SrO and TiO_2, and at the surface of the perovskite, either the TiO_2 layer or the SrO layer can be exposed. A singly-terminated surface will either have an exclusively TiO_2-terminated or an SrO-terminated surface [55]. The termination type of the substrate is important because the order in which the atoms of thin films are deposited on the substrate, as well as the composition and characteristics of the film, are determined by the various microscopic interactions that the exposed atoms at

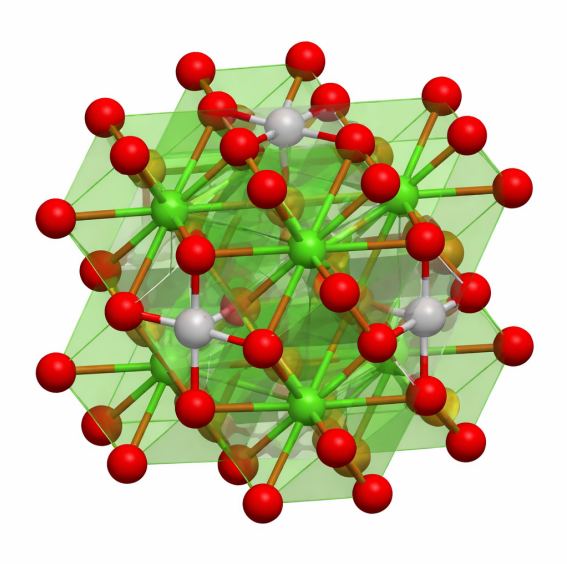


Figure 6. STO's crystal structure. Planes of TiO_2 are represented by the grey and red atoms, while planes of SrO are represented by the green and red atoms [54].

the surface will have with incoming ions during the film deposition process. Because it is more stable, a TiO_2-terminated surface is frequently thought to be ideal for the preparation of atomically smooth $SrTiO_3$ substrates [54]. STO has a broad bandgap ($\sim$ 3.2 eV) [56], which might help in controlling electric fields and reducing leakage currents, maintaining better switching performance, and ensuring device stability. In this thesis, STO has been employed as a substrate for these reasonable qualities; additionally, it has been employed for a similar reason in numerous other studies [24, 46, 57].

1.3.2 Active layer

The memristive material between the STO and Al layers, as well as between the buffer layers, was selected to be gadolinium calcium manganite oxide, $Gd_{1-x}Ca_xMnO_3$ ($0 \leq x < 1$), with a concentration of $x = 0.8$. Lähteenlahti *et al.*'s research indicates that this concentration is one of the most promising ones [24]. The migration of oxygen close to the Schottky contact between the manganite and the non-noble metal electrode is the most likely working principle in perovskite manganite memristors.

The oxidation of the metal and the high resistance condition are caused by oxygen migration from the active layer to the electrode. The memristor returns to its low resistance condition when the oxygen migration is reversed by an opposite voltage [36, 47].

$Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) is a perovskite-type crystal structure of mixed-valence manganite oxide. It has the general formula $R_{1-x}A_xMnO_3$ and crystallises in a structure of symmetry Pbnm. Figure 7 shows that manganese ions are located at the centres of corner-sharing oxygen octahedra, and Gd and Ca ions are located in the interstitial sites between the octahedra. In this structural family, R is a lanthanide cation, and A is an alkaline earth cation, while oxygen anions coordinate to all present cations [24, 53]. The structural distortion from the ideal cubic lattice to orthorhombic or tetragonal symmetry is attributed to the relatively smaller ionic radii of the A- or R-site cations (Ca or Gd) in comparison to the Mn cation. The result of this mismatch is a tilting and deformation of the MnO_6 octahedra. These distortions are crucial to the control of the physical properties of the material, including the initial phase of charge ordering [58]. Charge ordering is a kind of phase transition that involves the localisation of charge carriers, rather than their being mobile. Such localisation may lead to an ordered distribution of charges, usually called a chequerboard-like pattern in the lattice, and is usually accompanied by an increase in electrical resistivity [59]. Also, the distortion of the oxygen octahedra is inversely proportional to the electronic bandwidth. Hence, the stronger the distortions, the lower the magnetic ordering temperature and the higher the temperature at which the charge ordering occurs. In GCMO, the manganese ions are mainly antiferromagnetically ordered, particularly at a composition of $x = 0.8$. At this doping level, the Mn ions can also be in a magnetic cluster glass state. Bulk GCMO is typically metallic at $x = 0.8$ [53].

Several models are used to describe the electrical conduction mechanisms in ox-

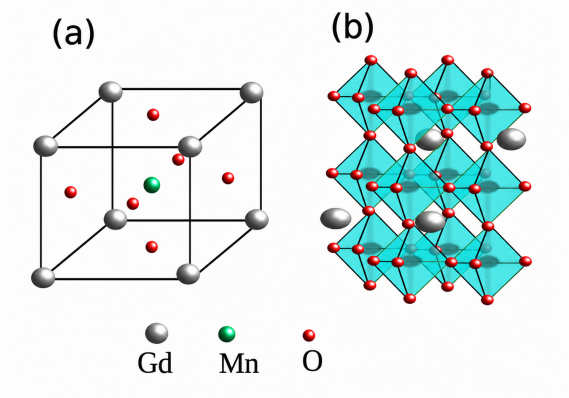


Figure 7. (a) Ideal cubic crystal structure of GCMO with atomic positions of Gd (or Ca), Mn and O. (b) The oxygen octahedra around the manganese centres in the perovskite lattice [53].

ide systems, such as ohmic conduction, space-charge-limited systems, Poole-Frenkel emission and Schottky emission. For Ohmic conduction, the material shows a linear relation between current and applied voltage, so the resistance is constant and the current increases with the applied voltage. Insulating materials often exhibit electrical conduction, which is described by the Poole-Frenkel effect. This model is based on the Pool-Frenkel effect, where the application of an electric field reduces the potential barriers associated with trap states to enable thermally assisted release and transport of electrons. Thus, the conduction mechanisms are dominated by trap-assisted conduction. Another important mechanism is the Schottky-type conduction, which is usually observed at metal-semiconductor interfaces. In this case, the current flow is controlled by the Schottky barrier formed at the interface between the two materials. This barrier affects the injection of carriers from the metal to the semiconductor and therefore limits the total current transport through the interface [60].

1.3.3 Buffer layer

Two materials, SRO and Nb:STO (niobium-doped STO), were created in our structures employing different buffer layers between the STO substrate and the active

Table II. Structural parameters and lattice mismatch of $SrRuO_3$ (SRO) and $SrTiO_3$ (STO) [50].

Material	Space Group	Structure	Lattice Parameters (Å)	Pseudocubic Parameters (Å)	Angle (°)	Mismatch (%)
$SrRuO_3$	Pbnm	$GdFeO_3$-type	$a_o = 5.53, b_o = 5.57, c_o = 7.85$	$a_p = 3.93, c_p = 3.93$	89.6 °	+0.64
$SrTiO_3$	–	Cubic	$a = b = c = 3.905$	–	90 °	−1.92

GCMO layer. The SRO has good surface smoothness, high crystalline quality, low resistivity, and excellent chemical and thermal stability. These substances are essentially isotropic pseudocubic perovskites [61, 62]. In the orthorhombic crystal system, the lattice is defined by three mutually perpendicular axes (a, b, and c), all of unequal length ($a \neq b \neq c$). This distortion is often due to the tilting or rotation of the internal octahedra, which breaks the symmetry of the perfect cubic form. Although the internal atomic shifts result in a real orthorhombic or tetragonal symmetry in many materials, such as perovskites, the lattice parameters are often close to each other, and the angles are close to 90°. When taking into account lattice mismatches, which affect the formation of SRO on top of STO, the pseudocubic lattice parameters are crucial. The space groups, lattice parameters, lattice distortions, and lattice mismatches of $SrRuO_3$, and $SrTiO_3$ are shown in Table II [50], and a schematic structure of SRO is shown in Figure 8.

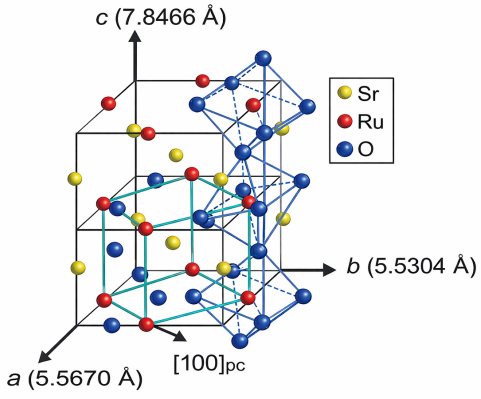


Figure 8. A schematic representation of the bulk orthorhombic unit cell of SRO. The RuO_3 octahedra and pseudocubic unit cell are represented by the thick cyan and blue lines, respectively [63].

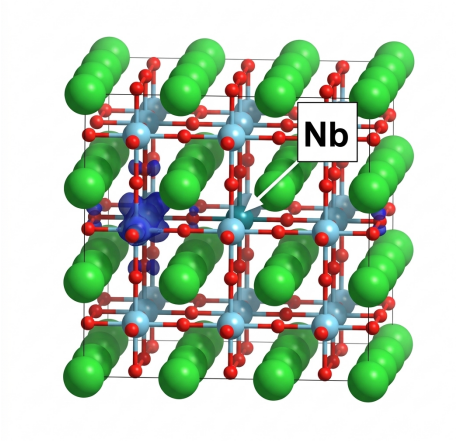


Figure 9. Sr, Ti/Nb, and O atoms are represented by the green (large), light blue/turquoise (middle-sized), and red (small) spheres, respectively [64].

At room temperature, the resistivity of SRO is less than $300\,\mu\Omega\cdot$cm [65]. The table II shows that when SRO is grown on top of an STO substrate, this slight difference in atomic spacing creates a small lattice mismatch of +0.64%. As this mismatch is remarkably low, SRO can grow with excellent structural quality, making it an effective buffer layer.

In the case of Nb:STO, it has also been used in our samples as a buffer layer for a similar purpose, and it is a cubic perovskite. The electrical conductivity $SrTiO_3$ can be easily tuned from an n-type semiconductor to metal-like conduction (up to $10^{-4}\ \Omega\cdot$cm) and even to superconductivity at low temperatures ($(T_c \approx 0.3\,\mathrm{K})$) when Ti is partially substituted with Nb [66–70]. The conductive Nb-doped $SrTiO_3$ with variable conductivity is not only used as a bottom electrode for the deposition of functional perovskite oxides [71–73] but also serves as an effective buffer layer. A schematic diagram of Nb:STO is shown in Figure 9. Nb:STO is an example of a donor-doped perovskite, where the dopant carries a higher positive charge than the ion it replaces in the host lattice. In this case, Nb^{5+} substitutes for Ti^{4+} in $SrTiO_3$, introducing an excess positive charge into a structure. As a result, the system tends to compensate by incorporating additional electrons or adjusting its oxygen content (when comparing Nb_2O_5 with two units of TiO_2). The resulting properties of Nb-

doped $SrTiO_3$ are strongly influenced by how this charge imbalance is compensated and where any extra oxygen is accommodated within the crystal structure. There are generally two ways to accommodate the extra oxygen in the structure.

Previous studies on 1% Nb-doped STO, reporting that Nb:STO has an electron concentration of $1.63\times10^{20}\,\mathrm{cm}^{-3}$, a resistivity of $1.8\times10^{-3}\,\Omega\cdot\mathrm{cm}$, and a carrier mobility of $33\,\mathrm{cm}^2/(\mathrm{V}\cdot\mathrm{s})$ [56]. Moreover, Nb:STO exhibits exceptional epitaxial growth on the STO substrate. It has clear unit-cell steps and distinct finite-size fringes on top of STO that indicate a crystalline structure [74]. Therefore, these characteristics make Nb:STO a promising candidate to be considered as an additional buffer layer in this study.

1.3.4 Electrodes

Al and Au have been used as the electrodes for the memristor devices in the following structure (Table I). As memristor devices typically consist of a simple metal-insulator-metal (MIM) configuration, where a thin insulating or dielectric layer is positioned between two metallic electrodes. In interface-type resistive switching (RS), the change in resistance arises from modifications in the material properties across the entire interface between the switching medium and the electrode [75]. In the fabricated devices, only a single active switching interface was intentionally designed. This was achieved by employing gold and aluminium as the electrode materials. The gold electrode forms an Ohmic contact with GCMO and does not participate in the switching behaviour, leaving the aluminium-insulator interface as the active switching region. Generally, in its as-fabricated form, a MIM device typically remains in a high-resistance, pristine state. In some cases, an initial "forming" process is necessary, requiring a relatively high voltage to activate resistive switching behaviour. In such structures, electrical conduction is governed by the potential barrier formed at the metal-insulator junction. By applying an external electric field,

this barrier height can be tuned, enabling reversible transitions between different resistance states [76–78]. The selection of electrode materials is a key factor, as it strongly influences the nature of the mobile species responsible for conduction as well as the overall switching mechanism in the device [79–82].

Aluminium electrodes tend to form a thin intermediate oxide layer, which can serve as an oxygen reservoir that facilitates the migration of oxygen ions [83]. In contrast, Kelvin probe measurements performed on the bulk GCMO thin film reveal linear conduction behaviour without any switching characteristics, indicating that the resistive switching is primarily confined to the region near the aluminium interface. At the aluminium contact, a rectifying AlO_x layer is formed, which induces oxygen depletion in the adjacent region of the GCMO layer (Figure 4). The combined influence of this interfacial oxide layer and the oxygen-deficient region results in the formation of an insulating interface. The extent of these interfacial effects can be tuned by an applied electric field, which drives oxygen vacancies to migrate towards or away from the interface depending on the field polarity [24]. This redistribution of oxygen vacancies alters both the AlO_x layer and the oxygen vacancy concentration in the interfacial GCMO region, ultimately giving rise to nonvolatile hysteresis in the current-voltage (I-V) characteristics [23].

2 Methods

2.1 Fabrication methods

The fabrication techniques used in this thesis are the pulsed laser deposition, photolithography and etching, electron beam evaporation, and ultrasonic wire bonding. The fundamentals of each of the techniques employed are covered in the following sections.

2.1.1 Pulsed laser deposition

Pulsed laser deposition (PLD) is a renowned physical vapour deposition (PVD) method for creating high-quality thin films. A high-energy pulsed laser beam is used in the system. It passes through a focusing lens before entering a vacuum chamber and making contact with the target. Continuous crystalline growth is necessary as the laser vaporises the material from the target and produces a plasma plume that spreads away from the target toward the substrate with a flux of material. In most cases, the heated substrate supports appropriate atomic mobility and crystal formation. A flux of atoms and ions that progressively grows at the top of the substrate surface is supplied by the plasma plume as it approaches the heated substrate. Due to the optimal deposition condition, these atoms arranged themselves in an ordered manner, which enables the crystalline epitaxial growth of the thin film that follows the crystal structure of the substrate. The entire deposition process occurs in a vacuum environment, which can prevent any contamination and also allow for control of the deposition atmosphere.

Since it serves to preserve the proper chemical composition (stoichiometry) of the oxide material, oxygen circulation during heating assures that oxygen cannot be lost during the development of the increasing film. Many variables, including substrate temperature, oxygen pressure within the chamber, laser energy density, and laser pulse frequency, can be optimised in the PLD process for various materials. The high-quality growth circumstances and structural quality of the deposited thin films can be controlled by varying these factors. As it mostly dictates the thickness of the final thin film, the number of laser pulses can increase the amount of material deposited, allowing for control over the film thickness [84]. Figure 10 shows the time scale and schematics of the PLD deposition process.

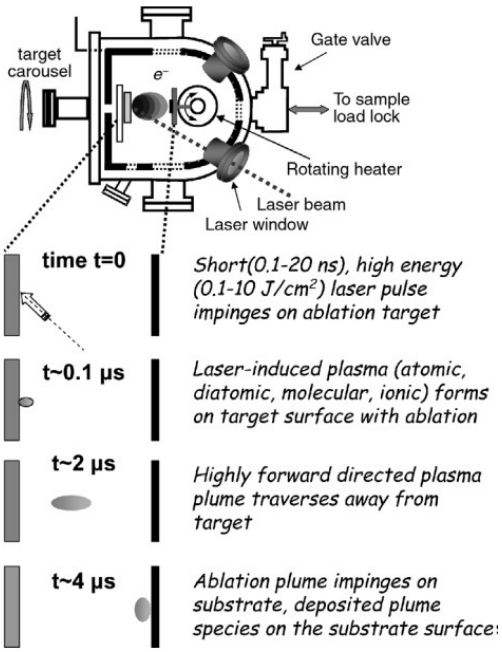


Figure 10. Schematic of a pulsed laser deposition system showing the main components and the time evolution of the plasma plume [84].

2.1.2 Photolithography

In combination, photolithography and etching create a systematic pattern-transfer process that enables the highly controlled creation of micro- and nanoscale objects on the substrate. In this approach, photolithography is first used to form a continuous thin layer and then eliminates the components for the desired design, as opposed to directly depositing on the material only where it is required. On the substrate's surface, any type of pattern can be optically transferred. A homogeneous thin layer of the target material is first deposited on the substrate. PLD or E-beam deposition is commonly utilised for this. The ultimate height or depth of the patterned structures is determined by the thickness of the film, making it important to choose the film thickness carefully. As soon as the film is ready, a thin, smooth layer of either positive or negative photoresist is applied to the film's surface. This is done by spinning a resist droplet at a high rotational speed. The homogeneity of this layer is crucial, as it may have an impact on the resolution of the final pattern. In

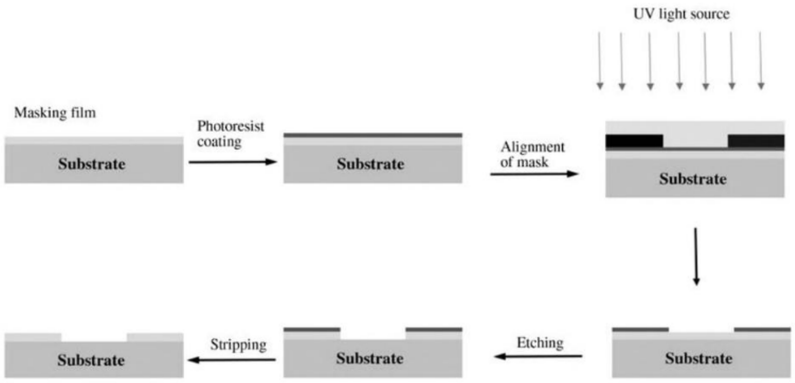


Figure 11. An illustration of the techniques required to create a patterned thin film using photolithography and etching [85].

the exposure step, the pattern is exposed directly on the photoresist surface with a laser writer. The photoresist undergoes some chemical changes as a result of the exposure; also, in a positive exposure, the exposed areas become more soluble in the developer solution while the unexposed ones become less soluble. The patterned resist layer remains on the surface after the sample is treated with a chemical solution including NaOH during the development stage, which eliminates either the exposed or unexposed areas, depending on the kind of photoresist. The portions covered by the photoresist are protected, and it serves as a protective mask for the thin layer underneath. The exposed portion of the thin coating is now selectively removed during the etching process by treating the sample with a chemical etchant in wet etching or in dry etching. Figure 11 shows how the photolithography and etching processes are executed.

The photoresist's predetermined pattern is successfully transferred into the thin film itself as the etchant reacts with the material, dissolving the exposed parts. The clean substrate with the perfectly defined pattern created from the initial thin film material remains after the etching process is finished, and the leftover photoresist is removed [85].

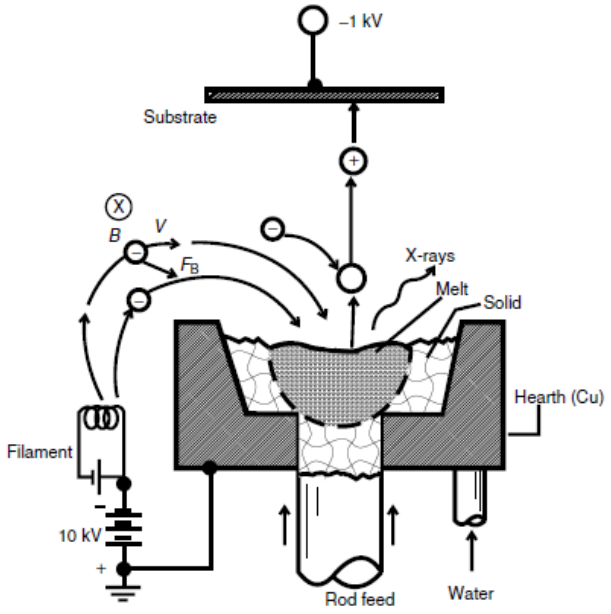


Figure 12. The figure illustrates the configuration of the electron beam system with its main components, electrical circuitry, the trajectory of the evaporated material towards the crucible, and the path of electrons emitted from the filament [86].

2.1.3 Electron beam evaporation

Electron beam evaporation (E-beam) is a Physical Vapor Deposition (PVD) technique which is used to deposit material onto a substrate through the evaporation of the material by heating it with an electron beam. Figure 12 shows the E-beam configuration with the general parts and electrical circuits of the apparatus.

In this process, a high-energy electron beam is generated from a heated filament, which acts as the cathode, usually under an accelerating voltage of around 10 kV. However, these electrons are accelerated and directed towards a target material, which must be placed inside a crucible, and it serves as the anode. As the high-energy electrons hit the surface of the source material, their kinetic energy leads to localised heating and causes the material to either melt or directly evaporate. This vapour of atoms or molecules travels through a high-vacuum environment and condenses onto a substrate positioned in its path, which forms a thin film. Using this high vacuum is essential, as it minimises the collisions between the vapour particles

and residual gas molecules by ensuring a longer mean free path and also reduces contamination. Moreover, the trajectory of the electron beam can be controlled by using an electrical or magnetic field, which allows precise targeting of the source material. So essential parameters such as the deposition rate and film thickness can be finely tuned, which makes the process highly controlled and suitable for high-purity coatings [86].

2.2 Chracterization methods

2.2.1 X-ray diffraction

To identify the crystal structure and phase of any material, the X-ray diffraction technique (XRD) is widely used. The X-ray radiation has a wavelength in the range of the typical distances between atoms; thus, it can be used to probe crystal structure. These techniques are based on the constructive interference of monochromatic X-rays when it diffracted from elements in lattice sites of a periodic crystalline structure [53].

When X-ray photons enter a material, they interact with the surrounding atoms' electrons. Among the various types of interactions, such as absorption and scattering effects, one significant type of interaction comes into focus: elastic (coherent) scattering, also called Rayleigh scattering, in which the X-rays do not lose any energy and maintain their phase relationship with the atomic nuclei. As a result, all of the atoms in the irradiated volume are struck by X-ray photons, and various atoms release scattered waves in all directions [87]. The periodicity of the crystal lattice causes constructive or destructive interference of dispersed radiation, which results in diffraction events that facilitate the study of crystal structure. This makes it possible to examine the crystal structure of materials. The diffracted signal forms the basis of this method's basic principle. William Lawrence Bragg used Bragg's law [88] to explain the condition for the constructive interface. The geometrical

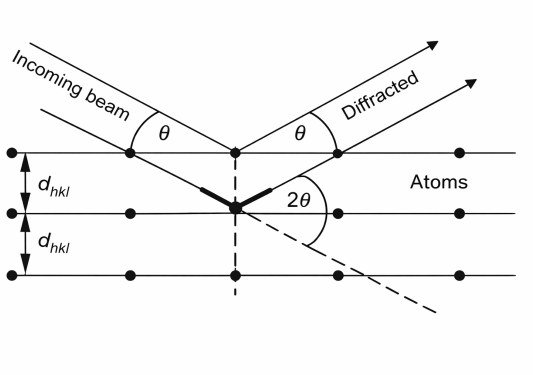


Figure 13. Conditions for diffraction from lattice planes in geometry [87].

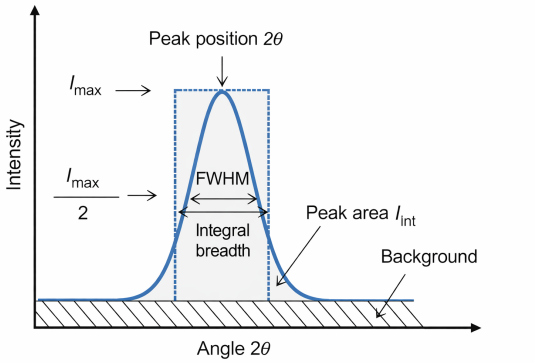


Figure 14. Peak of diffraction and extractable information content [87].

condition for the diffraction and the calculation of Bragg's law are depicted in the accompanying Figure 13, and can be formulated as

$$n\lambda = 2d\sin\theta, \tag{1}$$

where n is a positive integer, d is the distance between the lattice planes and λ and θ are the wavelength and angle of incoming radiation, respectively.

As seen in Figure 14, the XRD diffraction data is often displayed as an intensity distribution as a function of 2θ angle. The maximum peak intensity (I_{max}) and integrated intensity (I_{int}), which are located beneath the peak in the following image, can be estimated once the background has been removed. Additionally, the precise location of the peak and its width can be determined. The full width at half maximum (FWHM), which corresponds to the peak breadth at half of the maximum intensity. This also corresponds to the width of a rectangle of the same maximum

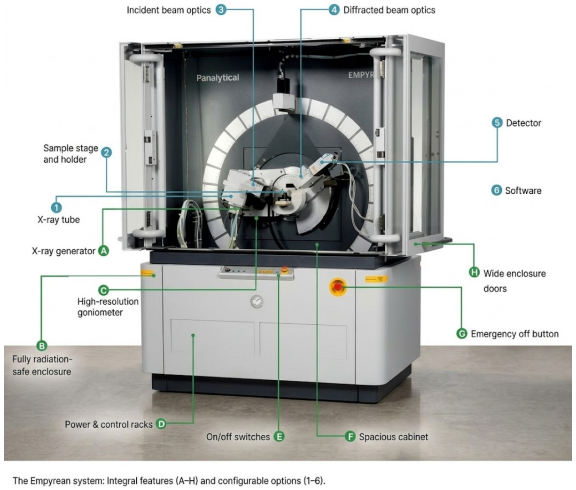


Figure 15. Detailed configuration and architecture of the Philips Empyrean Diffractometer [89].

and integrated intensity as the considered peak, which are two common ways to characterise the peak width. Different peak parameters are used depending on the purpose of measurements [87].

In this study, for thin films, the experimental setup has to be aligned to a particular diffraction angle with respect to the substrate to obtain XRD patterns in different directions, and the XRD measurements of the GCMO thin films were done by a Philips Empyrean diffractometer with a five-axis goniometer (Figure 15). The basic element for these movements is the high-resolution goniometer (c) that permits precise rotation of the sample stage and holder (2). The system was equipped with an X-ray tube (1) and incident beam options (3) $\theta - 2\theta$ in the range of $20° - 110°$ (approximately), which were implemented in the $(00l)$ direction to confirm the phase purity and calculate the c-parameter of the GCMO films. In particular, divergence slits in the incident optics are used to constrain the vertical divergence of the beam in order to avoid over-illuminating the sample at low angles and to keep high angular resolution. The diffracted beam optics (4) comprise antiscatter slits that stop stray radiation and air scattering after the beam interacts with the film. This enhances the peak-to-background ratio, which is important for the quality check of the films

Table III. Details of the X-ray diffraction setup parameters used to obtain XRD measurements for GCMO samples by the Philips Empyrean diffractometer.

Setup Details	**Empyrean diffractometer**
X-ray tube	Empyrean Cu LFF HR 40 kV, 45 mA
Soller slit	0.04 rad × 2
Filter	Bragg HD monochromator
Divergence Slits	1° and 1/2°
Antiscatter Slit	7.5 mm
Mask	4 mm
Goniometer	Five axis
Detector	PIXcel3D

by ω scans in $(00l)$ direction and for the ϕ scan of the (224) peak in $(0hl)$ and (hkl) directions. Finally, the conditioned signal is captured by the PIXcel3D detector (5), all under the control of the system software (6) in a fully radiation-safe enclosure (B). Table III contains more setup information.

2.2.2 Atomic force microscopy

Atomic force microscopy (AFM) is another method used for imaging the surface structures and details of many materials. It's a versatile imaging technique for the study of the surface topography and fine-scale structures of a wide range of materials. AFM uses a sharp probe tip attached to a cantilever to scan the surface of the sample. The imaging process is based on interatomic forces, mainly Van der Waals interactions, between the probe and the sample. These forces can be attractive or repulsive depending on the distance between the tip and surface. To capture these details, the system generally operates in one of three main modes, i.e., contact mode, tapping mode, and non-contact mode. Variations of these caused by the topogra-

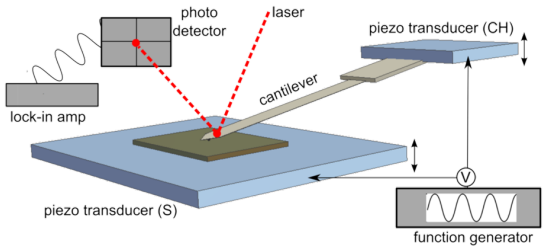


Figure 16. A schematic illustration of the common AFM component [91].

phy and surface features will result in a vertical deflection of the cantilever during scanning. The topographic surface data is collected by a photodetector, which uses a laser that is aimed at the top of the cantilever. The technique was applied to our samples to investigate the roughness and thickness of the material patterns created by different methods. An illustration of the measurement configuration is shown in Figure 16. AFM measurements were performed using the Bruker Innova Atomic Force Microscope in the contact mode [90].

2.2.3 Electrical characterization

First, electrical measurements were performed using a Keithley 2614b source meter and a measurement program written in Python. All the parametric information in this chapter is from the Series 2600B System Source Meter platform User Manual [92]. This instrument is a source-measure unit (also called an SMU), which is an instrument that combines source and measurement capabilities in a single instrument for manufacturers of electronic components and semiconductor devices. This combination reduces synchronisation and connection problems of multiple instrument solutions, making test processes easier. The electrical transport characteristics of memory devices are carefully tested and characterised using a Keithley 2614B source meter (Figure 18). The techniques used in the measuring programme follow common measurements made on memristive devices, such as I-V and R-V curves and resistive state readings. To identify the location of particular devices at particular

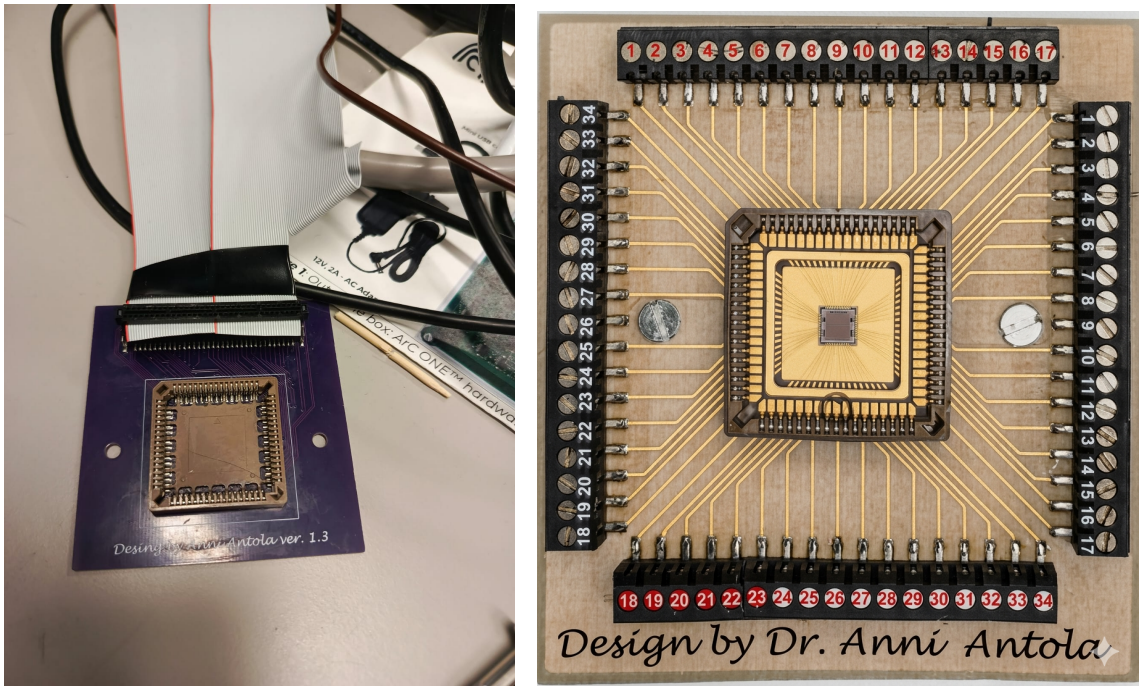


Figure 17. Devices of the samples connected to the numbered red and black lines of the Keithley instrumentation board for identifying device locations at specific addresses.

addresses, the manufactured sample can be attached to red and black lines numbered on the Keithley instrumentation board (Figure 17). The Keithley 2614B uses several crucial parameters that control how I-V measurements are carried out in order to describe the electrical behaviour of the devices with a specific bonding connection. It forces the programmed step of voltage across the device, pauses briefly for the signal to stabilise, and then simultaneously measures the resulting current. By repeating this loop across a defined range, such as a staircase sweep from -4 V to $+4$ V, it plots the device's electrical response point by point. As it sweeps the voltage and measures the current, it internally instantly calculates the resistance for every discrete data point.

Another instrument which is used in this study to investigate the resistive state of the devices in the films is ArC ONE. It is a commercial product of ArC Instruments [93]. The methods implemented in the measurement programme follow the general measurements performed on memristive devices. The fabricated sample's

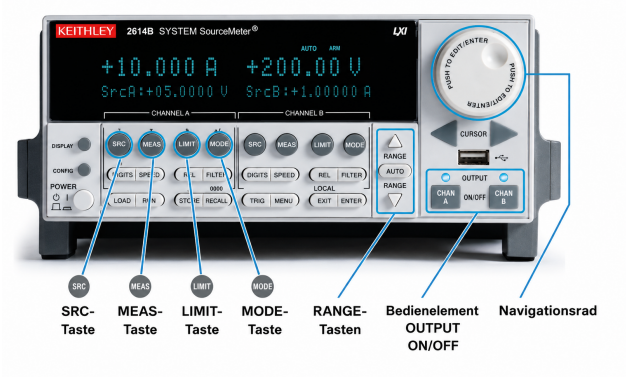


Figure 18. Keithley 2600B Series front panel layout and navigation controls [92].

devices can be connected with word- and bitline header banks on the ArC ONE hardware instrumentation board to communicate with certain devices at specific addresses. ArC ONE offers various modes and scripts for testing and characterising memory devices. The functions are accessed through the functional panels of the user interface shown in Figure 19.

Basic operations, i.e., positive and negative voltage pulse and resistive state read functionalities can be operated manually from Manual Operations. The main read voltage was 0.5 V.

To generate an $I - V$ curve, the system delivers a sequence of voltage pulses with stepped amplitudes that typically trace a triangular envelope to sweep the voltage up and down. Each voltage pulse biases the selected crosspoint, and the resulting current is rapidly measured and plotted against the corresponding applied voltage. For the resistance state, with the read voltage and measured current, it calculates the resistance using Ohm's law. By repeating this process as the write pulse amplitudes step through a full cycle, the system plots the calculated resistance against the preceding write voltage.

Figure 19. Device History, Manual Operations, Toolbar, Data Plot, Advanced Modules, and Crossbar Panel are the functional panels of the ArC ONE user interface [93].

3 Results and discussion

The following sections provide a detailed discussion of the fabrication process and the structural and electrical characterisation results of each fabricated sample.

3.1 Samples

Four thin-film samples have been made with the fabrication process using pulsed laser deposition (PLD), photolithography and electron beam evaporation (E-beam). Although each sample has a unique structure, all four samples have the same active layer GCMO. Table I displays the complete structures of each sample, and the fabrication procedure for these samples will be covered in the sections that follow.

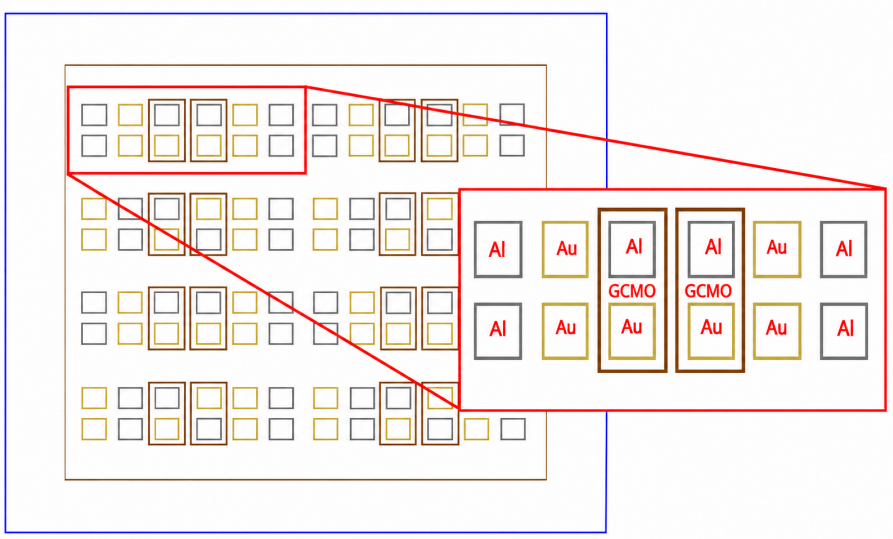


Figure 20. Figure shows the patterning design that was applied to each sample. In the following design, brown holes represent the GCMO layer, grey holes represent Al, and golden holes represent Au. The remaining area defines the substrate/buffer layer.

3.1.1 Fabrication

PLD was used to create four 5×5 mm^2 oxide thin-film samples on top of STO (100) substrates. For four samples each of the two samples, PLD was used to deposit the buffer layers, SRO and Nb:STO thin films on top of the substrates. In every sample, GCMO with Ca-doping $x = 0.8$ was the active layer. Using a laser pulse energy of 68 mJ and a pulse frequency repetition rate 5 Hz, the deposition was done during the PLD process at a substrate with 700° C temperature. To ensure that no oxygen from the sample surface was lost during the heating and cooling process, which involved heating and cooling at a rate of 25.0 K/min, with the oxygen pressure of 0.1 Torr was maintained. The sample was then post-annealed in situ in oxygen at 700° C for 10 minutes at 750 Torr. Each sample had a different number of PLD pulses (Table IV). The table displays the specific methods employed and the parameters associated with the samples. The same photolithography device pattern (direct laser writer) was designed for each sample (Figure 20).

Each sample surface was first cleaned with acetone and dried with nitrogen. A

small amount of spin-coated positive photoresist was applied to the GCMO surface to ensure uniform coating. A gentle bake for 90 s at 115° C was subsequently performed. The Dilase 250 lithography system was used in conjunction with Kloe Design software. The samples were positioned in the centre of the sample chamber. Before loading the intended GCMO pattern, angular correction, stage placement and z-height calibration were performed based on the sample size. To minimise system errors, the photolithography parameters were set to a z-position slightly above visual focus, a velocity of 50 mm/s, and a dimensionless exposure modification factor 20%. The laser writing stage was started after verification and requires the necessary amount of time to finish. The samples were baked once again for 90 s after exposure. The samples were developed by immersing them in a mixture of deionised (DI) water and NaOH. The samples were repeatedly immersed for $45 - 50$ s until the patterns were clearly visible, with each dive lasting $5 - 10$ s. After that, etching was carried out using a solution of diluted GCMO etchant combined with DI water ($1 : 4$ ratio because the etching solution was newly made and quite strong at the time). Each of the samples, repeated 5 s submissions, was immediately followed by a rinse in DI water. After the etching step, the samples were thoroughly washed with acetone to dissolve the resist. Pattering was created using the same techniques for each of the four samples.

The photoresist was similarly applied in order to deposit the Al and Au layers using the lift-off method. In the lift-off, the metal is deposited on top of the photoresist, which is consequently removed.

The final layer of Al and Au pads was fabricated by E-beam. First, the nitrogen supply was turned on to vent the load-lock chamber. For deposition, each sample was placed on the sample holder and taped in place to prevent movement. The sample holder was put into the load-lock chamber, which was then pumped down to a vacuum for approximately twenty minutes. Once the required pressure was reached and

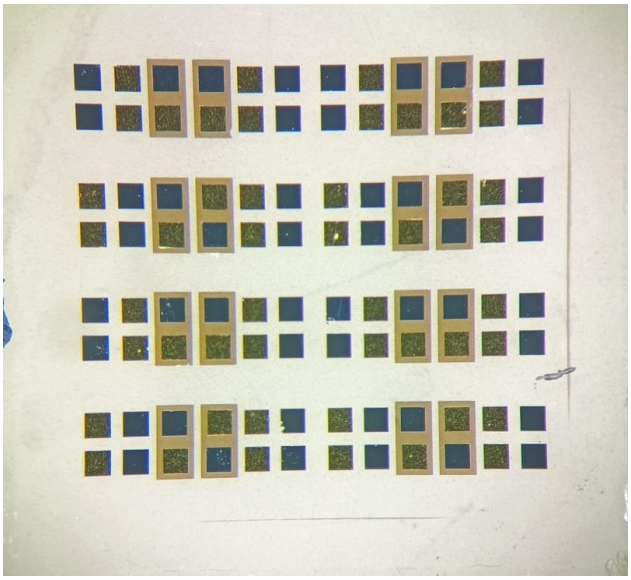


Figure 21. One of the final fabricated samples is shown in the illustration.

verified on the control panel, the sample was transferred to the deposition chamber, and the deposition program was executed. Thereafter, the system was switched to automatic program mode. The gate of the deposition process chamber was opened, and the sample holder was moved by the vertical adjustment mechanism. Once it was confirmed to be in place, the deposition proceeded. The deposition was performed at a chamber pressure of about 1×10^{-9} mbar and a high voltage of 10 kV. When the desired thickness was reached, the deposition was automatically stopped by the system. The aluminium layer was deposited with a thickness of 110 nm, and a rate of 1.5 Å/s, and the gold layer was deposited with a thickness of 200 nm and a rate of 1.0 Å/s. The operation was then terminated as the current slowly went back to its initial value. Once the program had been stopped and the rotation of the holder had stopped, the sample holder was moved back into the load lock chamber. After metal deposition, the samples were removed from the holder, detached, and cleaned with acetone to lift off the resist and remove excess gold and aluminium from unwanted regions. The corresponding Figure 21 displays the final fabricated sample.

Table IV. Fabrication parameter values for GCMO-based thin films

Sample Name	**Film code**	**Buffer layer pulses**	**GCMO**		**Al**		**Au**	
			Pulses	**Dimensions** ($h \times w$) (μ**m**^{2})	**Thickness** (**nm**)	**Dimension** (μ**m**^{2})	**Thickness** (**nm**)	**Dimension** (μ**m**^{2})
STO/GCMO	030226-1	–	1500	600×300	110	200×200	200	200×200
Nb:STO/GCMO	030226-2	–	1500	600×300	110	200×200	200	200×200
STO/SRO/GCMO	290126-1	2100	1500	600×300	110	200×200	200	200×200
STO/Nb:STO/GCMO	030226-4	3500	1500	600×300	110	200×200	200	200×200

3.1.2 Sample set

Four GCMO-based thin films with different substrates or conductive buffer layers were fabricated by PLD, and then patterned, and electrodes (Al and Au) were deposited, followed by photolithography and E-beam to study the effect of different interfacial environments and bottom electrode conductivities on the memristive switching behaviour of GCMO thin films. The height and width of the GCMO layer were $600 \times 300\,\mu\text{m}^2$ for each of the four patterning samples. The Al and Au pads are $200 \times 200\,\mu\text{m}^2$. The part of the Al and Au electrodes is located at the top of the GCMO, similar to the patterning design, and the gap between the pad's edge and the GCMO edge was $50\,\mu$m. Some of the Al and Au pads are on the substrate or buffer layer, so the distance between the GCMO edge and the electrodes on the substrate or buffer layer was $50\,\mu$m. From the patterning design, it was seen that there are two rows of electrodes placed side by side with a distance of $50\,\mu$m. The fabrication parametric values for each layer utilised to create the entire thin film are displayed in the following Table IV.

The electrodes were placed on the top of the GCMO and on the substrate/buffer layer in order to differentiate among the various conduction mechanisms. The top-to-top (in-plane) structure, which was measured between two pads on top of the GCMO, was designed to study the lateral resistance and switching behaviour of the active layer itself, and the top-to-bottom (out-of-plane) structure, where the electrodes are placed on top of the conductive buffer layer (like SRO/Nb:STO), was

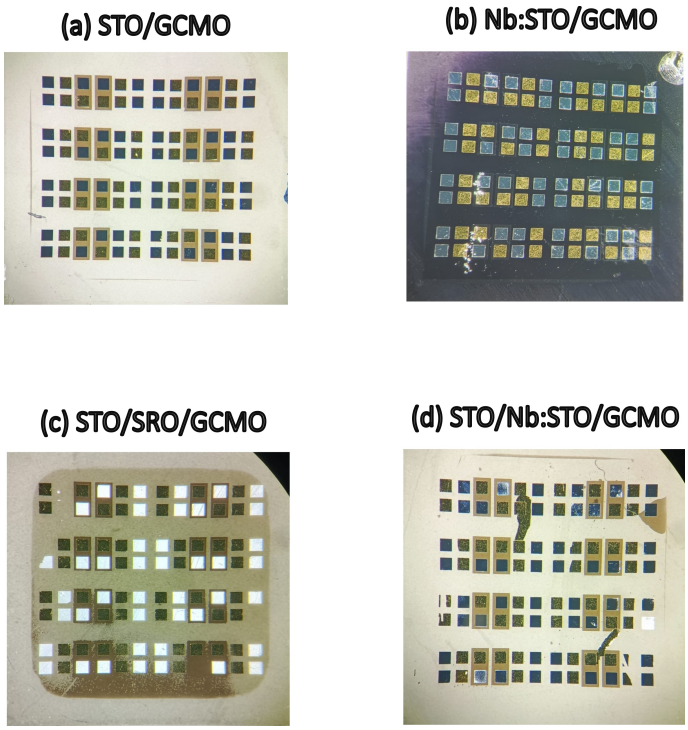


Figure 22. Each of the patterned samples is displayed in the following figure, corresponding to the pattern design.

designed to measure the vertical transport through the GCMO/SRO interface.

Sample (STO/GCMO) is the baseline with GCMO directly deposited on insulating STO, while the other three samples were modifications like the following: Sample (STO/SRO/GCMO) and sample (STO/Nb:STO/GCMO) use SRO and Nb:STO buffer layers as intermediate electrodes or interface-tuning layers, respectively, while sample (Nb:STO/GCMO) uses a Nb-doped STO substrate as a conductive foundation. While there are some errors that have been observed in the (STO/SRO/GCMO) sample, as seen in the figure of this sample, it is clear that the Al pads look somewhat whiter than usual compared to other samples. Later, it was predicted that it might be because some of the Al had been oxidised, and the reason is unknown; further investigation will be needed in the future regarding this issue. Figure 22 shows the fabricated samples according to the patterned design (Figure 20). Al and Au were used as top-contact materials in order to allow comparison between symmetric and asymmetric electrode configurations.

Table V. The structural results extracted from XRD data.

Sample	$2\theta(004)$	$\Delta\theta(004)$	$\Delta\omega(004)$	$\Delta\phi(204)$	$2\theta(204)$	$2\theta(224)$	a	b	c	Intensity	V_{cell}
STO/GCMO	48.71	0.24	0.38	1.81	60.51	70.00	5.32	5.62	7.47	67252.4	223.45
Nb.STO/GCMO	48.67	0.23	0.39	1.48	60.51	71.00	5.31	5.34	7.48	50353.3	211.98
STO/SRO/GCMO	48.83	0.24	0.31	1.56	60.62	71.11	5.32	5.33	7.45	49079.3	211.53
STO/Nb.STO/GCMO	48.88	0.24	0.41	3.33	60.78	71.24	5.29	5.34	7.45	43429.2	210.37

3.2 Structural properties of films

3.2.1 X-ray diffraction analysis

The crystallographic characterisation of each thin film was done by XRD measurement. The lattice parameter in the out-of-plane direction c and the identification of the possible impurity phases were determined from XRD $\theta - 2\theta$ and ω scans in $(00l)$ direction. The $\theta - 2\theta$ measurements were performed in (204) and (224) directions to determine the lattice parameters of in-plane directions a and b. Furthermore, 2-dimensional ϕ-2θ scans of (224) peaks were performed to study the twin and grain boundaries. Table V represents all the values. The sample was aligned, and the instrument parameters were set to (**voltage**= 45 kV and 40 mA before the XRD measurements. Table V shows the structural results from the XRD measurements.

The 2θ scans of all films showed only GCMO $(00l)$ and substrate peaks. The GCMO-related peak (004) were observed near $2\theta \approx 48.7°$–$48.9°$ for all samples. Comparing Table V data with Figure 23, the measured 2θ values for (004) peak positions were for the first sample STO/GCMO: 48.71°, for the second sample, Nb:STO: 48.67°, for the third sample STO/SRO/GCMO: 48.83°, and for the fourth sample STO/Nb:STO/GCMO: 48.88°. The XRD patterns of all four structures show a dominant GCMO peak in the same range corresponding to the $(00l)$ reflections. The proximity of these 2θ values indicates that the GCMO thin films have a highly consistent crystal structure, even with the underlying bottom electrode or buffer layer (SRO and Nb:STO).

The out-of-plane structural properties of the sample were also plotted as intensity

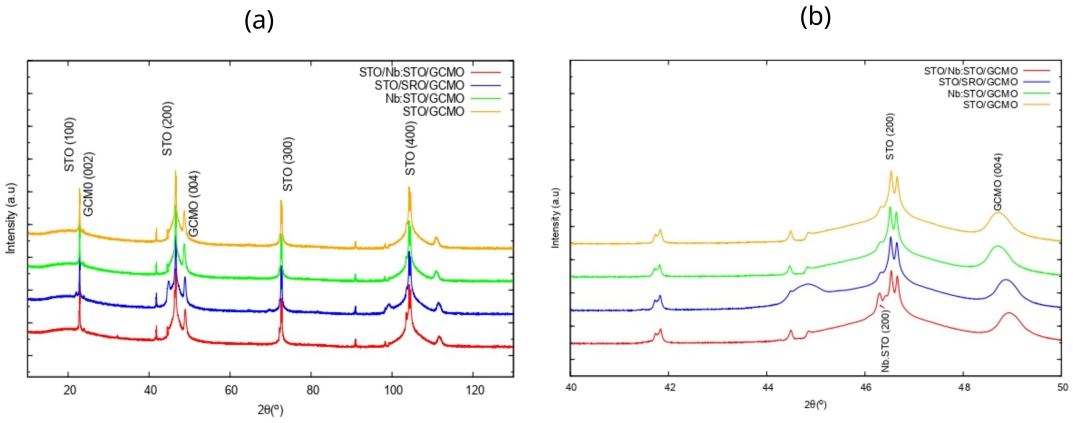


Figure 23. The figure shows 2θ XRD measurements in $(00l)$ direction for GCMO thin films deposited on substrates. (a) shows the GCMO peaks for all samples; however, in (b), in a close-up view, the Nb:STO peak (200) has been found, and it's been identified as the basis of the following analytical studies [94, 95].

against ω angle, which is shown in Figure 24. This is also known as a rocking curve. The widths of the curve $\Delta\omega(004)$ are between 0.31° and 0.41°, demonstrating a comparable out-of-plane crystalline quality across the samples.The smallest full width at half maximum ($\Delta\omega$) is observed for the STO/SRO/GCMO sample. This narrow ω peak indicates a very small mosaic spread, i.e., nearly all microscopic crystalline domains are perfectly aligned with their lattice planes parallel to the substrate surface normal. Therefore, these domains fulfill the Bragg condition at almost the same incident angle in the course of the sample till, which implies a better out-of-plane structural alignment and good crystalline quality.

The texture of the (204) reflection for each structure in Figure 25 shows a clear four-fold symmetry, with four distinct spots of high intensity separated exactly 90° at the outer edge of the plot. This particular spot pattern confirms that the GCMO film axes are rigidly locked in three dimensions and sets the epitaxial growth. The spots are placed at a fixed radial distance from the centre, fixing the vertical axis and providing a uniform out-of-plane orientation. At the same time, the horizontal axis is locked since they are separated by a strict 90° angles around the circle (az-

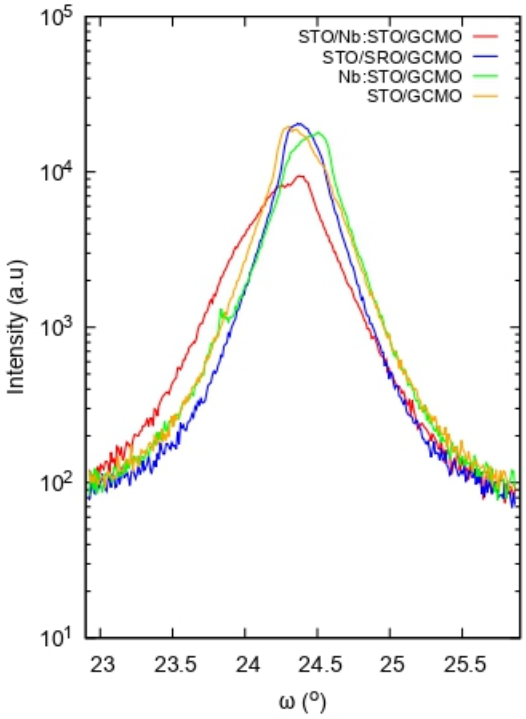


Figure 24. The ω curve shows the intensity (a.u.) as a function of the incident angle ω (degrees).

imuthal angle ϕ), confirming a well-defined in-plane alignment with the substrate grid. Furthermore, the intense concentration at the centre corresponds to the specular out-of-plane $(00l)$ reflections, suggesting highly parallel stacking of crystal planes, while the weaker inner spots correspond to the underlying substrate shining through the thin film. Texture measurements gave $\Delta\phi(204)$ values between 1.48° and 3.33° (Table V. The highest $\Delta\phi(204)$ was observed for the STO/Nb:STO/GCMO structure. The poles for this specific sample appear visually somewhat broader and less pinpoint-sharp than the other samples, confirming a wider spread in the in-plane crystallographic orientation. The lattice parameters were extracted from the asymmetric reflections, resulting in unit-cell volumes of around 210–223 Å^3 (Table V). To understand the strain in the fabricated GCMO films, their unit cell volumes compare to the bulk value for nominal GCMO ($x = 0.8$) (Table V), which is 211.67 Å^3 [53]. The STO/GCMO film has the largest volume ($V = 223.45$ Å^3), meaning its

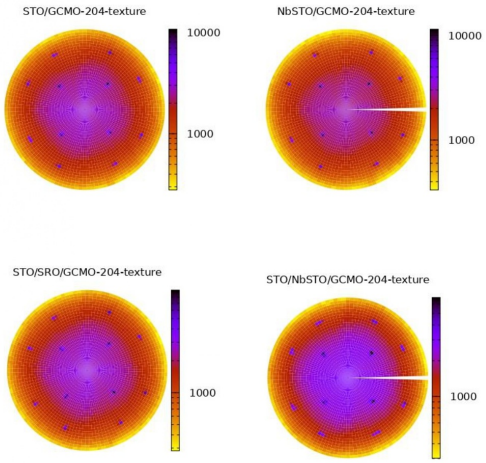


Figure 25. This figure illustrates the (204) reflection's XRD texture (pole) figures for GCMO thin films grown on the substrates: STO/GCMO, Nb:STO/GCMO, STO/SRO/GCMO, and STO/Nb:STO/GCMO.

crystal structure is the most relaxed. On the other hand, the buffered samples have smaller volumes than the bulk material, which shows they are under compression.

3.2.2 AFM roughness

For two different locations, measurements have been made of the thickness and roughness of the GCMO layer as well as the roughness of the substrate (STO and Nb:STO) and buffer layer (SRO and Nb:STO). The scanning ranges for the roughness were 20 μm and 5 μm with the scanning rates 0.50 Hz (for 20 μm) and 1 Hz (for 5 μm). For the thickness, the scanning range was 50 μm, and the scan rate was 0.50 Hz. In this case, a scan resolution of 256 $\times$ 256 pixels was used, recording the Height-Forward, Height-Backwards, Height sensor-Forward, and Height sensor-Backwards channels. For analytical measurement, the Height sensor-Forward values were recorded for each data set. Although the GCMO layer's thickness and roughness were measured at two different locations for each sample, the results showed little variation between these two places; however, the substrate and buffer layer

Table VI. Surface roughness and thickness values of the GCMO thin films, substrates, and buffer layers obtained from a 5 μm scan area.

Sample	Roughness (nm)		GCMO Thickness (nm)
	GCMO	Substrate and buffer	Average value
	R_q	R_q	
030226-1(STO/GCMO)	0.67	0.66	55.61
030226-2(Nb:STO/GCMO)	2.23	0.61	57.86
290126-1(STO/SRO/GCMO)	0.89	0.91	55.19
040226-4(STO/Nb:STO/GCMO)	1.51	0.71	54.68

measurements for the STO/SRO/GCMO sample showed a significant difference. Thus, the roughness of two additional places has been measured for the third sample (290126-1). Although the primary cause is yet unknown, this discrepancy may be the result of a small fabrication process error. Among two locations, the values in the scanning range at 5 μm shows the smaller values; thus, Table VI provides the optimum thickness and roughness values that have been chosen from the AFM measurement data.

The surface roughness of the thin films was measured using the root mean square (RMS) roughness (R_q) with (nm) units. This value calculates the standard deviation of the surface height, making it a reliable way to check how uniform the surface is and how much it bumps up or down. As shown in the table VI, the R_q values for the GCMO layers across the four samples range from 0.67 nm to 2.23 nm. As these values are only between a fraction of a nanometre and a few nanometres deep, it indicates that the film surfaces are exceptionally flat and uniform. The surfaces remain very flat overall, even though the GCMO layer on the Nb:STO/GCMO sample is slightly rougher than the others. The AFM 2D image in Figure 26 shows some bright spots on the GCMO surface for the (Nb:STO/GCMO) sample, which could be contamination developed during the fabrication process. These bright spots have been observed in the other two samples, except for the first sample

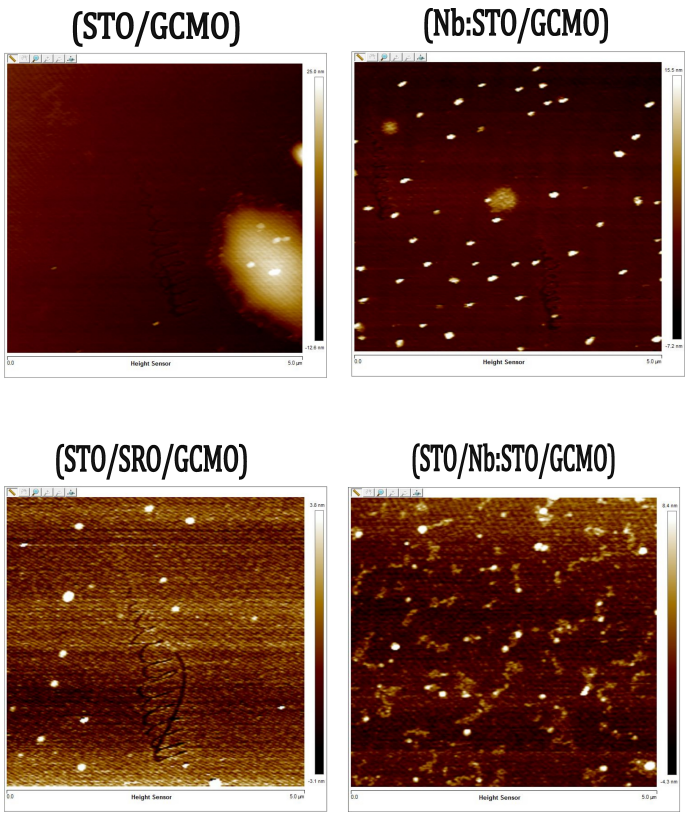


Figure 26. AFM measurement for the roughness of the GCMO layer for each sample.

(STO/GCMO); for this reason, the roughness values of these three samples appear slightly larger than those of the (STO/GCMO) sample.

For comparison, the roughness values of the underlying substrate and buffer layers for all samples are very close to each other, ranging from 0.66 nm to 0.91 nm (Table VI). These small difference values, combined with the low roughness of the GCMO layer, show that the highly uniform substrate and buffer layers provided an excellent, flat base for the GCMO layer to grow properly on top. The two-dimensional surface shapes of the substrate and buffer layers are shown in figure 27.

The average thickness of the GCMO layer is in the range of 55.61 nm to 57.86 nm. Table VI shows that there is not much change in the GCMO thickness among the samples. The (Nb:STO/GCMO) sample has a slightly higher thickness value than the other samples, which may be due to its higher roughness.

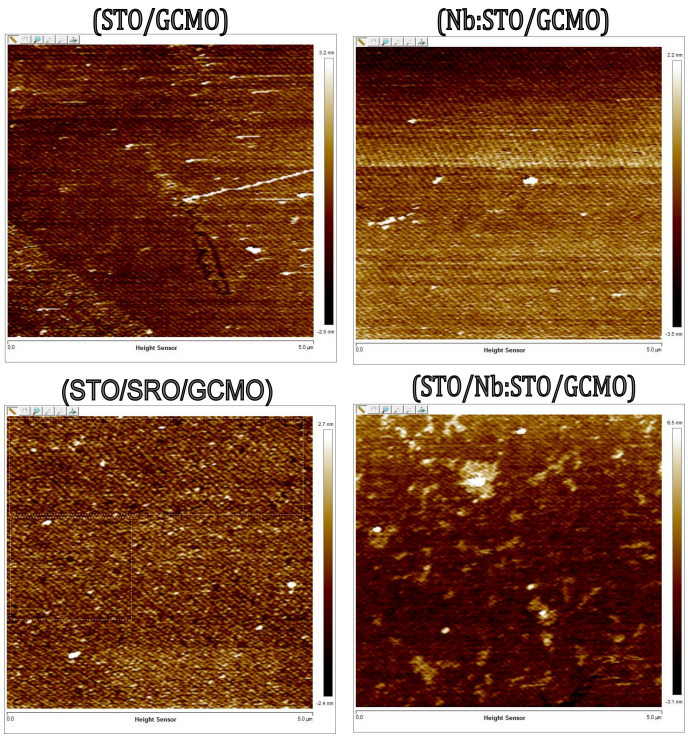


Figure 27. AFM measurement for the roughness of the substrate and buffer layer for each sample.

3.3 Electrical properties

Electrical properties were measured using Keithley and ArC ONE measurement systems. Current-voltage measurements were performed at room temperature for different contact locations. For the initial measurements, symmetric voltage sweeps from $-4\,\mathrm{V}$ to $+4\,\mathrm{V}$ were applied to these two different measuring instruments. Ten consecutive voltage sweeps were recorded to evaluate the repeatability and possible resistive-switching behaviour of each measured device. Several electrode and layer configurations, including Al/Al and Au/Au reference contacts, Al/Au asymmetric top-electrode contacts, and Au/GCMO/Al and Al/GCMO/Al device structures, have been compared. Since Keithley appears to have an issue with overly conductive connections, the same device connections were measured using both the ArC ONE and Keithley setups for comparison. Among the several connections that were measured by both systems, two common connections (Al and Au at the top of GCMO

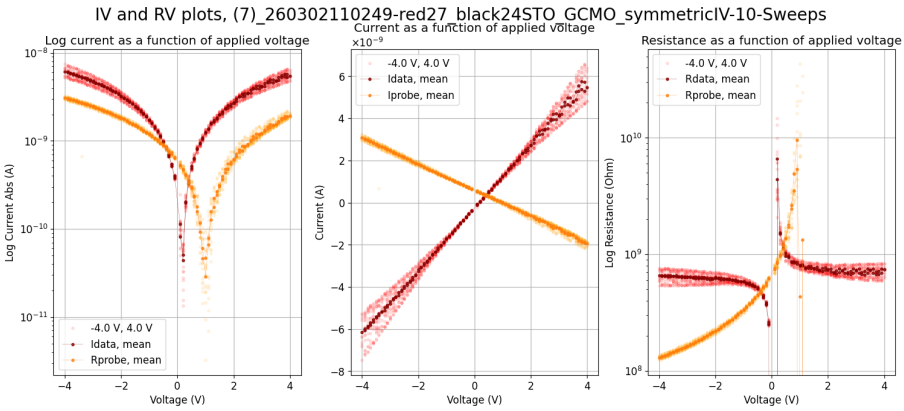
and at the top of the substrate/buffer layer) have been described in detail in the following sections, with the reference plots for each sample.

3.3.1 STO/GCMO

Sample devices of STO/GCMO thin film with a symmetric top-top GCMO contact configuration with Al and Au electrodes were prepared, which exhibit a highly symmetric, non-linear rectification around 0 V. From Figure 28 (a), initial Keithley measurements showed an extremely insulating state, indicating that either the film broke during wire-bonding or the bond failed to fully penetrate a highly resistive aluminium oxide (AlO_x) surface layer. In Figure 28 (b), the ArC ONE system captures a clearer response where voltage sweeps away from 0 V the electrical junctions to turn on, resulting in an exponential current rise. However, over ten consecutive voltage cycles, the current at ± 4 V steadily increased while the peak resistance at 0 V dropped from approximately 7 kΩ to under 2 kΩ. This permanent drop signifies a cumulative failure or uncontrolled electroforming, likely caused by oxygen vacancies that permanently drifted the device from a high-resistance state to a low-resistance state.

In comparison, Al and Au electrodes contacted on top of the bare STO substrate behave purely as a highly resistive, passive insulator with no resistance switching capabilities. From Figure 29 (a) and (b), it maintained a tiny current scale ($\sim 10^{-9}$ A to $\sim 10^{-8}$ A) and a massive resistance scale (10^8 Ω to 10^{12} Ω). While the true film data (I_{data}) showed a typical non-linear response passing perfectly through the origin, the probe measurement (I_{probe}) suffered from a noticeable shift, with its zero-current point displaced to +1.0 V and causing a massive resistance spike near 10^{12} Ω. This artefact occurs because the real current passing through such a highly insulating layer is very small. Ultimately, as the substrate's resistance remained at a flat, massive background level without any hysteresis loops, it confirmed that the bare

(a)



(b)

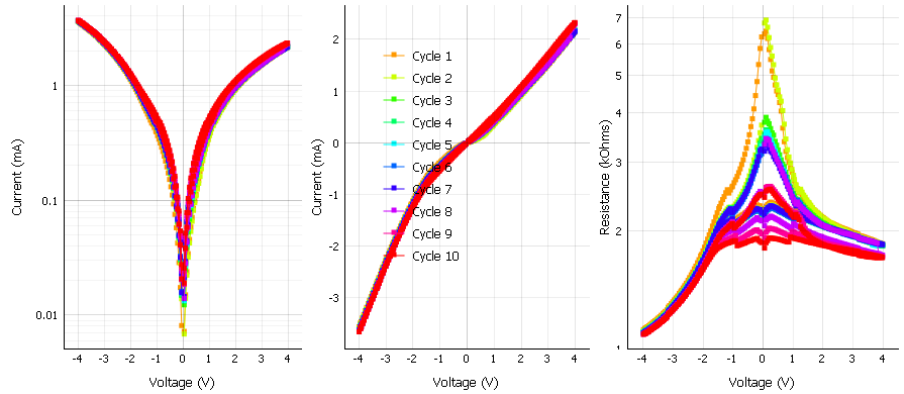


Figure 28. Transport measurement of an Al/GCMO/Au device fabricated on an STO substrate.(a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing a low current and the initial high-resistance-state behaviour. (b) Evolution of the I-V and R-V characteristics during ten consecutive sweeps measured with the ArC ONE system, demonstrating a permanent, irreversible degradation of the interface resistance barrier.

substrate does not switch and acts only as a passive dielectric.

3.3.2 Nb:STO/GCMO

Both configurations showed repeatable results across 10 consecutive cycles. However, the absence of an open hysteresis loop due to the complete overlap of the forward and reverse lines resulted in no active resistive switching between low and high resistance states in either device connection. In Figure 30 (a) and Figure 31 (a),

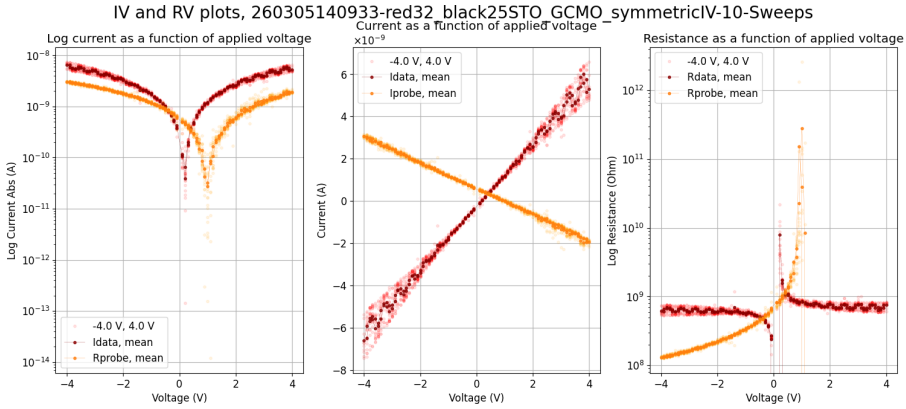


Figure 29. Transport measurement of an Al/Au device fabricated on an STO substrate. The Keithley results indicate that the bare STO substrate is electrically inactive, with no effect on the transport behaviour and device stability.

both device connection measured results from the Keithley measurement showed identical behaviour. The current immediately jumped to the safety compliance limit of the instrument, 4.0×10^{-2} A, limiting the measured voltage to near zero. The mechanical stress of the wire-bonding process physically penetrated the electrode layer and created a direct metal-to-metal bypass, forcing the electricity to travel through a wide highway instead of the active material, resulting in a permanent short circuit.

The ArC ONE system was able to overcome this limitation and show, in Figure 30 (b) and Figure 31 (b), fundamentally different electrical behaviours for each of the device connections. In the electrodes on top of the GCMO device, $I-V$ measurement (Figure 30 (b)), the system recorded low current in the nanoampere range and a maximum value of about 300 nA. It showed rectifying, unidirectional conduction, with the current being nearly zero at negative bias and flowing only at positive bias, causing the resistance to decrease to the 1 MΩ range with increasing voltage. In contrast, connection on top of the bare Nb:STO substrate exhibited symmetric, non-linear conduction, i.e., current could flow equally well in both positive and negative directions (Figure 31 (b)). Since Nb:STO is a highly conductive, doped semiconductor substrate, its current peaked at 6 mA, which is $10,000$ times higher

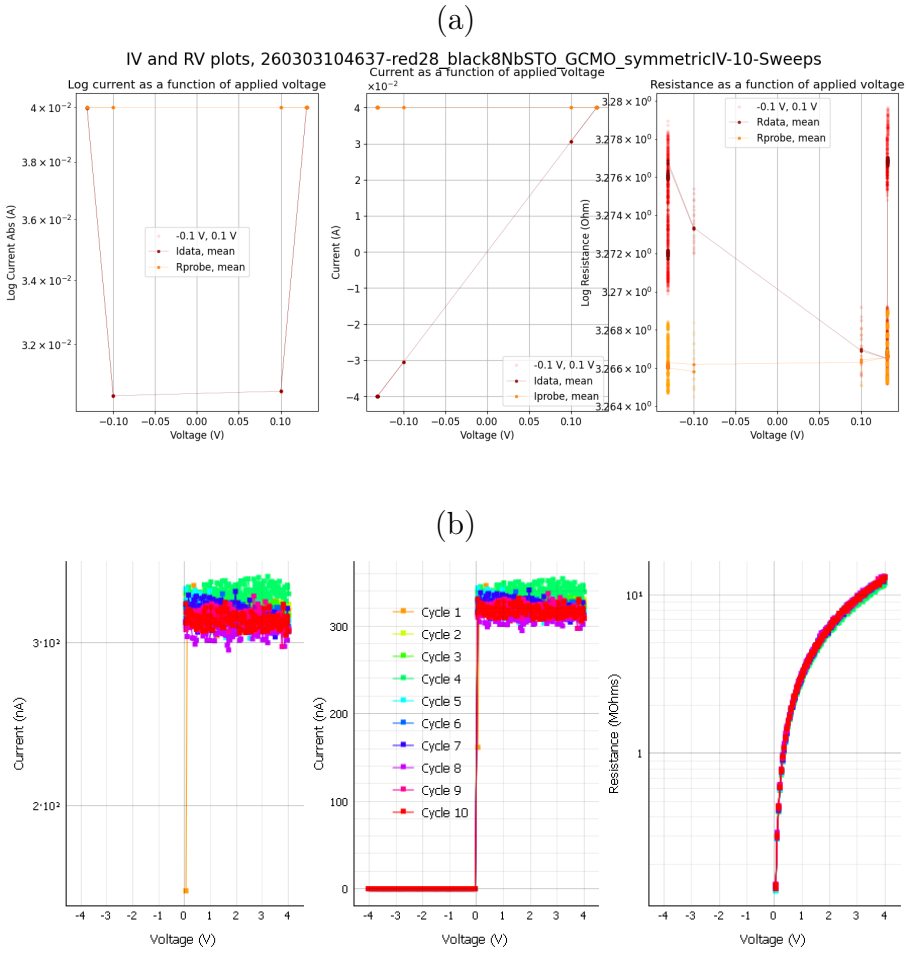


Figure 30. Transport measurement of an Al/GCMO/Au device fabricated on an Nb:STO substrate. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing a low current and the initial high-resistance-state behaviour under low voltage. (b) Evolution of the I-V and R-V characteristics during ten consecutive sweeps measured with the ArC ONE system, indicating a permanent electrical breakdown that results in a fixed non-switching rectifying state with highly reproducible characteristics across all cycles.

than the GCMO sample. Its resistance was a sharp V-shape on a logarithmic scale, with a maximum at 0 V and dropping rapidly from 1 kΩ to less than 10 Ω at higher biases. These results indicate that the Keithley measurements were limited only by the instrument due to the physical shot circuit. The ArC ONE data gave evidence that the bare Nb:STO substrate behaves as a very conductive non-switching baseline, while the GCMO layer presents rectifying properties.

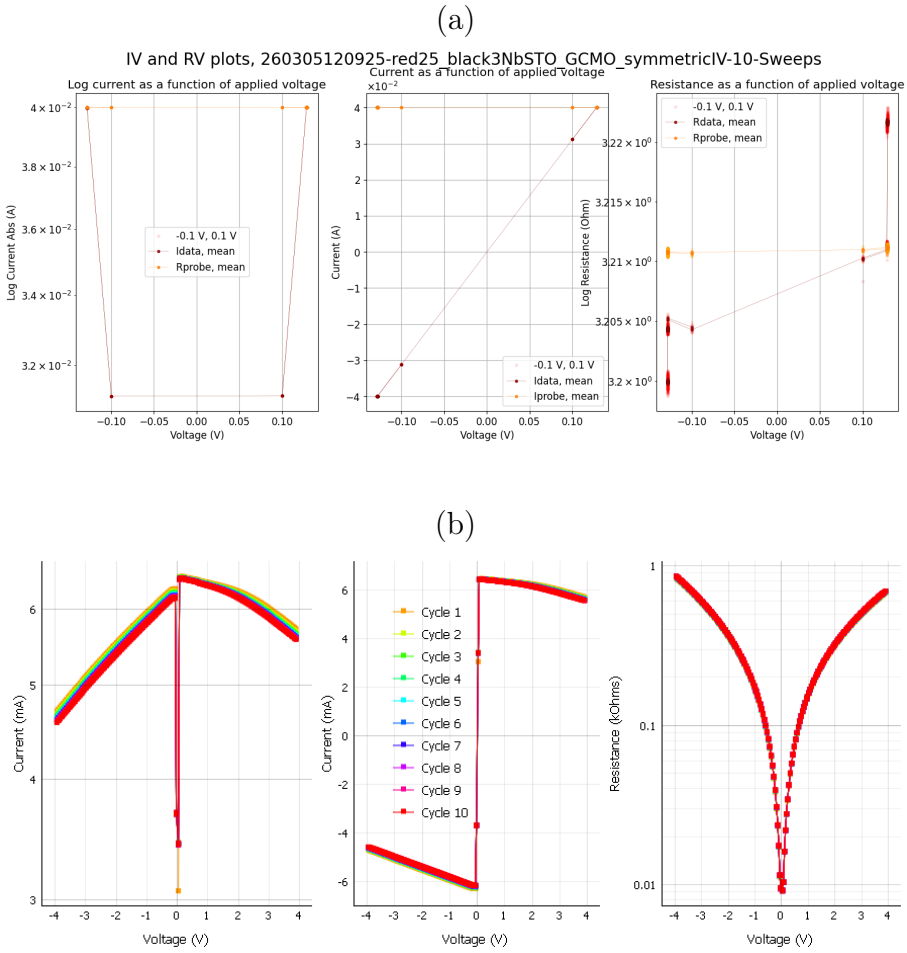


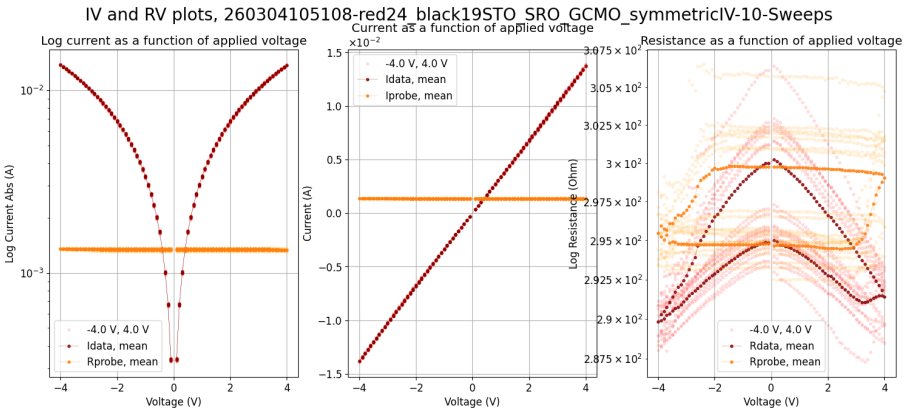
Figure 31. Transport measurement of an Al/Au device fabricated on an Nb:STO substrate. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing instrument-limited short-circuiting. (b) Evolution of the I–V and R–V characteristics during ten consecutive sweeps measured with the ArC ONE system, demonstrating highly repeatable, non-hysteretic bulk semiconductor conduction. The results indicate that the Nb:STO substrate significantly affects the transport behaviour and stability of the device.

3.3.3 STO/SRO/GCMO

The devices in this film exhibit non-linear electrical behaviour when the electrodes on top of the GCMO layer are connected.

For the Keithley measurement, shown in Figure 32 (a), the current is zero in the middle and increases exponentially in both directions, reaching a maximum current of $\approx \pm 1.4 \times 10^{-2}$ A at the voltage limits. This makes the resistance form a smooth

(a)



(b)

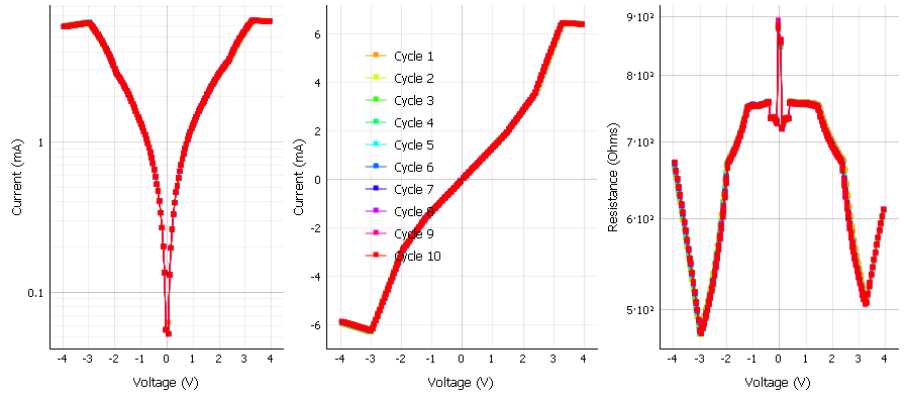
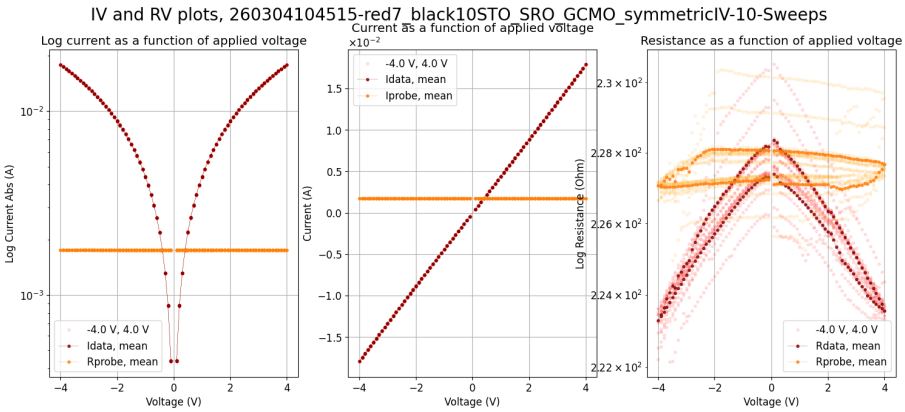


Figure 32. Transport measurement of an Al/GCMO/Au device fabricated on an SRO bottom electrode. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing a smooth, natural curve where current increases with voltage and resistance forms a normal hill shape. (b) Evolution of the I–V and R–V characteristics during ten consecutive sweeps measured with the ArC ONE system, indicating a flattened current at high voltage due to instrument limits, which creates an unnatural M-shaped resistance curve.

parabola with a maximum near $\approx 3.0 \times 10^2\,\Omega$ around 0 V. This behaviour is similar to the ArC ONE measurement shown in Figure 32 (b), at lower voltages, but the current levels out to a plateau at ± 6.2 mA at voltages greater than ± 3 V. This seems to be an effect of the current saturation due to an instrumental limitation of the ArC ONE instrument, as it approaches its internal safety compliance limit. Then the current is forcefully flattened, and the voltage continues rising, giving

(a)



(b)

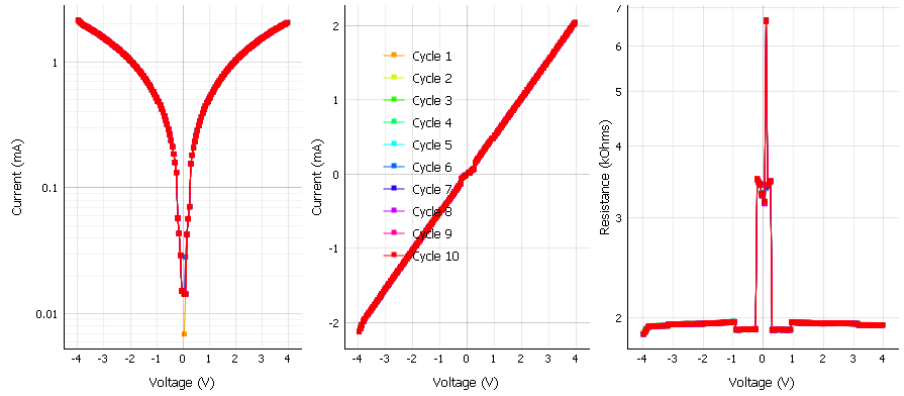


Figure 33. Transport measurements of an Al/Au device fabricated on a bottom electrode SRO. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing completely linear and symmetric behaviour with a low, flat resistance baseline due to the direct contact with the highly conductive metallic layer. (b) Evolution of the I–V and R–V characteristics during ten consecutive sweeps measured with the ArC ONE system, showing a constant resistance and a stable, linear current response across all cycles. The results indicate that direct contact with the conductive bottom electrode SRO establishes entirely linear transport behaviour.

a distorted "M-shaped" profile of the calculated resistance peaking at the voltage extremes.

In contrast, when electrodes are directly connected to the highly conductive metallic SRO layer, the electrical behaviour becomes entirely linear and symmetric. In the Keithley measurements shown in Figure 33 (a), without the resistive

GCMO layer, the maximum current is slightly higher $\pm 1.8 \times 10^{-2}$ A and shows a lower, mostly flat resistance baseline of about $\approx 2.28 \times 10^{2}\,\Omega$. For the ArC ONE measurements (Figure 33 (b)), it seems that the linear behaviour keeps the current low enough that it never triggers the internal compliance limit. Consequently, the current rises steadily without flattening, and the resistance remains completely constant at approximately 1.9 kΩ across the entire voltage range, except for a brief measurement spike at exactly 0 V.

In summary, the observations confirm that under these conditions, none of the devices exhibits non-volatile resistive switching, as the overlapping forward and backward traces show no permanent memory state changes.

3.3.4 STO/Nb:STO/GCMO

Keithley measurements shown in Figure 34 (a), at the first device connection (Al/Au on top of GCMO), show current peaks between 4.5 μA at ± 4 V range, and resistance peaks at $1.05 \times 10^{6}\ \Omega$ at zero bias. This indicates that the current is flowing symmetrically for positive and negative voltages, i.e., it is like a normal steady diode without memory or switching loops. However, when the same connection is tested with the ArC ONE instrument, the behaviour will be totally different and extremely fluctuating, as shown in Figure 34 (b). Negative voltage induces sharp jumps at -0.8 V, forcing the current past -570 μA at -4 V. This smooth curve and negative voltage cause sharp, staircase-like jumps that indicate the material is suffering permanent, messy electrical damage known as dielectric breakdown. Following this, when a positive voltage is applied, the current is still suppressed (10^{-7} A to 10^{-4} A), but the resistance fluctuates rapidly between 0.1 GΩ and 10 GΩ, making the connection highly unstable and noisy, implying that it cannot be used for reliable memory switching.

The Keithley measurements are directly across the Nb:STO buffer layer, as shown

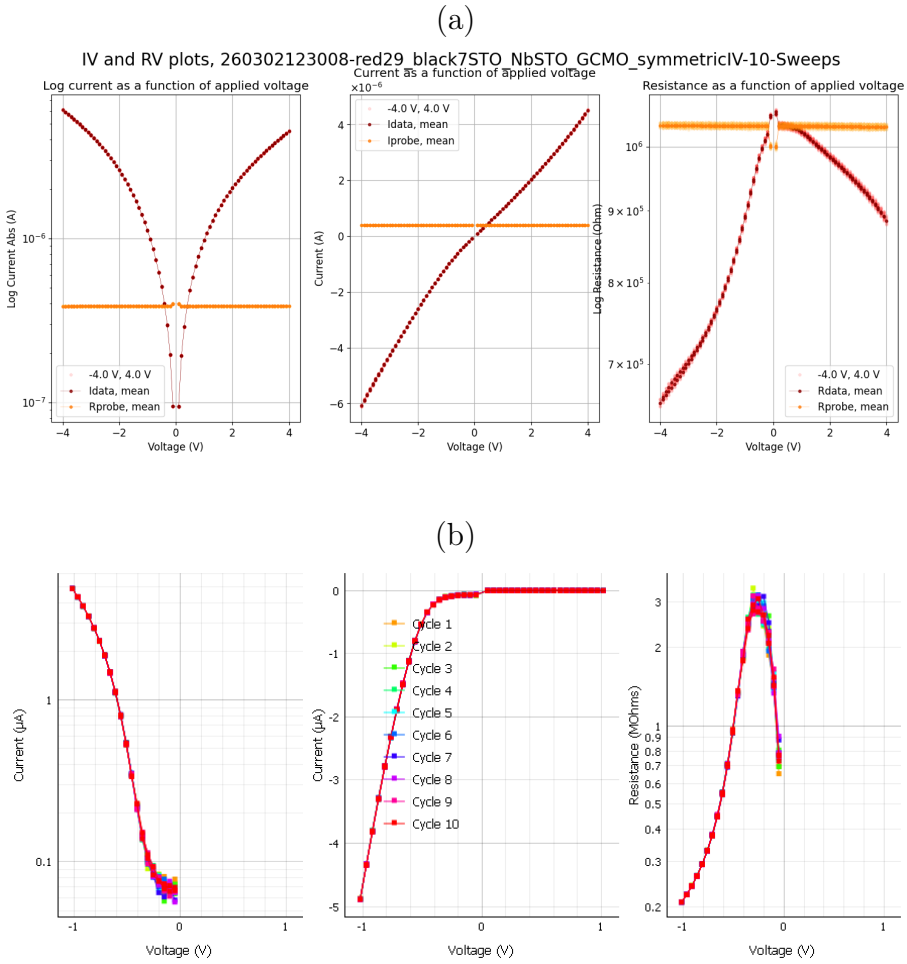
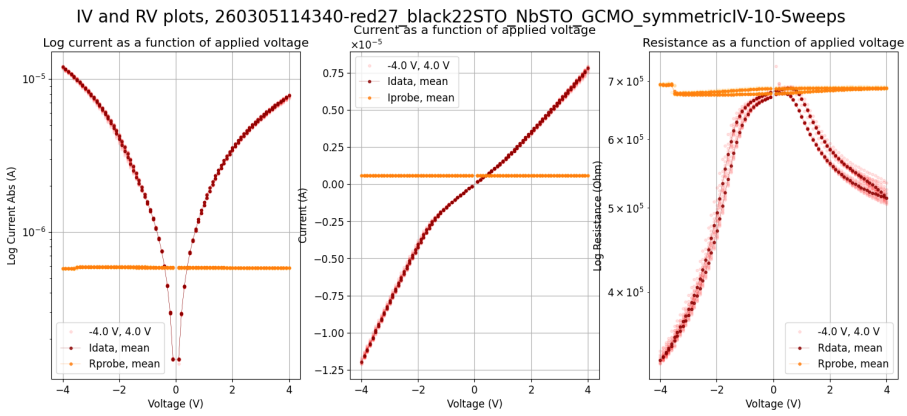


Figure 34. Transport measurements of an Al/GCMO/Au device fabricated on a bottom electrode Nb:STO. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing stable, symmetric diode-like behaviour. (b) Evolution of the I–V and R–V characteristics during ten consecutive sweeps measured with the ArC ONE system, demonstrating highly unstable, fluctuating results characterised by permanent dielectric breakdown.

in Figure 35(a), showing that the material has stable, slightly lopsided diode behaviour on average. The maximum current is 12 μA for -4 V bias and 18 μA for $+4$ V bias. The maximum resistance is 6.8×10^5 Ω near zero bias, falling to 3.5×10^5 Ω at -4 V and 5×10^5 Ω at $+4$ V. For ArC ONE measurements shown in Figure 35 (b), a permanent electrical conditioning step (electroforming) takes place in the first cycle, between individual fast-test cycles. The current jumps from 1.5 μA to 3.5 μA at precisely $+3$ V. The resistance falls from 2 MΩ to 0.6 MΩ.

(a)



(b)

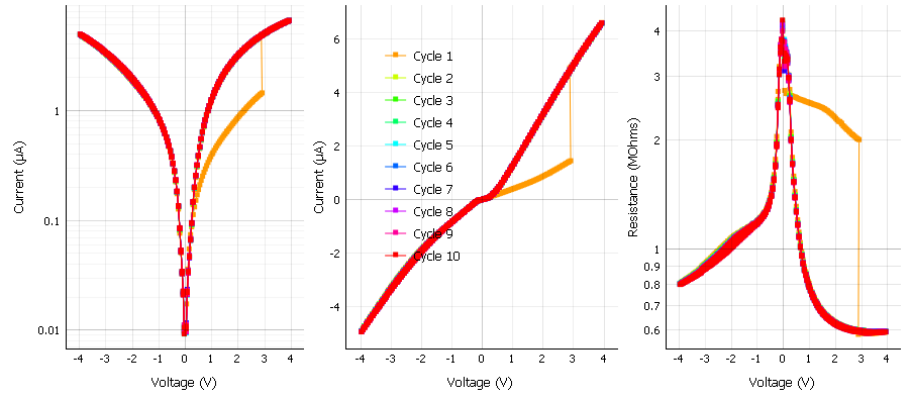


Figure 35. Transport measurements of an Al/Au device fabricated on a bottom electrode Nb:STO. (a) Current-voltage characteristics measured using a Keithley source meter after wire bonding, showing a stable, intrinsically rectifying junction with asymmetric diode behaviour. (b) Evolution of the I–V and R–V characteristics during ten consecutive sweeps measured with the ArC ONE system, indicating a permanent, first-cycle electroforming step followed by a fixed, non-switching diode path. The results indicate that the bottom electrode Nb:STO dictates a fixed, rectifying junction rather than enabling resistive switching, thereby stabilising the devices' overall transport behaviour.

After this one-off event, the nine subsequent cycles completely settle into a highly repeatable diode path, with a maximum of 5 μA at -4 V and 6.5 μA at $+4$ V, having a maximum zero-bias resistance of 4 MΩ. These highly repeatable diode paths indicate no further jumps or state changes. The results ultimately demonstrate that the Nb:STO buffer layer is not intrinsically capable of repeatably switching from

one resistance state to another but rather simply stabilises into a fixed, predictable diode junction.

4 Summary and conclusion

This thesis focuses on evaluating how different bottom electrode configurations influence the structural and electrical properties of $Gd_{0.2}Ca_{0.8}MnO_3$ (GCMO) memristive devices. To create the buffer layers (SRO/Nb:STO) between the substrate STO and active layer GCMO, as well as the top contacts (Al and Au), four thin-film samples were successfully created using pulsed laser deposition (PLD) and fabricated with photolithography and e-beam.

The crystallographic characterisation for all four samples has been shown by the XRD analysis and AFM measurements. The XRD patterns of all four structures show a dominant GCMO peak in the same range corresponding to the $(00l)$ reflections. The 2θ values from the XRD measurement indicate that the GCMO thin films have a highly consistent crystal structure, even with the underlying buffer layer (bottom electrode). The ω curve (rocking curve) shows comparable out-of-plane crystalline quality across the samples, with the STO/SRO/GCMO sample showing the smallest peak width, suggesting the small mosaic spread in the out-of-plane direction. In addition to the out-of-plane orientation, the distinct four-fold spot pattern from the XRD texture figure confirms that the GCMO film axes are rigidly locked in three dimensions, establishing high-quality epitaxial growth. The fixed radial distance of the spots ensures a uniform out-of-plane orientation, while their strict 90° azimuthal separation (ϕ) confirms excellent in-plane alignment with the underlying substate grid. But STO/Nb:STO/GCMO implies a larger distribution of the in-plane orientation. The data of unit cell volume analysis provides critical insights into the strain states of the fabricated GCMO films. Compared to the bulk value of 211.67 $Å^3$, the unbuffered STO/GCMO film exhibits the largest volume

(V = 223.45 Å^3), indicating a highly relaxed crystal structure. Conversely, the smaller volumes observed in the buffered samples demonstrate that they are under compressive strain, highlighting the influence of the buffer layers on film structure.

The surface roughness of the thin films was measured by the root mean square (RMS) roughness (R_q) in the unit of nm from the AFM measurement. This value calculates the standard deviation of the surface height and thus is a good way to check the uniformity of the surface and the amount it is bumped up or down. The root mean square (RMS) roughness values (R_q) suggest that the thin films have very flat and uniform surfaces with roughness values ranging only from a fraction of a nanometre to a few nanometres. The high surface uniformity can be directly attributed to the underlying substrate and buffer layers that provided an excellent ultra-flat base that successfully promoted the proper homogeneous growth of the top GCMO layer.

The crystallographic characterisation confirms the epitaxial alignment of the GCMO thin films on the underlying substrates and buffer layers with good quality.

The electrical characterisation shows that none of the device configurations exhibits reliable resistive switching. The unbuffered STO/GCMO sample exhibits an insulating, rectifying state that is rapidly exposed to uncontrolled electroforming. The underlying baselines strongly dominate the electrical behaviour of the modified structures; the Nb:STO substrate behaves as a highly conducting semiconductor, the SRO layer shows fully metallic conduction, and the Nb:STO buffer behaves like a stable, non-switching diode junction. Where resistance changes are observed under bias voltage because of the irreversible dielectric breakdown and noise, rather than a controlled, repeatable switching mechanism. However, the electrical characterisation did not show a clear systematic improvement of the memristive performance in the studied configurations and voltage ranges. Further research is needed to determine if any of these bottom electrode layouts can allow repeatable resistive switching.

Thus, the present results should be interpreted as an exploratory comparison of material stacks.

Use of AI in thesis

This thesis was written with the help of Google Gemini (version 3.5). The AI program was only used as a supportive writing assistant for text editing, summarising long discussion sections, and cross-checking the linguistic clarity of the independent data analysis. All scientific interpretations, data evaluations and concluding remarks are completely original work.

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